

## **Upcoming Milestones for Readout**

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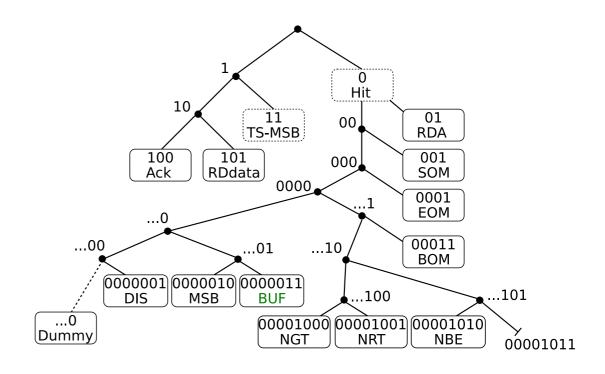
## **SPADIC 2.2 Data Transport, Configuration, Unpacking**

#### New SPADIC words format

- Full usage of Xyter-Frames,
  24 bit instead of 16 bit
- Transport layer in AFCK mostly unmodified
- Timestamp to 8 bit, new epoch frequency
- Baseline calibration to be adapted (Python), frequency

#### Configuration, IPBus core

- New parameters: gain switch, shaping order, trending baseline
- Spadic ui or equivalent



#### Raw data unpacking

- Word and message classes to be updated



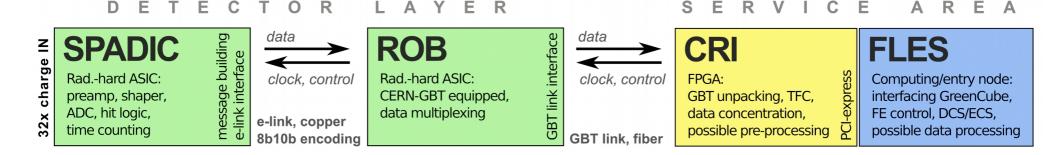
# Multi-SPADIC Frontend Boards and GBTx Integration

#### Multi-SPADIC boards

- Common links for control and clock, to be addressed
- FNR concept to be proven: inter-chip & inter-board

#### GBTX integration

- Chip addressing through GBT layer
- GBTx core for unpacking
- Downlink: LVDS (SPADIC) ↔ SLVS (GBT) matching, currently in CROB-FMC





### **RealMicroslice Building**

#### RealMicroslice building

- Fixing of microslices in real time

#### Microslice format

- Timing master, i.e. TOF-CLOSY handling
- Common readout: time-format in Microslice header, Microslice length
- Data efficiency: full usage of Microslice payload

