RUPRECHT-KARLS-
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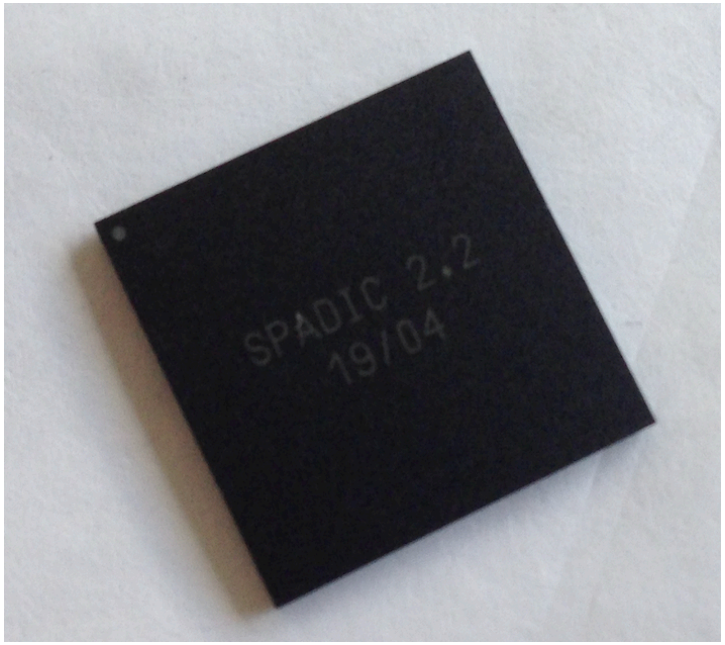
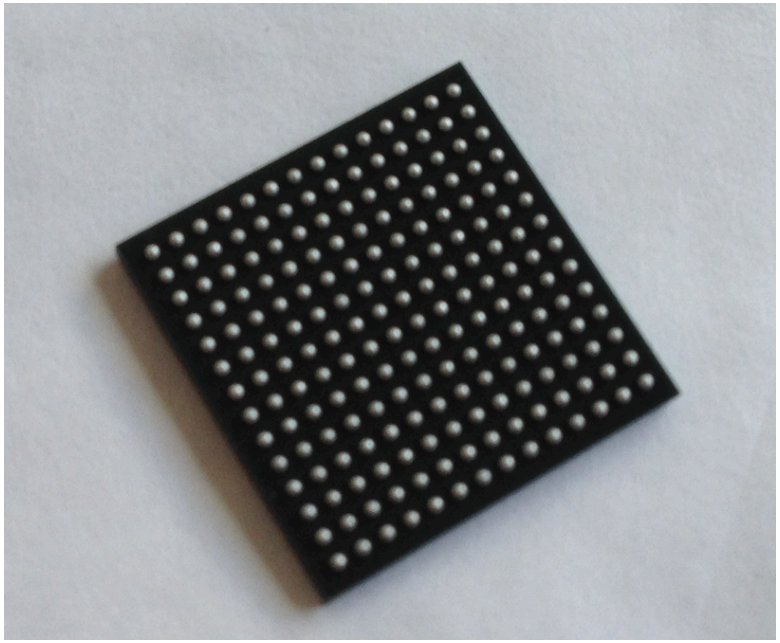
HEIDELBERG

# SPADIC 2.2



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# Purpose of this talk

- Summarize a few properties of SPADIC

- Disclaimer:
  - With the short-notice leave of Michael Krieger, lot of know-how got lost. We had to emphasize to get the chip design done.
  - We are still collecting information and are ‘reconstructing’ the design

  - We clearly need to provide documentation… WIP...

# History

- SPADIC 1.0 initial version, CBMNet Interface
- SPADIC 1.1 bug fixes, (serializer and ‘hangup’ of FE)

- SPADIC 2.0 Elink Interface (inherited from STSXYTER)
  Data not yet packed efficiently
  Packaging in QFP package
  Used for Detector tests
- SPADIC 2.1 Optimized interface (better data packing)
  Problem: No RAM in Chip (mistake at IMEC)
  Packaging in BGA packages
- SPADIC 2.2 Design very close to 2.1
  Changes for instance
  - synchronisation of counter reset
  - more flexible hit detector

# SPADIC 2.2

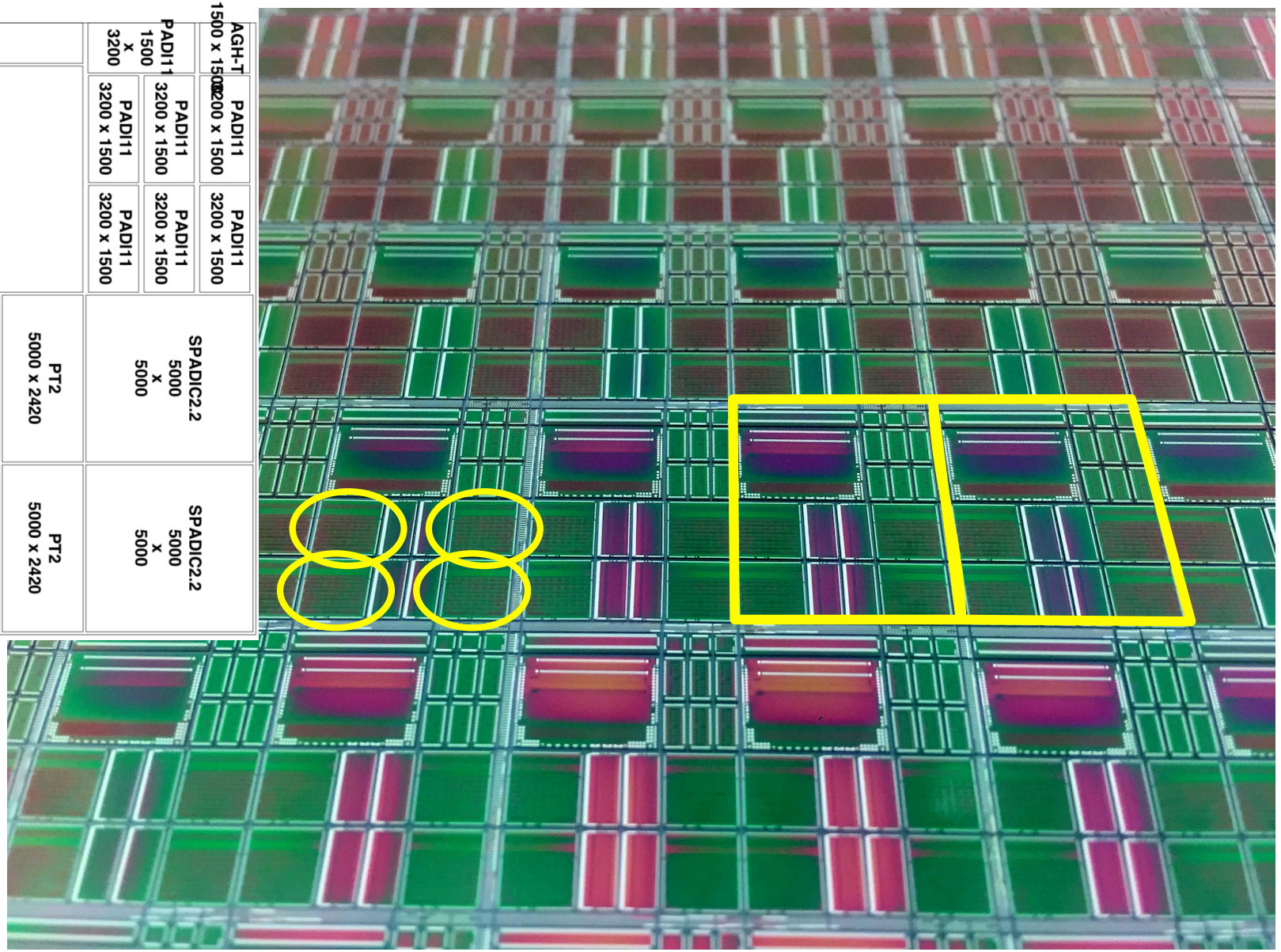
- Submission via common CBM engineering run
- 24 wafers processed
- 8600 Chips delivered
- Packaged in BGA packages (chips now in Frankfurt)

- ~15000 chips needed for full TRD, incl. spares

- A new chip fabrication will be started soon by GSI (bug fix in PADI). This will give us all the chips we need

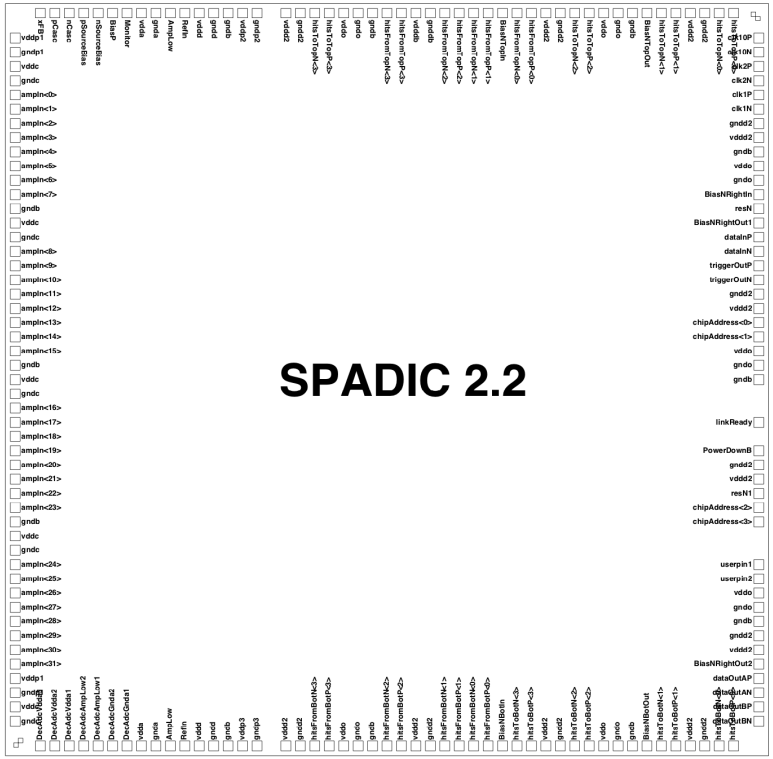
- Packaging must be done quickly because available BGA carriers will expire (company will refuse to use them later ~middle of the year)

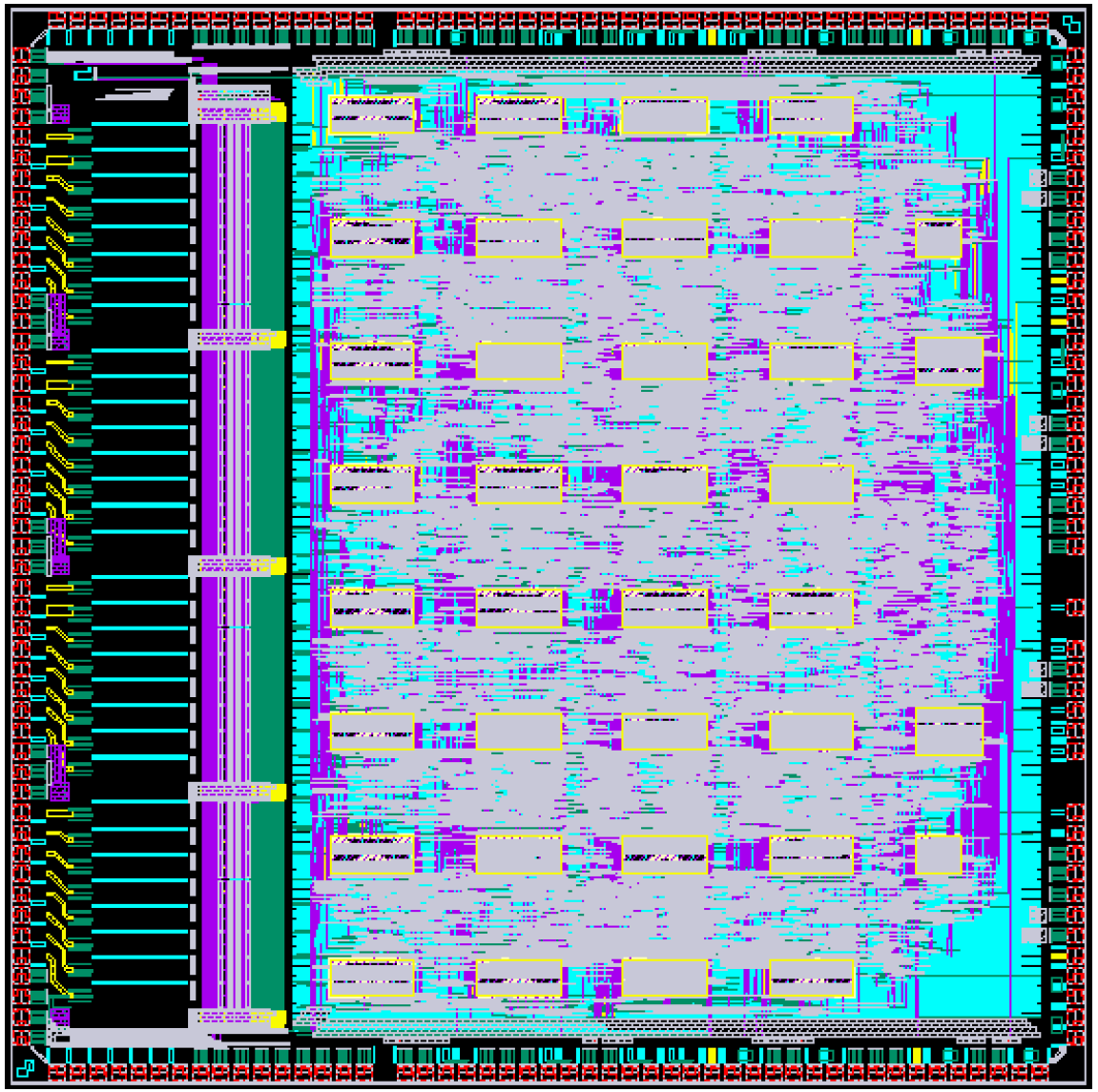
# Reticle and Wafer



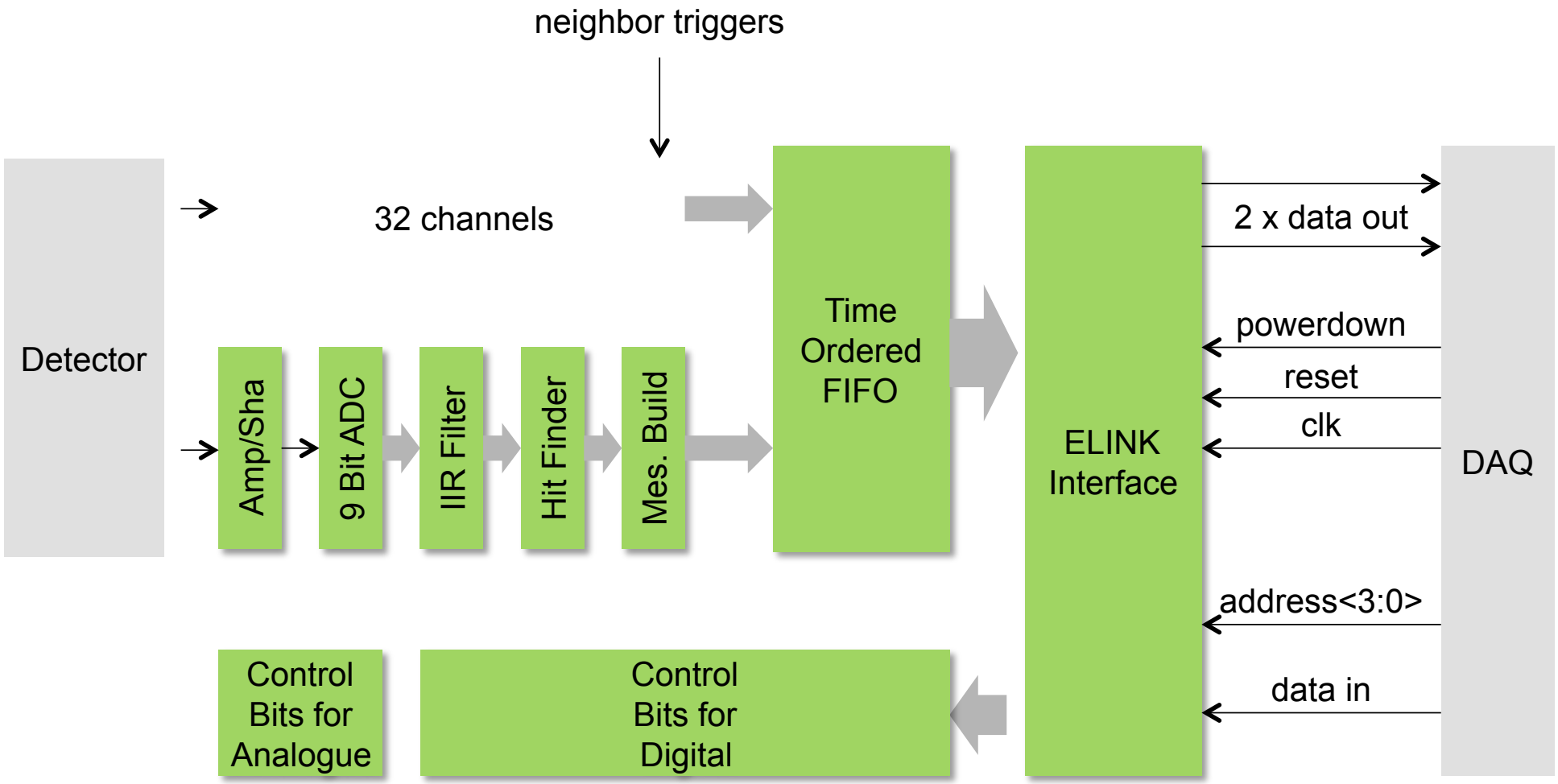
# Pinout

- Pins of 2.2 identical to 2.1

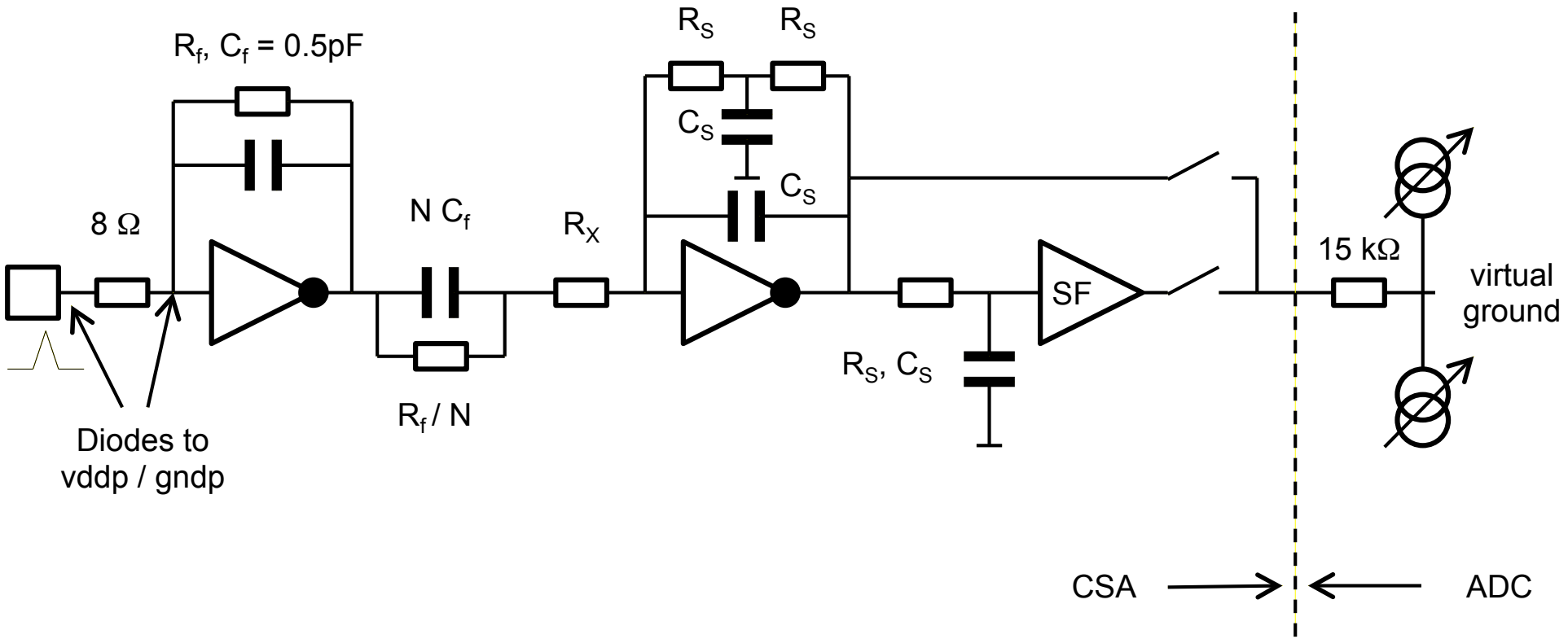


# SPADIC Overview



# Frontend


$R_f$, $C_f$ = 0.5pF
$R_S$
$R_S$
$C_S$
$C_S$
8 Ω
N $C_f$
$R_X$
15 kΩ
virtual ground
SF
$R_S$, $C_S$
$R_f$ / N
Diodes to vddp / gndp
CSA
ADC

# FE / Shaper (2.2)

- Only positive input polarity
- Input protections (adding some noise) as before
- Overload recovery diode in CSA
- Default Shaping is CR-RC with peaking time of 120 ns
- Can switch to CR-$CR^2$ shaping with 240 ns peaking time (with additional source follower) – selectable
- Gain can be reduced to ½ to extend ADC range - selectable

- ExOR in/out to all configuration bits (for checksum)
  - All configuration bits in analogue and digital part
  - Checksum is transferred with every ACK frame

# Overall Feature

- Added PowerDownB = AnalogPowerOn pin
  - it disables the internal reference so that all bias go to 0

- This allows smooth chip start:
  - Analogue Consumption is turned on before power is applied
  - Then registers are configured
  - PowerDownB is released

# ADC

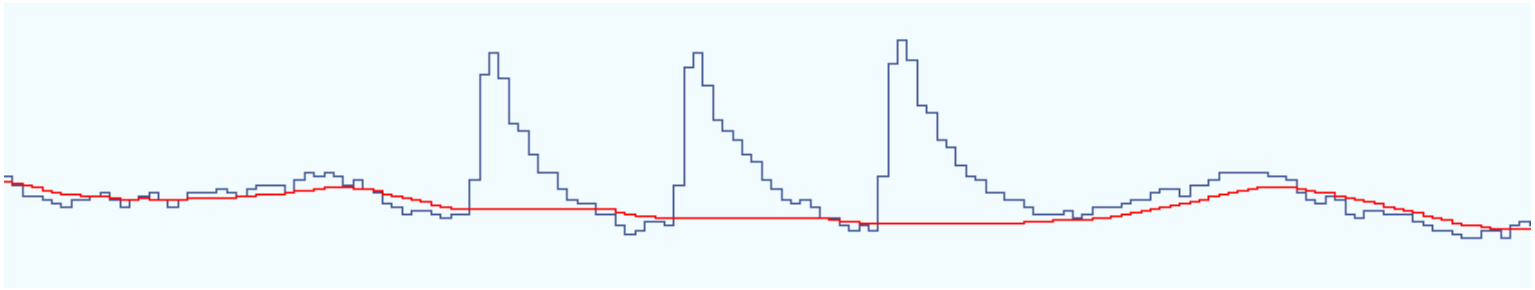
- 9 Bit
- As before
- Clocked Slower due to slower ELINK Clock (160 MHz instead of 250 MHz for CBMNet) and slower shaping: 16 MHz

# IIR Filter

- As before
- Disabled stages do not draw power (clock disable)

# Hit Finder

- Triggering schemes have been extended wrt 2.1
- 2 x 4 external neighbour triggers (one more than before)
- One more presample
- Alternative selection mask can be defined for multi hits
- Running average of baseline implemented in each channel
  - suspended if there is a hit
  - can be selected instead of the first regular sample
  - simulation output:



- Trigger Logic has been enhanced with multiple thresholds etc.. (Old Logic is still there, one bit selects which to use)

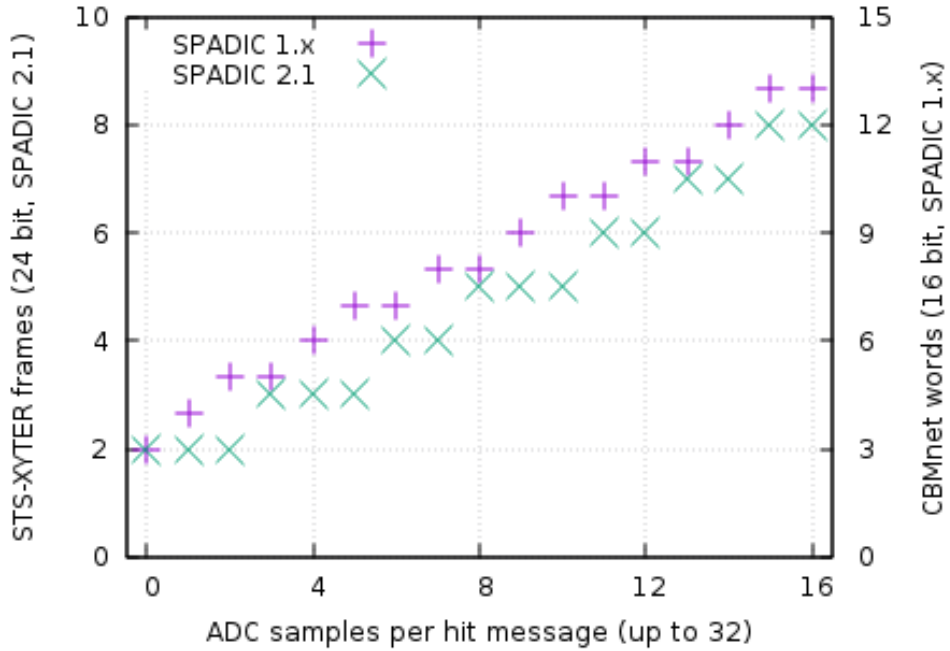
# Data Aggregation

- Pulse picking can use different pattern for double hits

- More flexible than in 2.0 (1 or 2 links)
- More efficient implementation (eliminated one FIFO)

# Data Format

- New, compressed data format has been implemented (same as in 2.1)
- This is described in detail in a document
- Minimal words with 1 ADC sample require only 2 frames



# Proposed data format for SPADIC 2.1

Michael Krieger

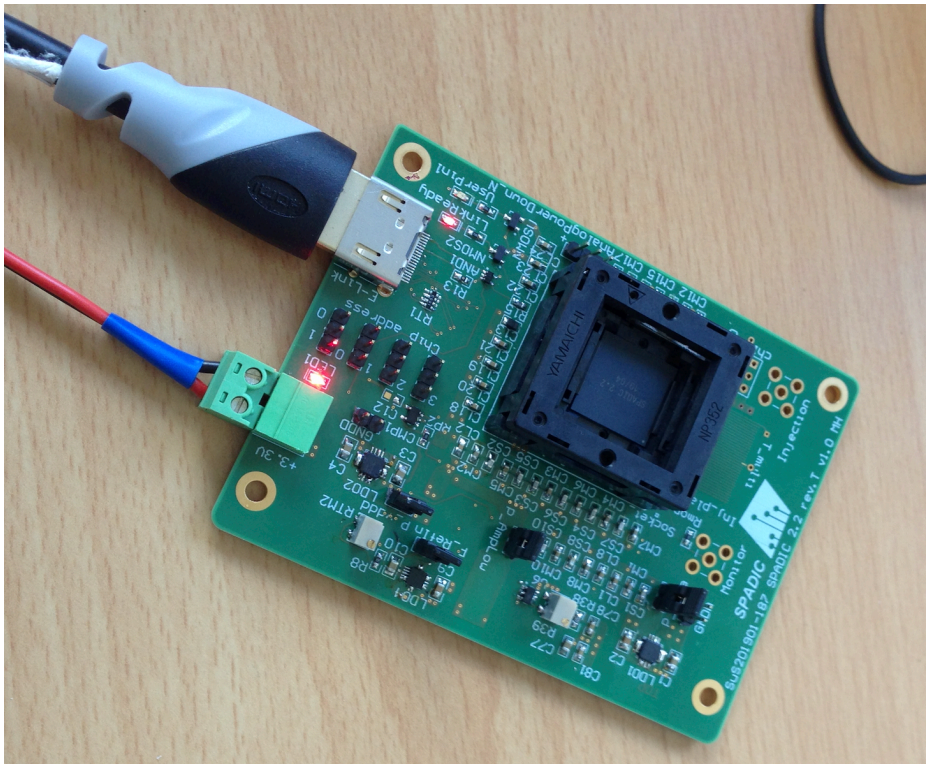
Revision be0dafb
April 18, 2018

and implemented!

## Contents

# Setup for KGD Testing

- Chips will not be tested in wafer, but in package
  - due to high yield, money lost by packaging of broken ASICs is less than the effort to test them on a probe station
- Test setup for SPADIC2.2 is ready (HiWi Marcel Hun)
- Uses a commercial ZIF test socket




- Status:
  - Power Consumption OK
  - Links comes up
- Need to modify control software

# Next Steps

- Establish communication to Chip
- Modify data receiving software to unpack the frames according to the new format (Doku available)
- test all, in particular new, feature. Doku missing.