FASP based data acquisition

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CBM-TRD Retreat
27-29 March 2019
Schloß Waldthausen

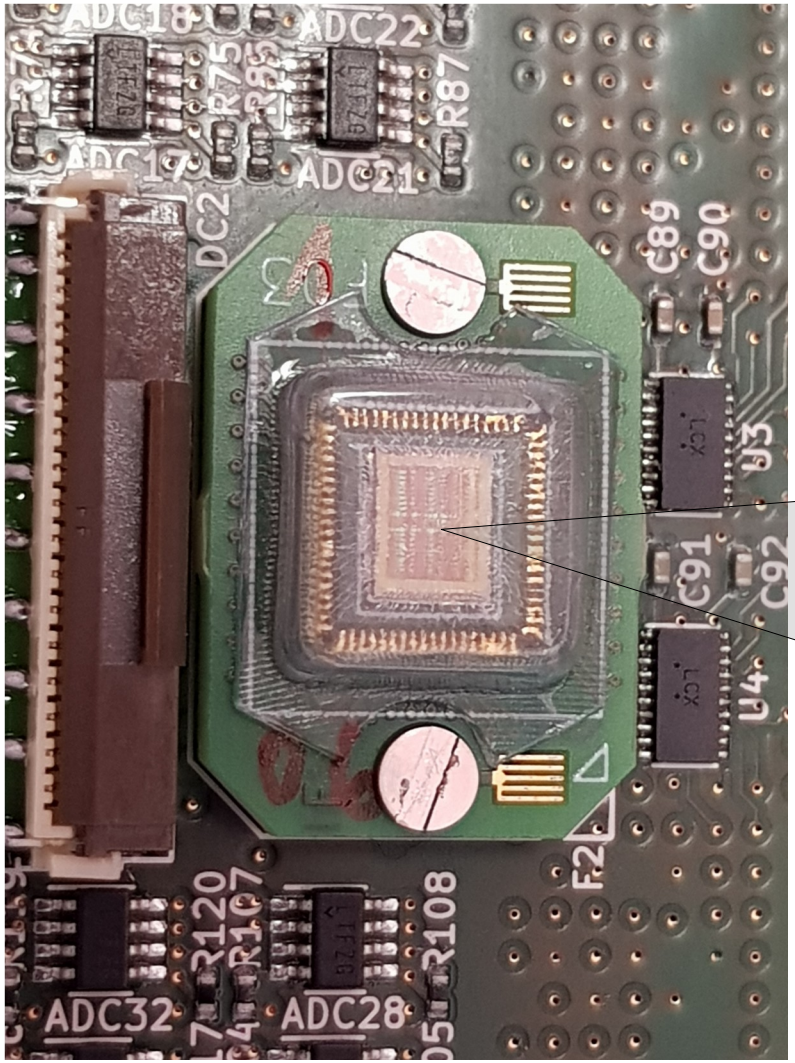
Motivation & Outlook

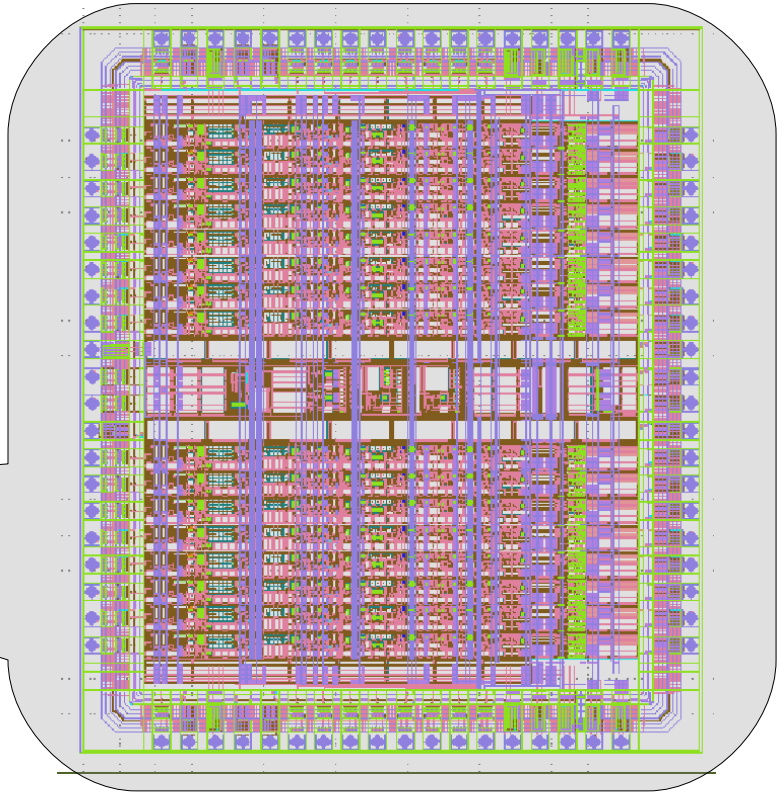
- **Fast Analog Signal Processor**
  - Fast : shaping time of 100 ns optimally selected for < 250 ns response time and full charge/particle integration.
  - Analog : Max. signal detection, base line correction, fast recovery on overflow, etc.
  - Signal Processing : Max. signal holding (Flat-top), channel-wise trigger logic (chip select)
  - Specialties : Non-diagonal response matrix for triangular pad geometry, neighbor trigger (small signal processing based on topology), CHIP to CHIP analog/digital communication.
- **General Event Time-stamping Serializer**
  - Digital companion of FASP : control and command I/O with FASP
  - Packs 2 FASPs : packs signal-time information for 32 chs
  - Data volume scales with hit rate.
  - Freezing in silicon to be discussed.

Front End Electronics

- FASP v03
- GETS
  - *Firmware*
- TESTS
  - *Rate*

FASP v03



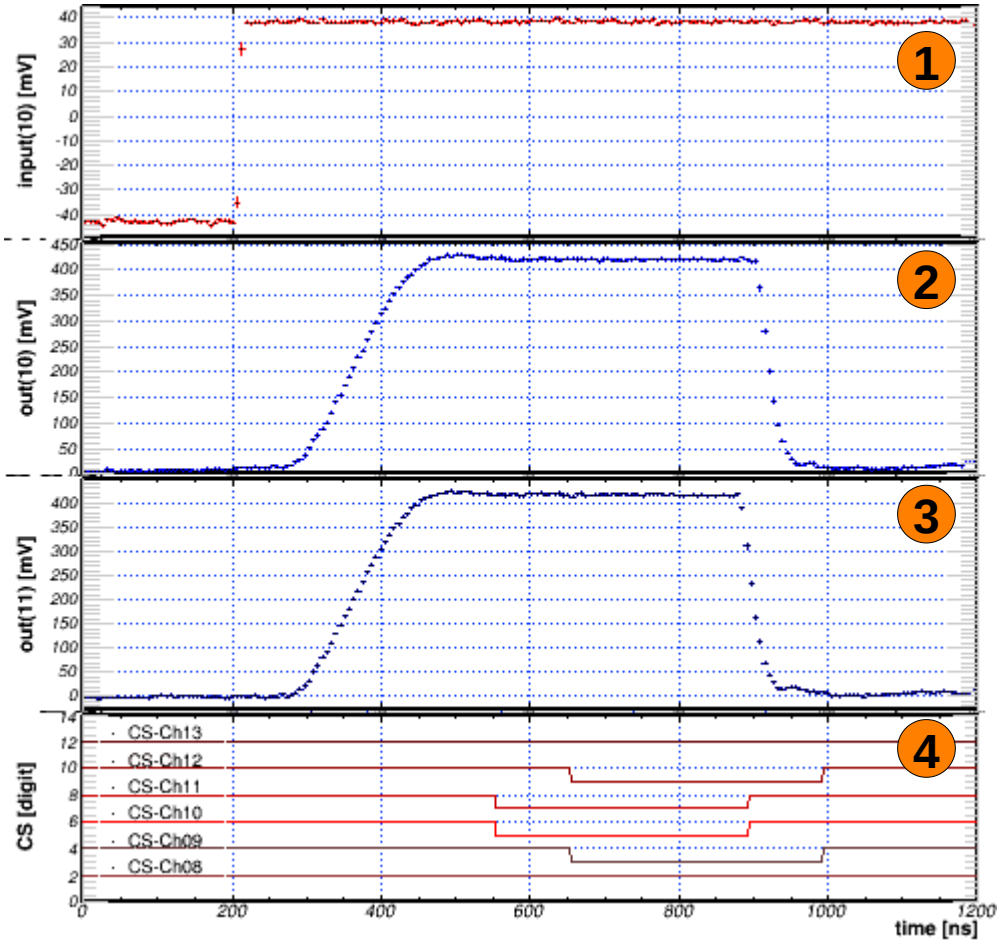


v03 prepared for mCBM has
- improved analog circuitry and
- a new processing logic for neighbor read-out.

See A. Bercuci et al.; FEE readiness of Bucharest TRD chamber for mCBM, CBM Progress Report 2018

CHIP-wise QA

CHIP production (AMS)
CHIP bonding on FASP-board (HPD)
CHIP testing on Test-board (HPD)



1. Pulser signal

2. Analog out on direct channel

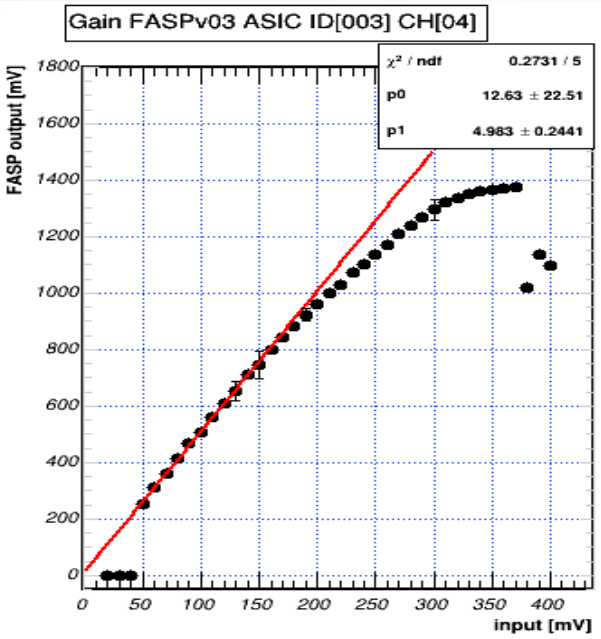
3. Analog out on paired channel

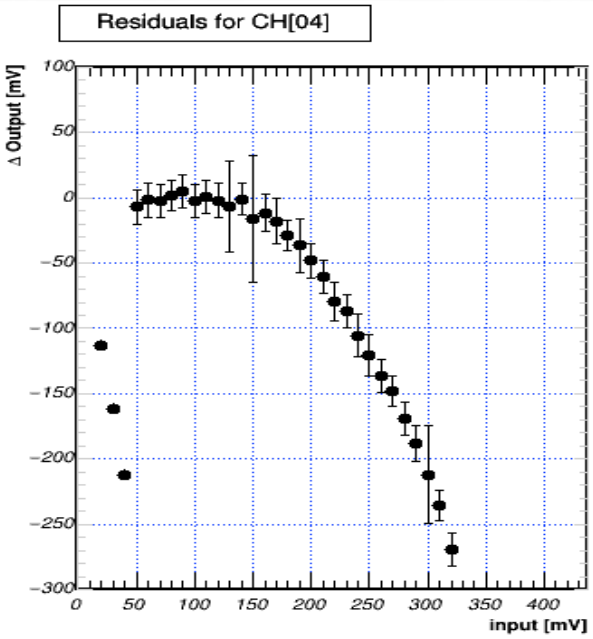
4. Triggers (NE)

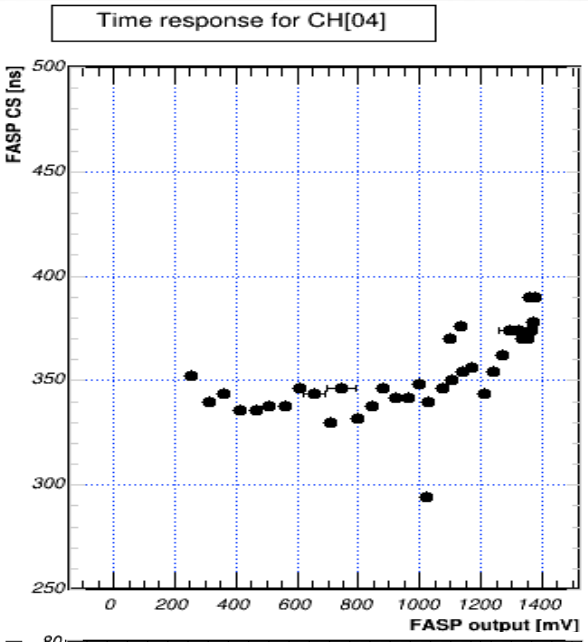
Production projection

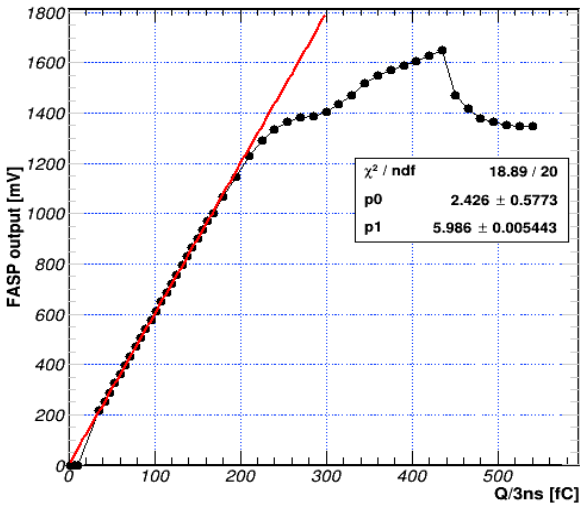
- Currently 6 chips/2 FTE/2 weeks !
- 1 type Module 1 (e.g. at mCBM) is operated by 180 FASPs or 2880 channels
- bonding externalized
- QA need development

Channel-wise QA



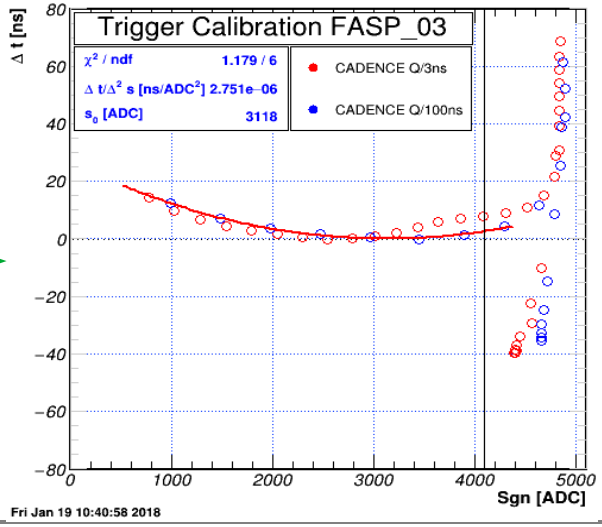




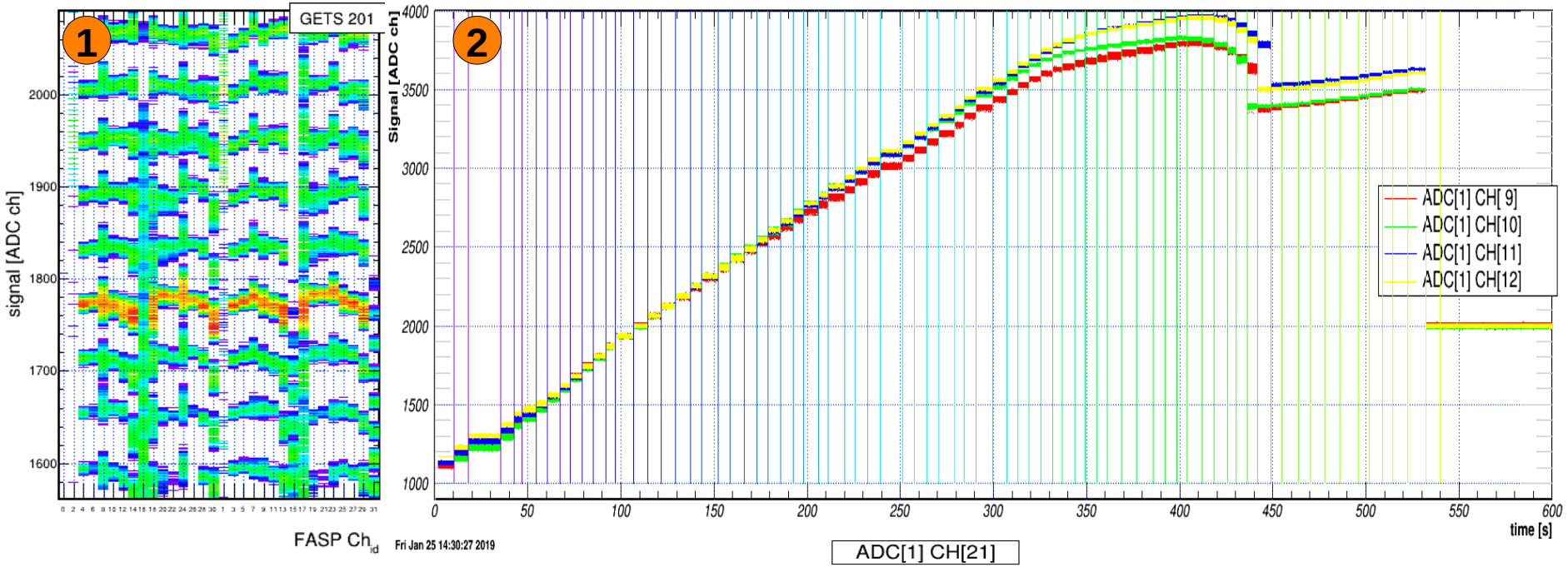


FASP03 MWPR 2019

CADENCE



Calibration

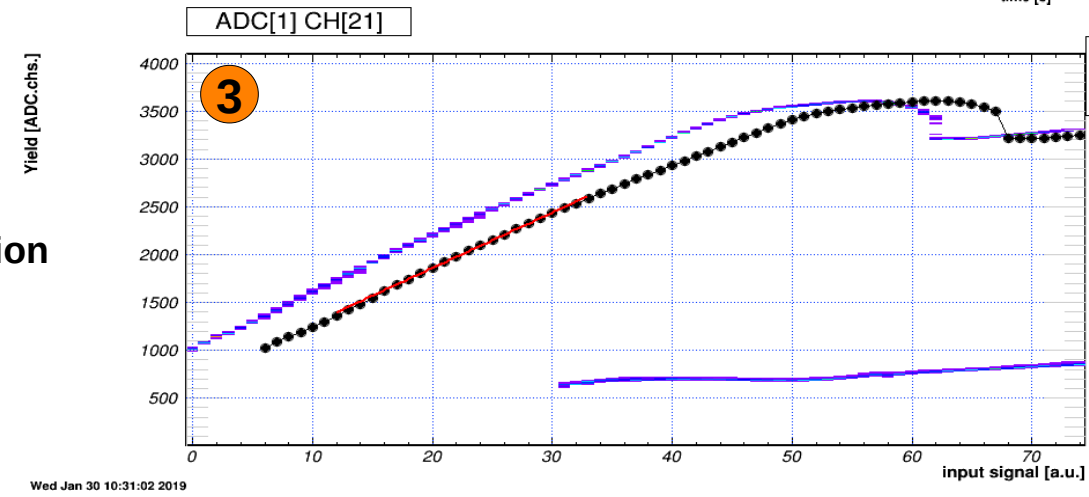


1. Pulser FEE calibration run

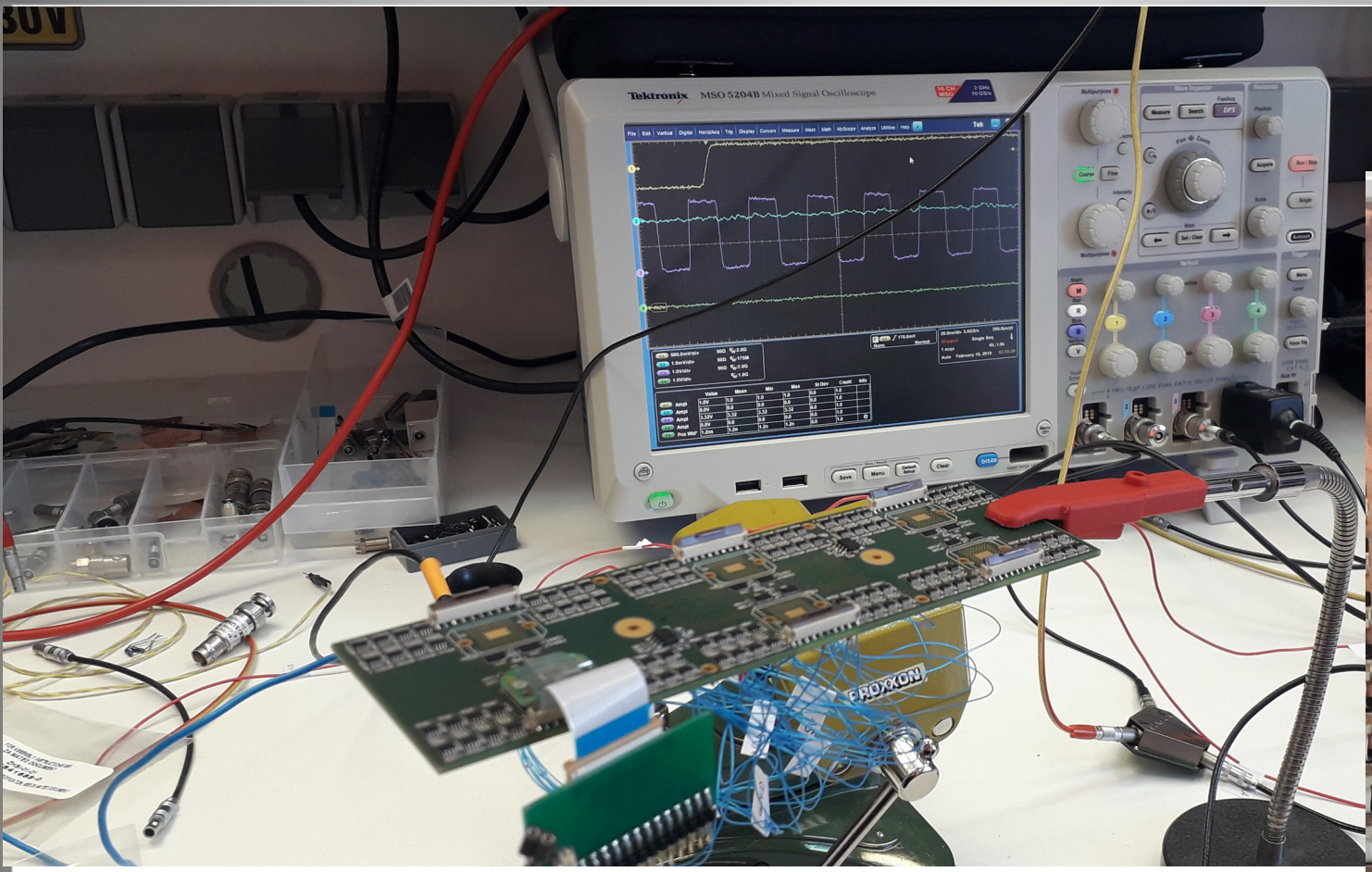
2. Time expansion of Pulser run

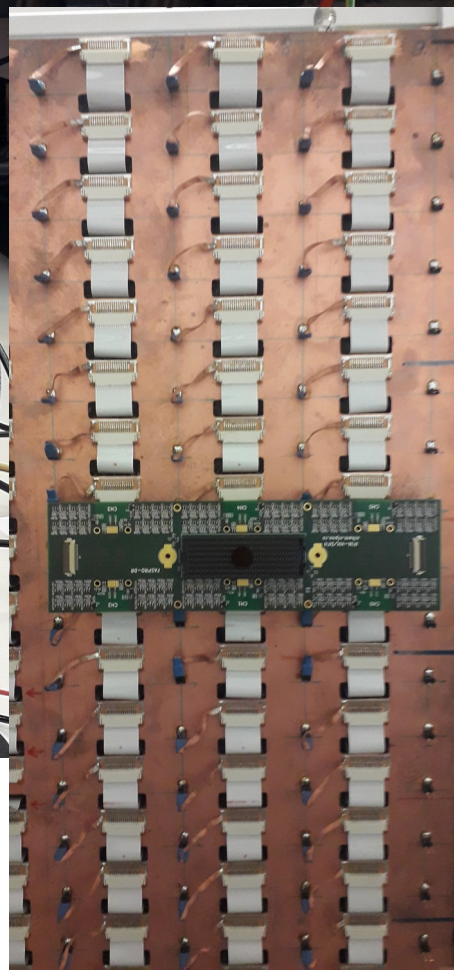
3. Ch-wise FASP-gain identification

FEE calibration



FASPRO : FASP FEB



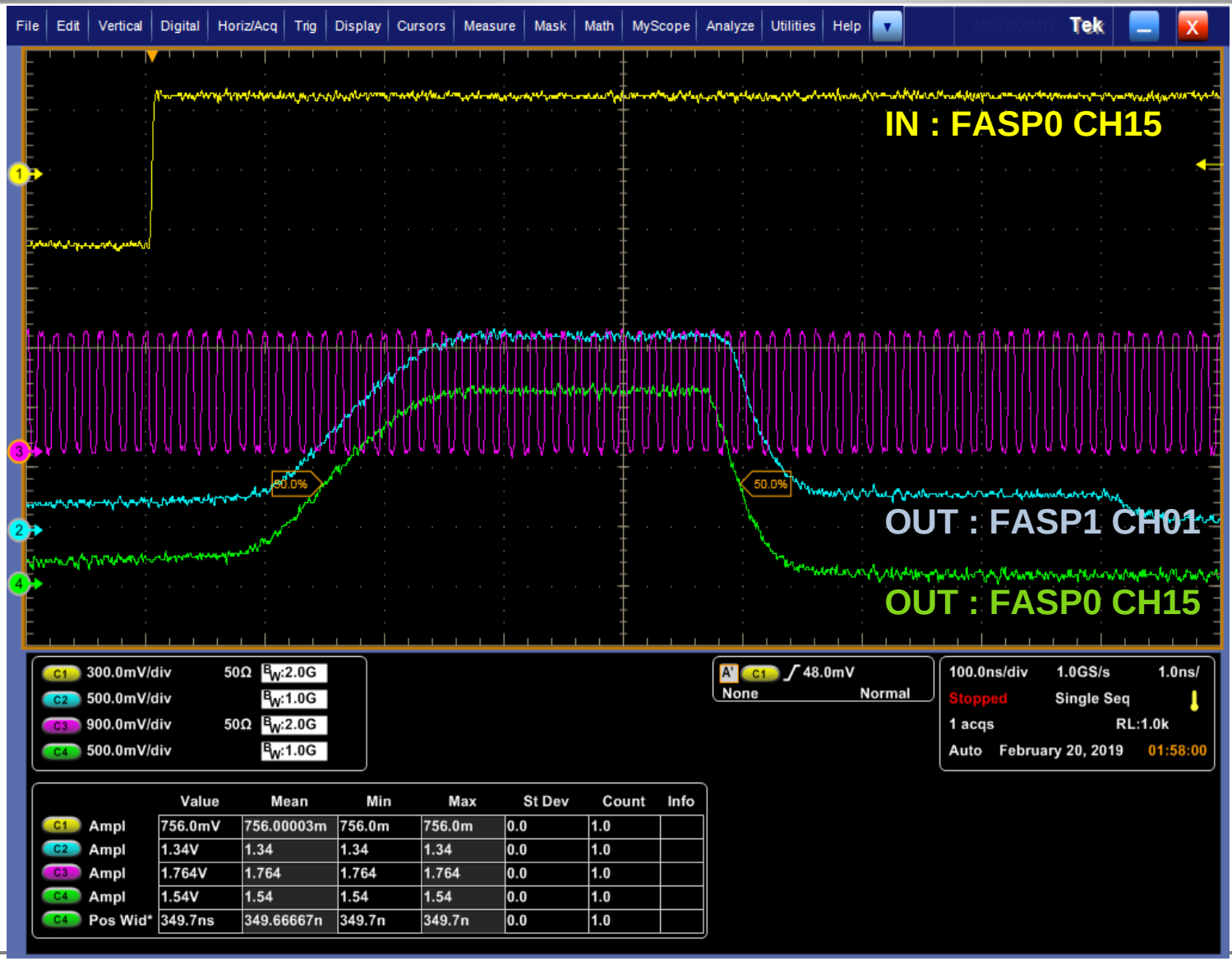


A very preliminary but successful first test

- CLK 80 MHz
- CHIP 2 CHIP communication works (finally)
- Bugs in mounting the FMC+ connector. Fixing at producing firm

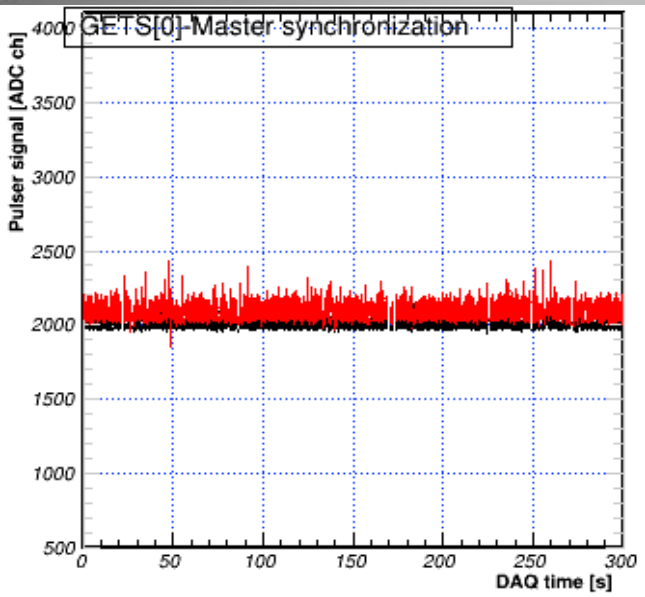
FASPRO : FASP FEB

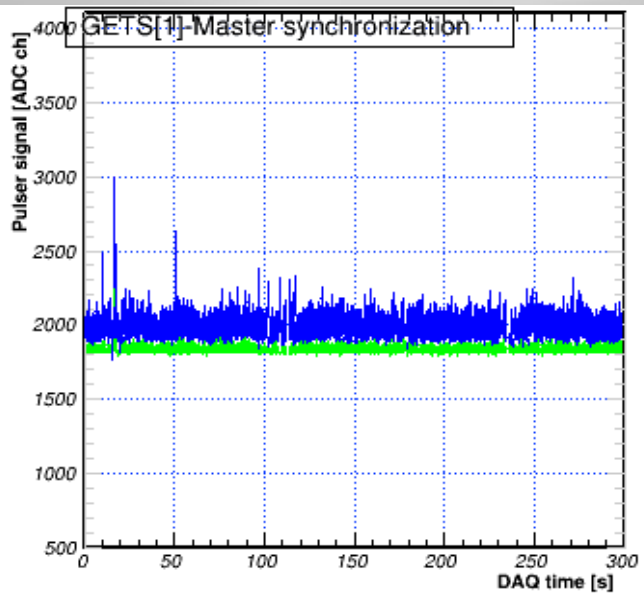
CHIP to CHIP communication

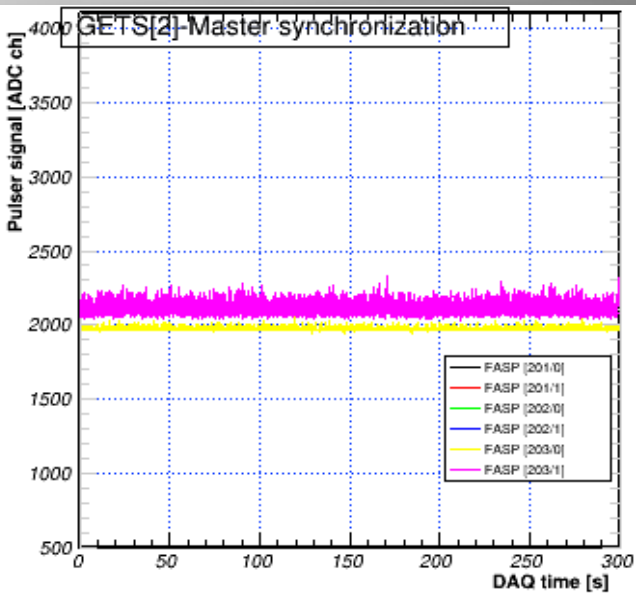


CHIP to CHIP communication

GETS : Tests @ close to 100 kHz particles/cm²

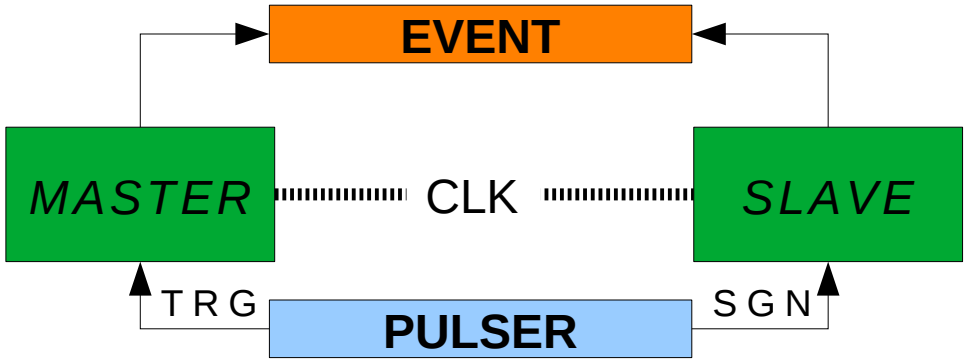






QA

System Synchronization Test



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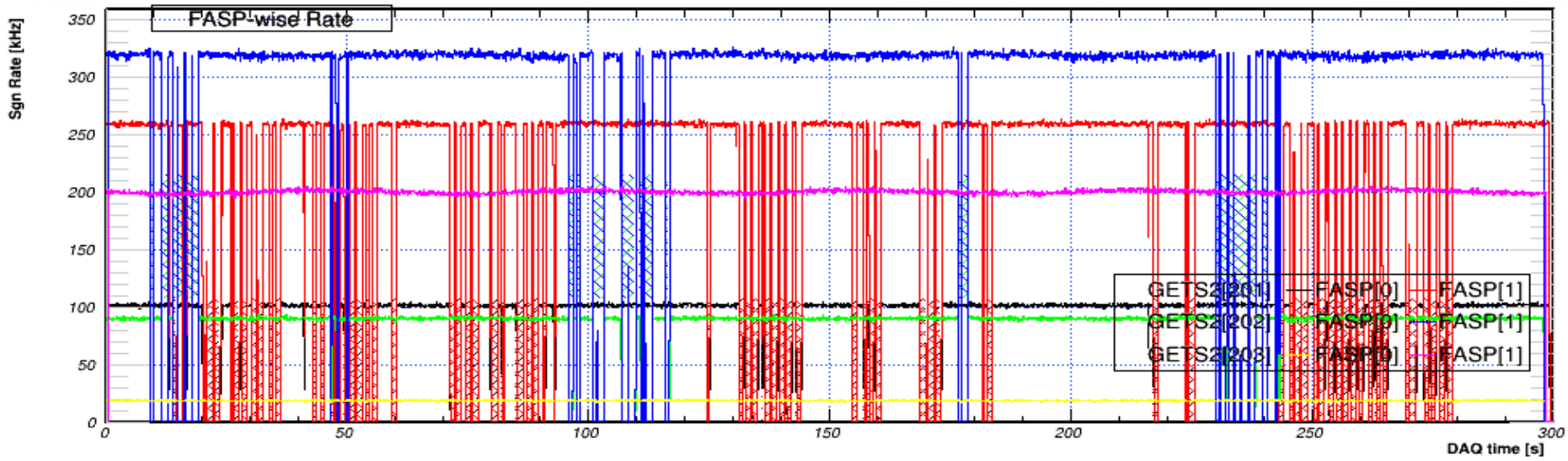
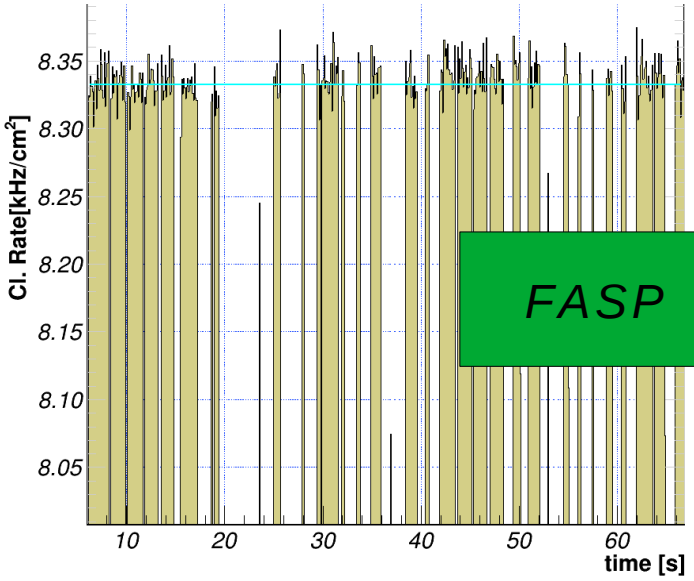
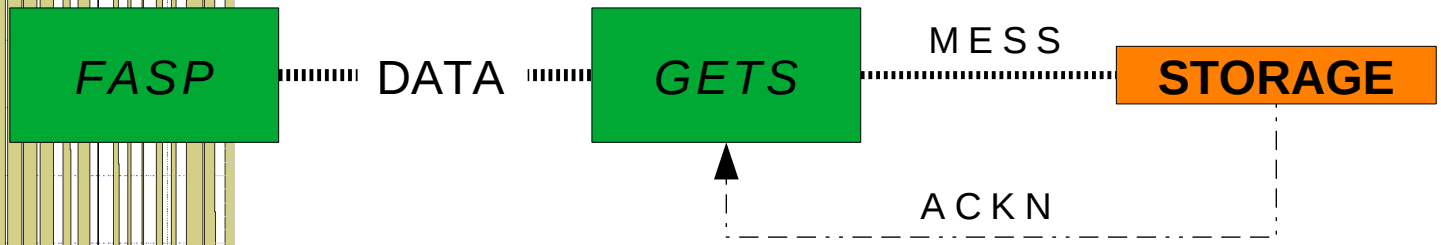




QA
GETS-STORAGE Communication Test



GETS → for mCBM and beyond

STATUS

1. Delay on building the GETS board for mCBM due to shipping delays (1 year) of new FPGA from microSemi PolarFire

2. Days before the FPGA arrived

3. GETS board (housing 2 GETS) is first priority

4. Deadline Nov. 2019 for mCBM installation

5. We consider freezing the system and casting it to silicon for CBM but decision still needs evaluation.

6. We try to keep the solution as flexible as possible for as long as we can ...

CBM-TRD
Bucharest team

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BACKUP

RATE → real life signals @ 100 kHz/cm²