Status of SPADIC front-end boards

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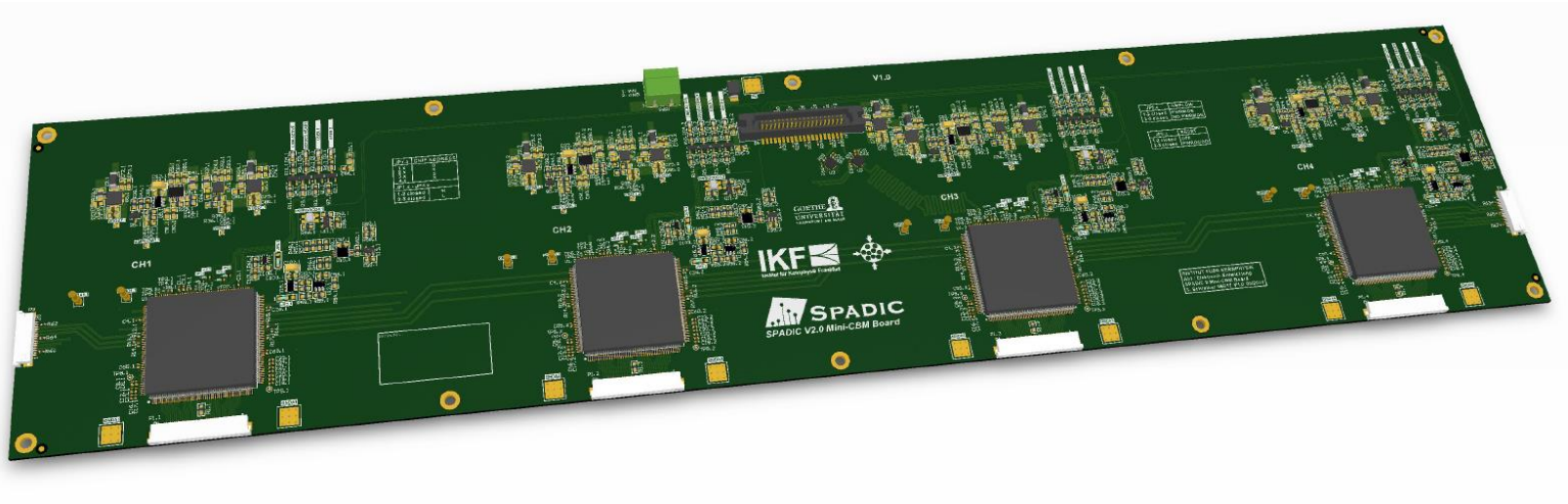
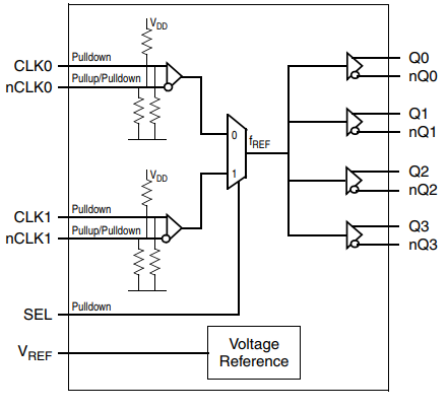
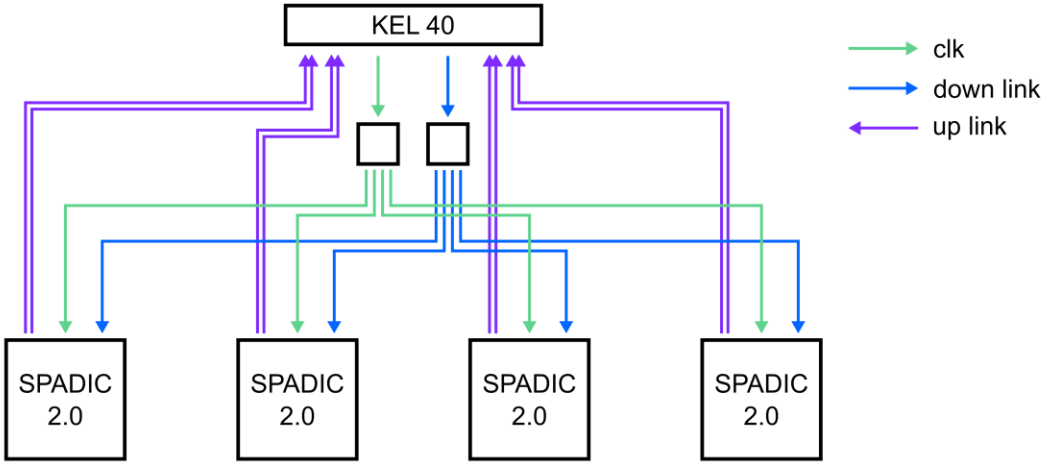
Quad SPADIC 2.0 FEB



- Shared clk and down link



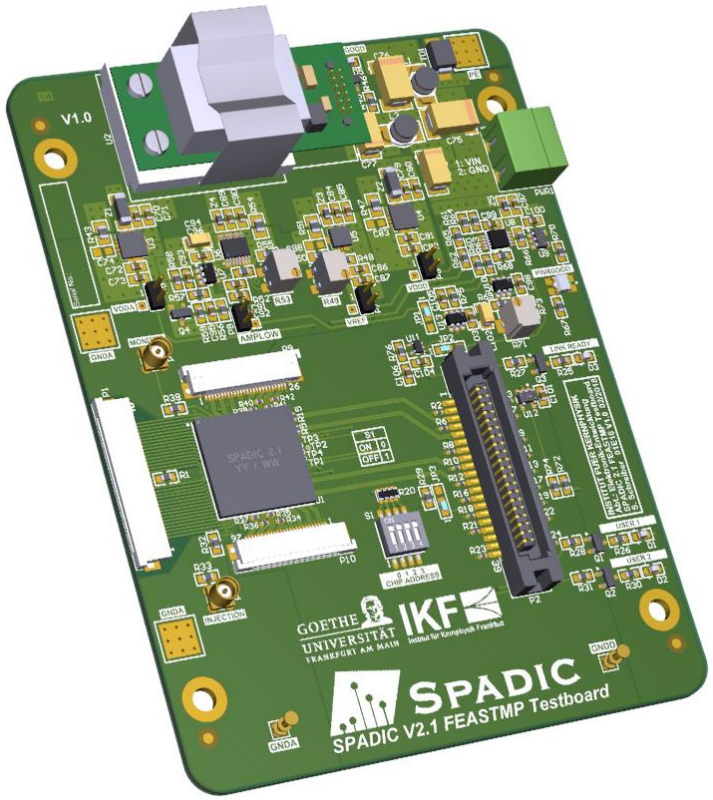


LVDS Fanout Buffer 8P34S1204NLGI

Single SPADIC 2.1 FEB

- BGA packaging (15 x 15 mm²)
- Added power-down input for analog part
- Four inter-chip neighbour trigger

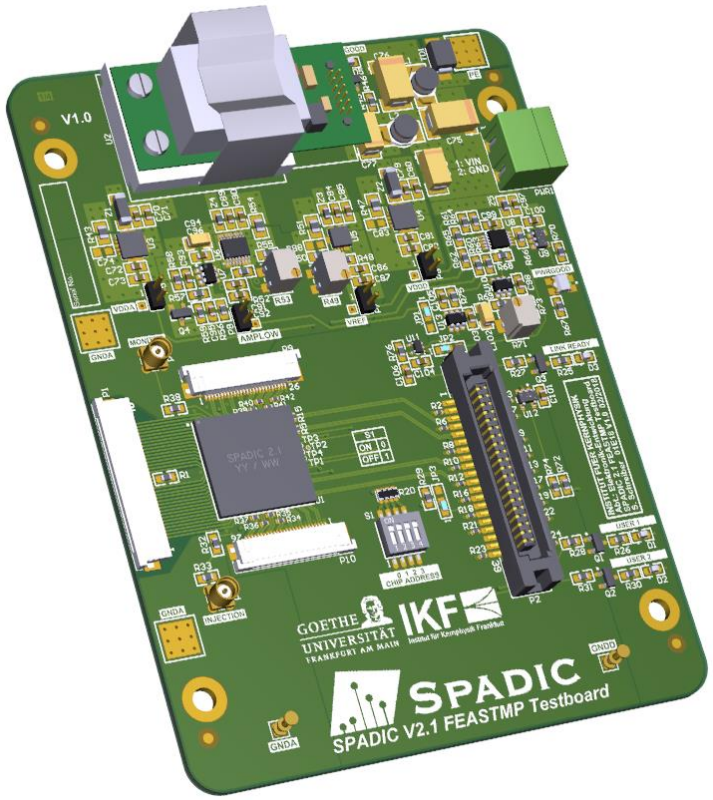
- Registers are read and writeable
- Due to an error by the manufacturer produced without memory



Single SPADIC 2.2 FEB

- Pin compatible to SPADIC 2.1
- Same PCB layout

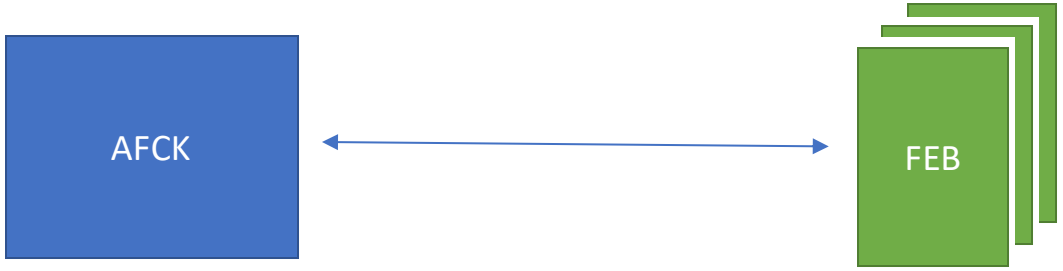
- Currently at the assembler



DAQ Setup

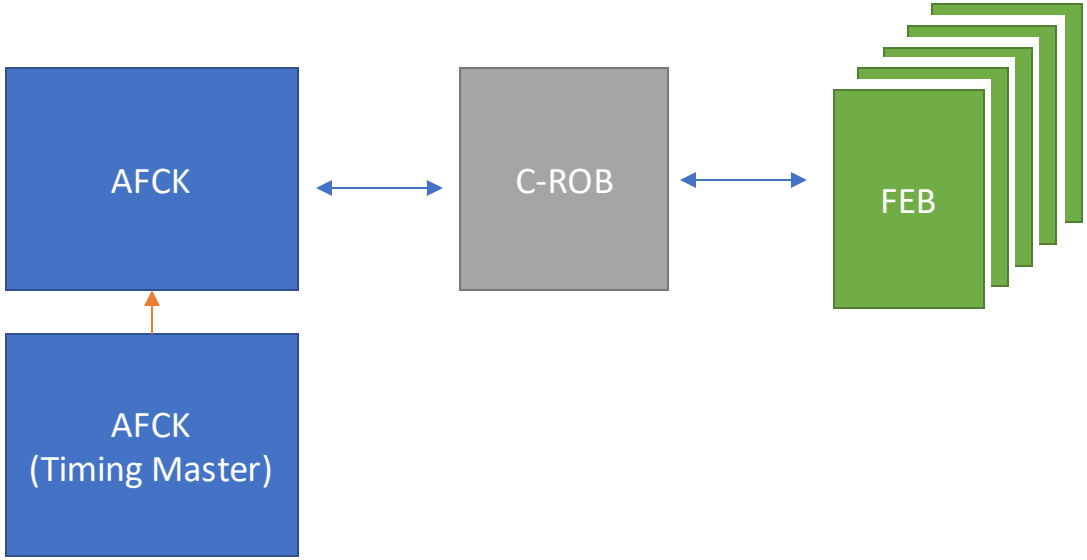
Basic Setup:

- Readout of up to three FEBs
- Only one AFCK required

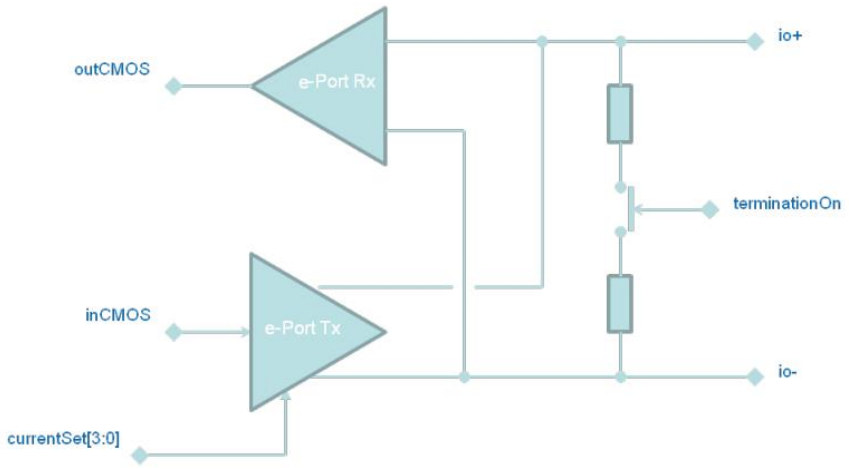


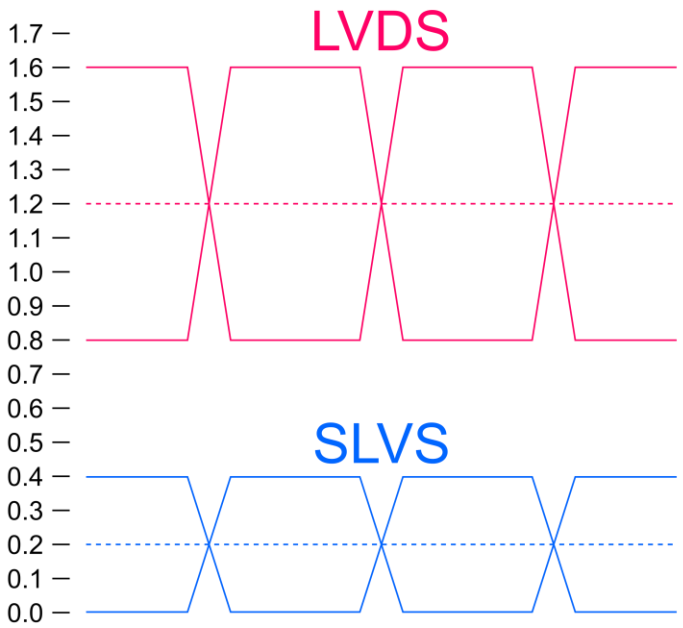
C-ROB Setup:

- Readout of up to six FEBs
- Requires additional AFCK as "Timing Master"
- Vital for mCBM/CBM



Connection to the C-ROB





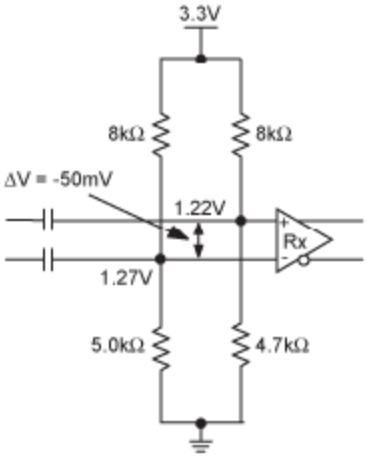
E-link **receivers** are capable of handling LVDS and SLVS.
E-link **drivers** have a programmable output current, with a mean voltage of 0.2 Volt

LVDS: differential signal with a voltage swing of **±400 mV** centred on **1.2 V**
SLVS: differential signal with a voltage swing of **±200 mV** centred on **0.2 V**

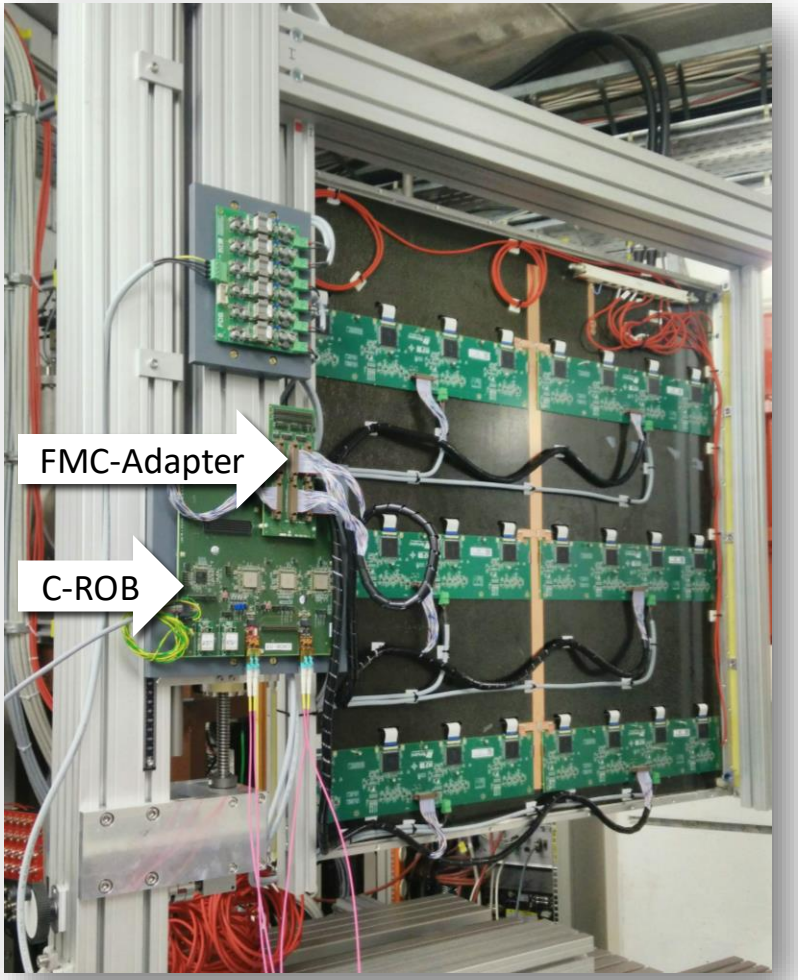
Connection to the C-ROB

The solution:

- AC-Coupling + Biasing
- Possible due to 8B10B encoding
- Implemented on the FMC-Adapter



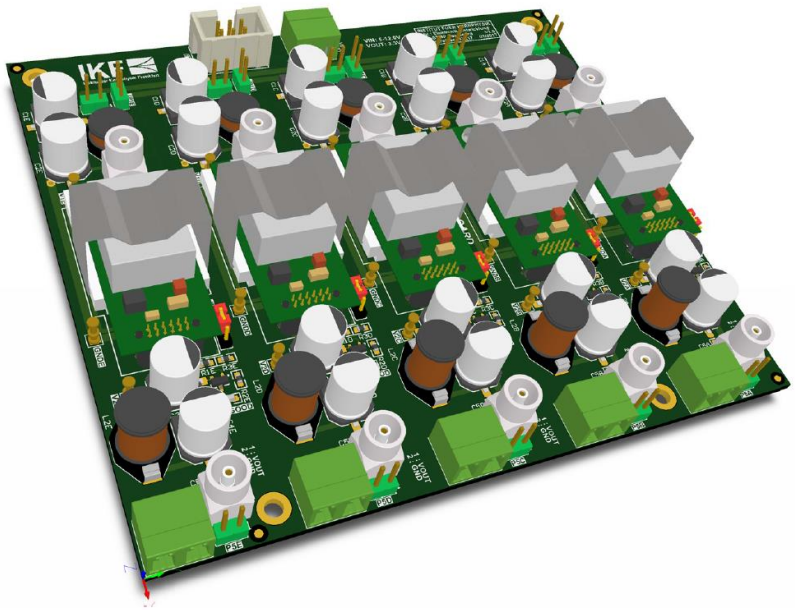
Example circuit, not necessary the one used by Cruz.

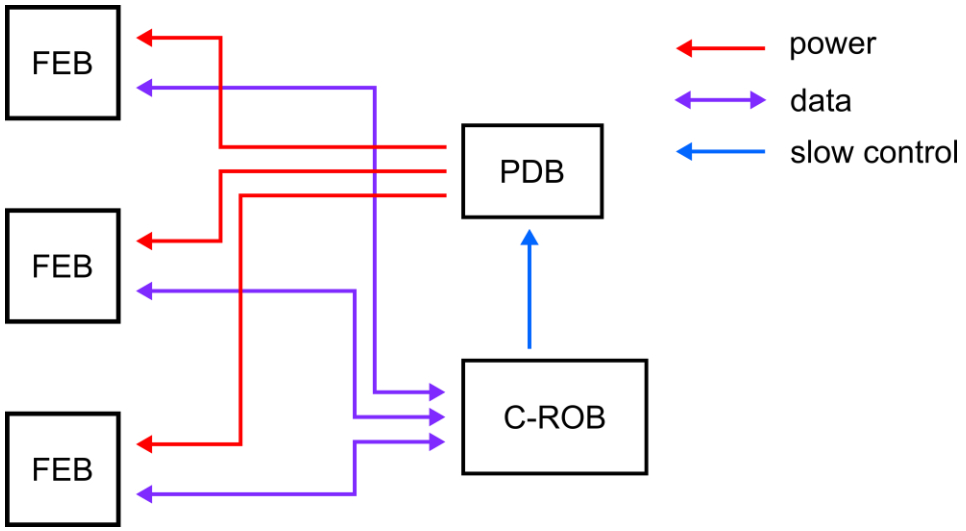


Quad SPADIC 2.0 FEBs at mCBM

BACKUP

Power Distribution Board





- 2.5 Volt FEAST-MP
- Controlled by the FMC-Adapter on the C-ROB
- One board per chamber (at mCBM)

Quad SPADIC 2.0 FEBs at mCBM