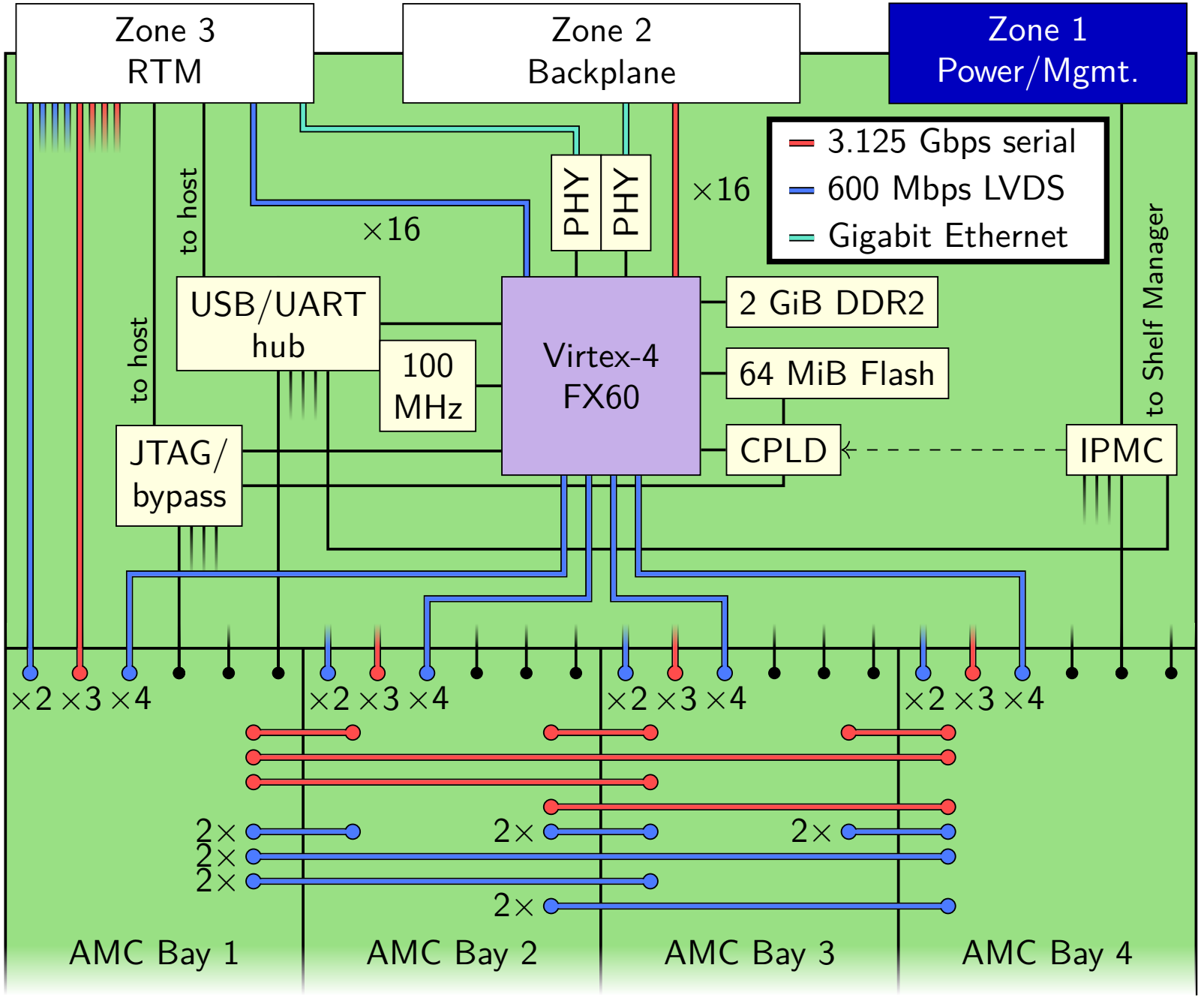
Update on New CN Design

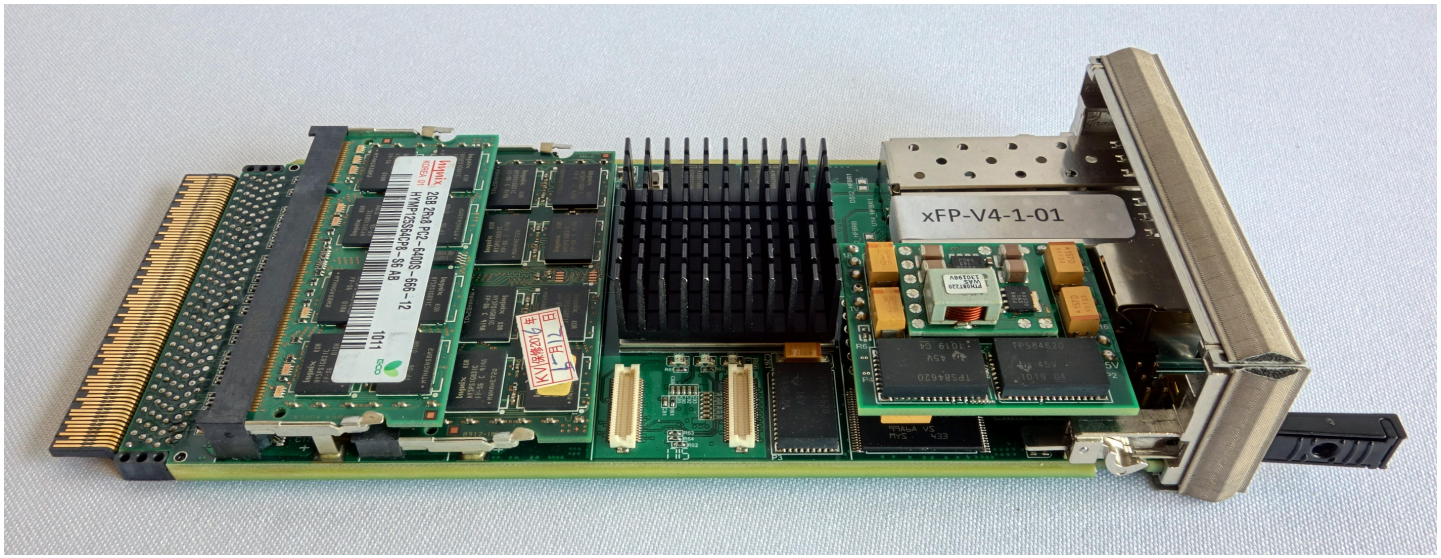
May 2015: Compute Node Carrier Board (CNCB) v3.3

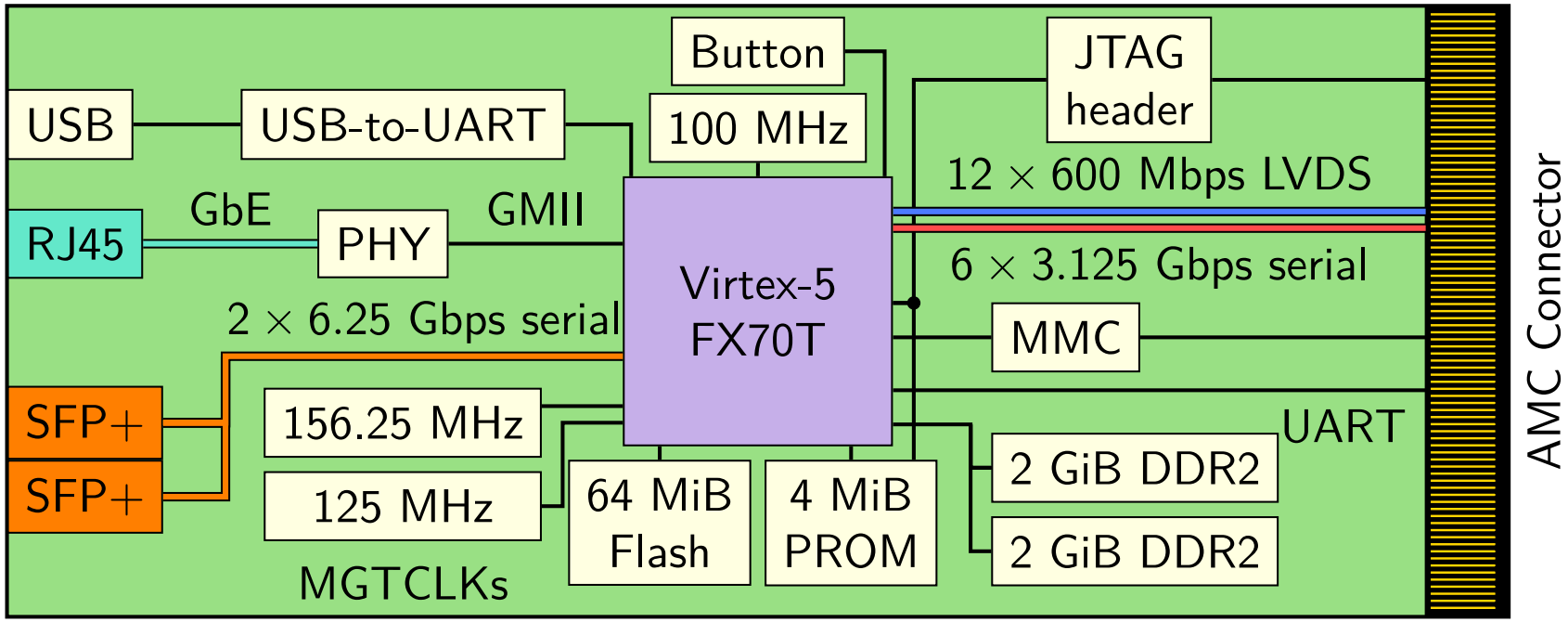
- Four full-width **AMC slots**
- Virtex-4 FX60 FPGA as **switch** to ATCA backplane

May 2015: Compute Node Carrier Board (CNCB) v3.3



Nov 2014: xTCA-Based FPGA Processor (xFP) v4.0





Compute Nodes in the ATCA Shelf

Two fully equipped Compute Nodes, one backplane GbE switch

xFP Cards in microTCA shelf

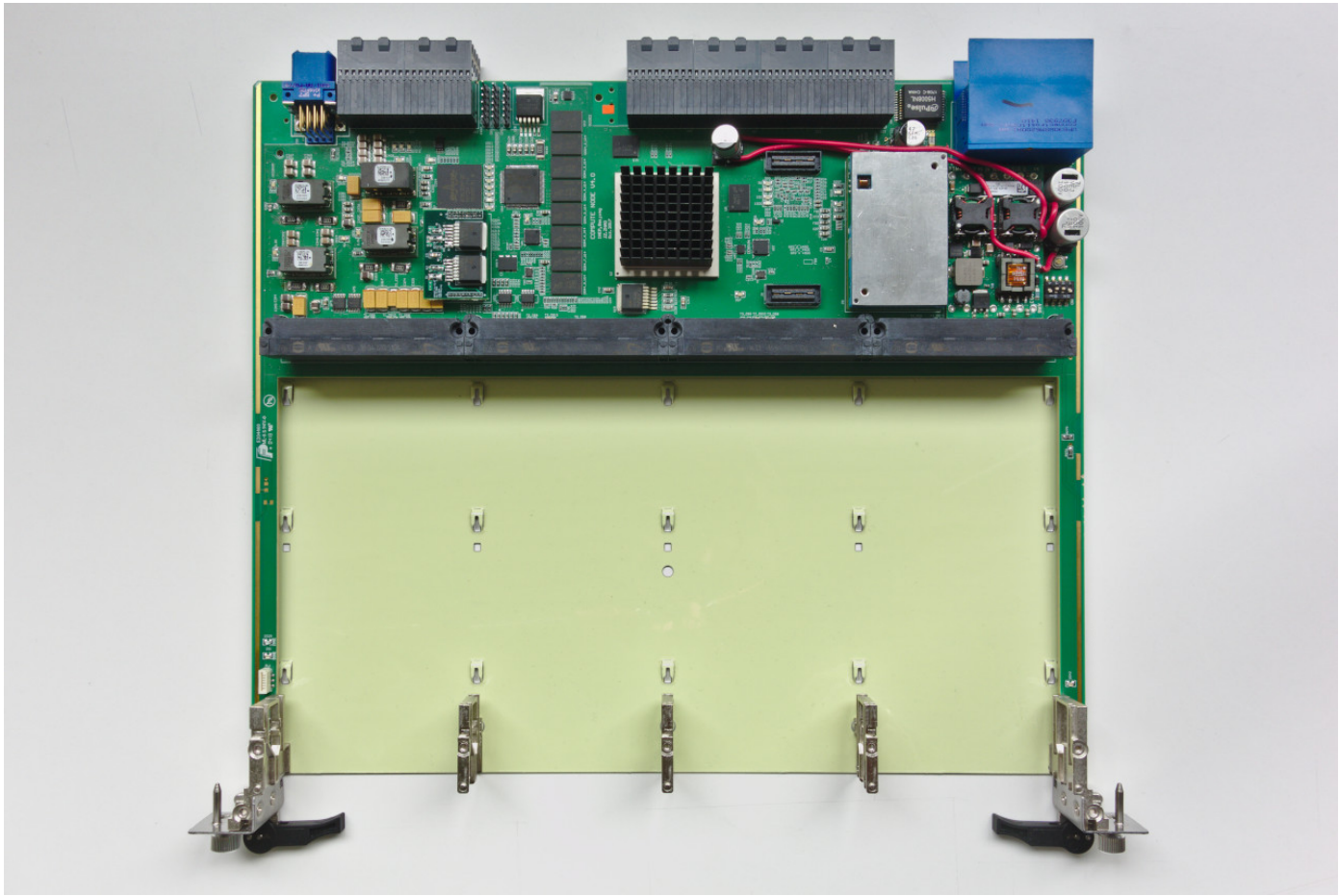
Compute Node Upgrade: Carrier Board

- **First step:** upgrade Carrier (but stay compatible with current AMC)
- **FPGA:** Change to Xilinx UltraScale architecture

	Virtex-4 FX60 (CNCB)	Virtex-5 FX70T (xFP)	Kintex UltraScale 060 (Upgrade)
Registers	50k	44k	663k
LUTs	50k $\times$ 4-input	44k $\times$ 6-input	332k $\times$ 6-input
DSP Slices	128	128	2760
BRAM	4 Mb	5 Mb	38 Mb
MGT	16 $\times$ 6.5 Gbps	16 $\times$ 6.5 Gbps	32 $\times$ 16.3 Gbps
CPU	PPC405	PPC440	-

- **No more hard-core CPU** $\rightarrow$ Slow control on MicroBlaze or light-weight option like IPbus
  - Belle II experience shows that Linux-based slow control adds a lot of complexity

CNCB v4.0: First Prototype



Two prototype boards were produced, then tested in Gießen and at IHEP

- No more power module, everything integrated on PCB

CNCB v4.0 Prototype Tests

	Gießen	IHEP
FPGA access	OK	OK
RAM	OK (16 GiB tested)	OK (2 GiB tested)
JTAG hub	OK (Carrier + AMCs)	OK (only Carrier tested)
PLL chip	OK	OK
Eth. switch	OK (Carrier, AMCs, backplane)	not tested
Flash chips	OK	not tested
Auto config.	OK	not tested
AMC links	OK (6.25 Gbps Aurora)	OK (12.5 Gbps loopback)
Backplane links	OK (3.125 Gbps Aurora)	OK (12.5 Gbps loopback)
IPMC interface	OK	not tested
Clock fan-out	not tested	OK
Linux on MB	OK	not tested

(IPMI functionality tested by Björn Spruck)

$\Rightarrow$ all essential functions tested successfully at at least one site

CNCB v4.0 Prototype Remaining Issues

- Main issue: **voltage drop** of several supply voltages, especially at high loads
  - 1.80 V $\rightarrow$ 1.69 V
  - 0.95 V $\rightarrow$ 0.91 V
  - Reason: DC/DC converters' remote-sense not correctly connected
  - Will be fixed in the next iteration
  - Compensated by manual adjustment $\rightarrow$ no noticeable impact
- Prototype was equipped with FPGA **speed grade** -1 instead of -2
  $\rightarrow$ MGT links tested at 12.5 Gbps instead of 16.3 Gbps
- The **MGT link to the RTM connector** (for 10G Ethernet) works only up to 3 Gbps (tested with loopback adapter at IHEP)
- DDR4 with the nominal memory clock (1000 MHz), but only **very slow R/W speeds** (~ 20 MB/s, MicroBlaze)
  $\rightarrow$ Should be tested with high R/W speeds, up to the hard limit of 16 GiB/s

Compute Node Upgrade: Rear-Transition Module (RTM)

- Two **RTM prototypes** have been produced
- Features:
  - On-board **USB-JTAG programmer** (Digilent)
  - **UART-USB interface** for 4 AMC cards + switch FPGA
  - **USB hub** for UART interfaces, IPMC
  - **SFP+ cage** for switch-FPGA 10G Ethernet

- Tests in Giessen and at IHEP revealed problems running the link at full speed.
- The eye diagram looks bad and the speed is limited to 3 Gbs
- This points to a layout problem in the PCB where the high speed signals have to pass a very crowded area near the DDR4 RAM
- Currently under investigation using PCB simulation tool HyperLynx
- Options include moving components on the PCB and/or adding more layers

Conclusions

- Prototypes of new CN carrier board under test
- Regular Skype meetings (every 2 weeks) between Giessen and IHEP
- Basic functionality of most components verified
- Various issues identified which will be fixed in the next iteration
- Problem with high speed link needs further investigation and (maybe) more significant change of PCB layout