Digital Signal Processing for the APFEL

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$\bar{\text{P}}$ANDA-Collaboration Meeting 18/3

November 2018

1. APFEL ASIC Feature Extraction
2. Integration of Feature Extraction into SADC
3. MAMI Beamtest with SADC

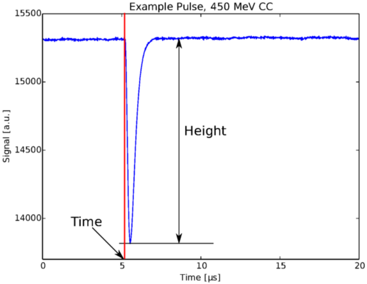
Digital Signal Processing

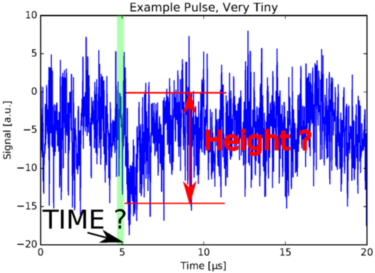
Properties

- Hit detection
- Time
- Energy (pulse height)

Requirements on Feature Extr.

- Fast (calculation time)
- Sensitive to ASIC pulse shape
- Linear
- Threshold as low as possible
- Dead time as short as possible





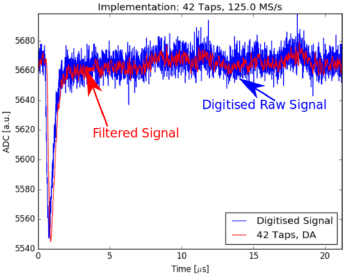
Digital Signal Processing

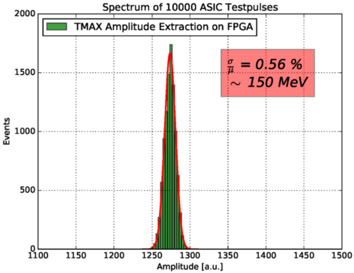
Filter

- Modification of transfer function
- Suppression of HF noise
- $\Rightarrow$ smoothing

Feature Extraction

- Determination of amplitude
- T_0 determination
- Pileup detection/correction





Filter (smoothing)

transfer function

output function

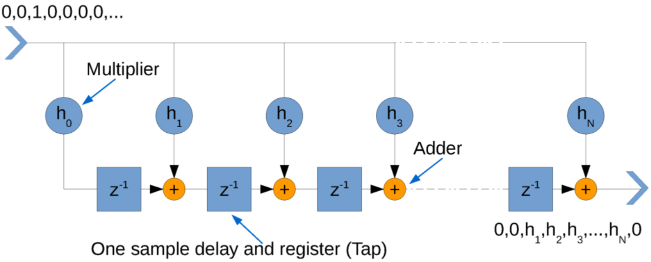
$$H(j\omega) = \frac{G(j\omega)}{F(j\omega)}$$

input function

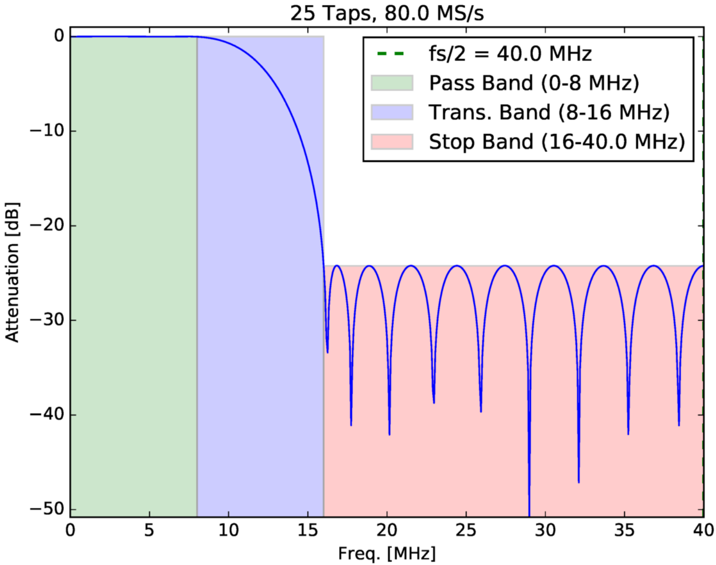
Smoothing via Finite Impulse Response (FIR) Filter

Idea

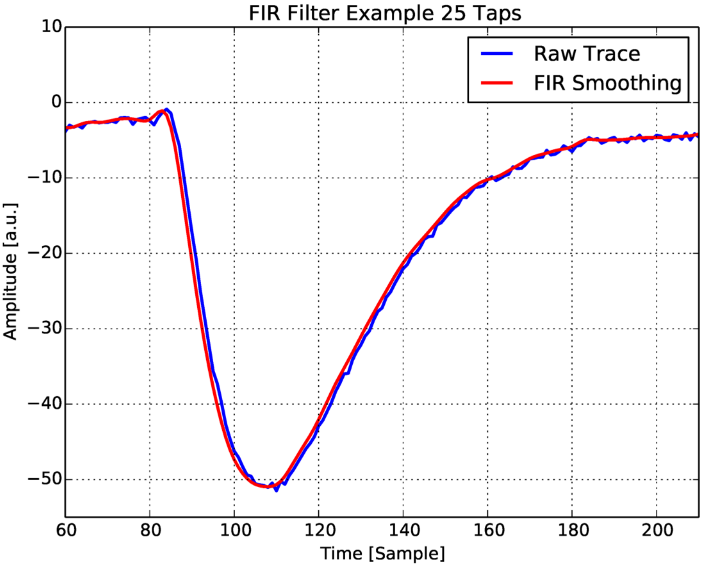
- Transfer function suppressed HF noise (low pass)
- Z transformation of impulse response
- $H(z) = \sum_{n=0}^{N} h(n) \cdot z^{-n}$
    - $h(n)$: Filter Koeffizienten
    - $z = e^{i\omega T}$
- Each output value is weighted sum of most recent input values
- $\textbf{out}[n] = h_0\textbf{in}[n] + h_1\textbf{in}[n-1] + ... + h_N\textbf{in}[n-N]$



Smoothing via Finite Impulse Response (FIR) Filter



Smoothing via Finite Impulse Response (FIR) Filter



Smoothing via Finite Impulse Response (FIR) Filter

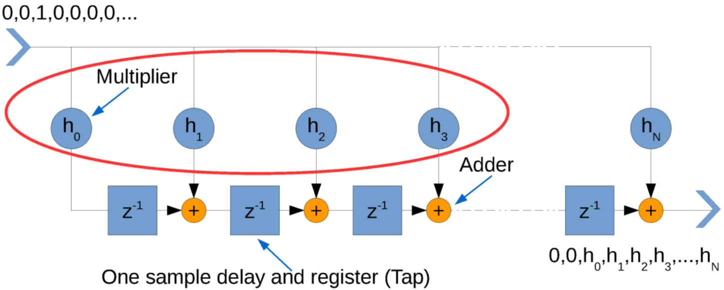
Benefits

- Reliable smoothing procedure (stable, no self-excitation)
- No pulse washout (pulse slope)
- Best way to increase signal/noise ratio

Drawback

- FIR filtering eats FPGA recourses

Smoothing via Finite Impulse Response (FIR) Filter



Implementation

- Efficient synthesis with Digital Signal Processing slices (DSP)
- ~1 DSP slices per tap, 25 taps · 32 channel 800 DSP slices
- 600 DSP slices on XC7K160T
- Need of resource saving implementation

Implementation with Distributed Arithmetic

Idea: Using Look Up Tables (LUT) instate of multiplication slices

$$y = \sum_{k=0}^{K} h_k \cdot x_k$$

$$x_k = \sum_{n=0}^{N} b_{kn} 2^n$$

$$\dots$$

$$y = \sum_{n=0}^{N} \left[\sum_{k=0}^{K} h_k \cdot b_{kn} \right] 2^n$$

Precalculated and stored in Look Up Tables (LUT)

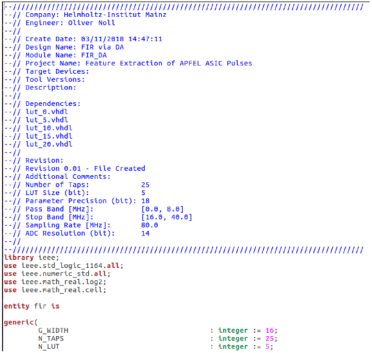
FIR with Distributed Arithmetic

VHDL Generator

- Software package which generates hardware description
- Free choose of parameters
    - Number of taps
    - Samplingrate
    - Pass-/stopband
    - Fix point resolution
    - ...

Hardware Simulation

- GHDL testbench
- Timing integrity



```
--/////////////////////////////////////////////////////////////////////////////
--// Company: Helmholtz-Institut Mainz
--// Engineer: Oliver Noll
--//
--// Create Date: 03/11/2018 14:47:11
--// Design Name: FIR via DA
--// Module Name: FIR_DA
--// Project Name: Feature Extraction of APFEL ASIC Pulses
--// Target Devices:
--// Tool Versions:
--// Description:
--//
--// Dependencies:
--// lut_0.vhdl
--// lut_5.vhdl
--// lut_10.vhdl
--// lut_15.vhdl
--// lut_20.vhdl
--//
--// Revision:
--// Revision 0.01 - File Created
--// Additional Comments:
--// Number of Taps:            25
--// LUT Size (bit):            5
--// Parameter Precision (bit): 18
--// Pass Band [MHz]:           [0.0, 8.0]
--// Stop Band [MHz]:           [16.0, 40.0]
--// Sampling Rate [MHz]:       80.0
--// ADC Resolution (bit):      14
--//
--/////////////////////////////////////////////////////////////////////////////
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
use ieee.math_real.log2;
use ieee.math_real.ceil;

entity fir is

generic(
        G_WIDTH                                   : integer := 16;
        N_TAPS                                    : integer := 25;
        N_LUT                                     : integer := 5;
```

Time Measurement and Amplitude EXtraction (TMAX)

TMAX Amplitude Path

- Sensitive to rising edge
- Cancels out falling edge
- No overshoot
- Baseline subtraction

Derivative:

$$D[i] = T[i + r] - T[i]$$

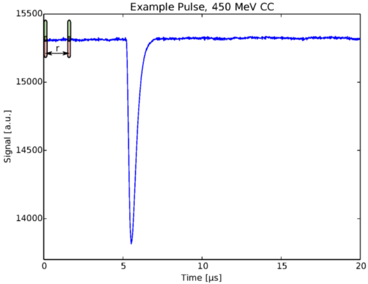
Heaviside function Θ:

$$x \mapsto \begin{cases} 0: & x < 0 \\ 1: & x \geq 0 \end{cases}$$

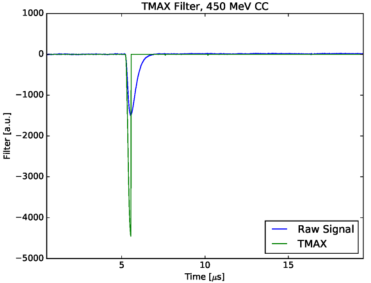
TMAX:

$$F_{TMAX} = \sum_{i=0}^{N} D[i] - \Theta[-D[i]] \cdot D[i]$$

Example Pulse, 450 MeV CC



TMAX Filter, 450 MeV CC



Time Measurement and Amplitude EXtraction (TMAX)

TMAX Time Path

- T_0 at maximum
- Linear interpolation between samples
- Implementation with LUT

Derivative:

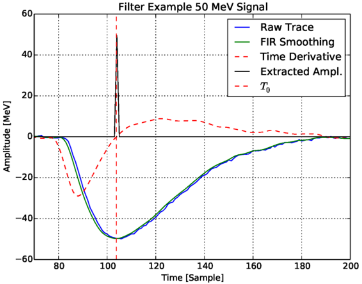
$D[i] = T[i + r] - T[i]$

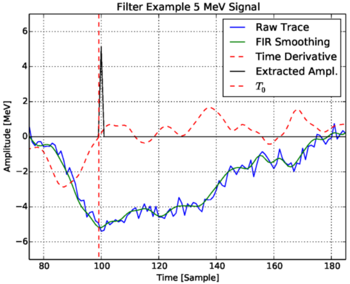
Time at change of sign:

i_0 and i_1

Linear Interpolation

$$T_0 = i_0 + \frac{D[i_0]}{D[i_0] - D[i_1]}$$

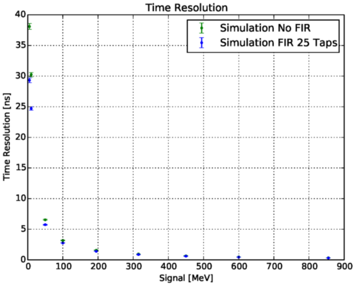


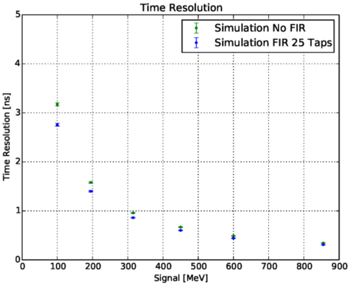


Time Measurement and Amplitude EXtraction (TMAX)

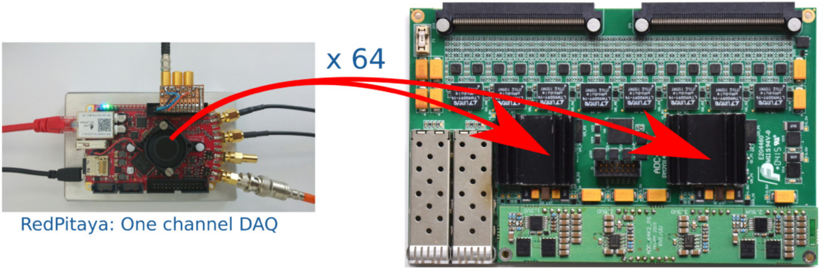
Is it worth all the effort?

- P̄ANDA operates triggerless
- FIR improves time resolution:
  better time resolution → better energy resolution





Integration of Feature Extraction into SADC

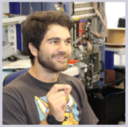


RedPitaya: One channel DAQ

PANDA SADC (P. Marciniewski): 64 channel

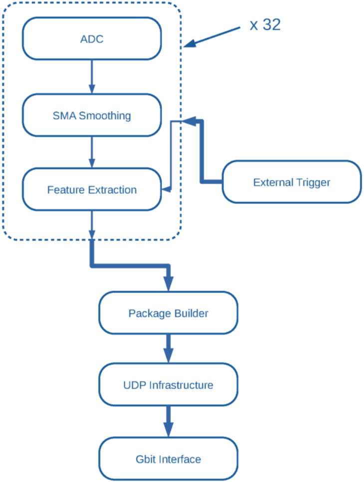
Integration of Feature Extraction into SADC

Bonn Firmware



Johannes Müllers
HISKP, Bonn

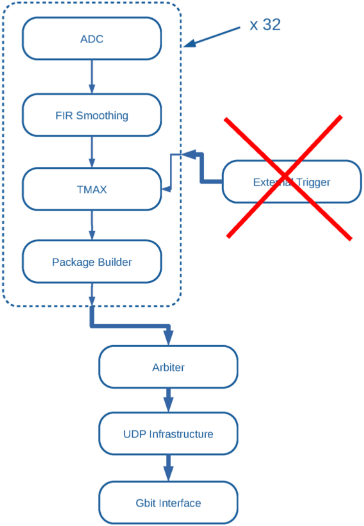
- Firmware for Crystal Barrel
- GitLab repository
- Meetings in Bonn
- Helping hand



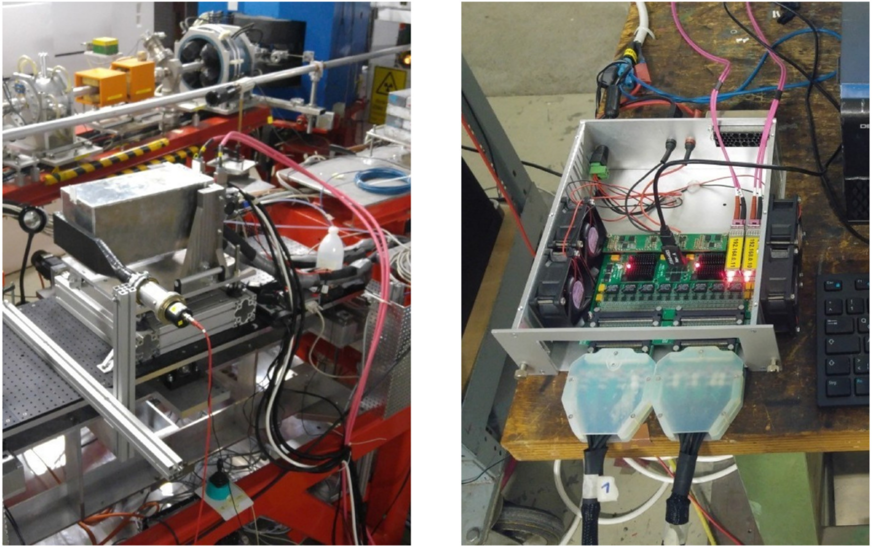
Integration of Feature Extraction into SADC

Mainz Firmware

- Using Bonn infrastructure
- Triggerless
- FIR filtering
- TMAX feature extraction
- New data package concept
- Full hardware simulation



MAMI Beamtest with SADC



MAMI Beamtest with SADC

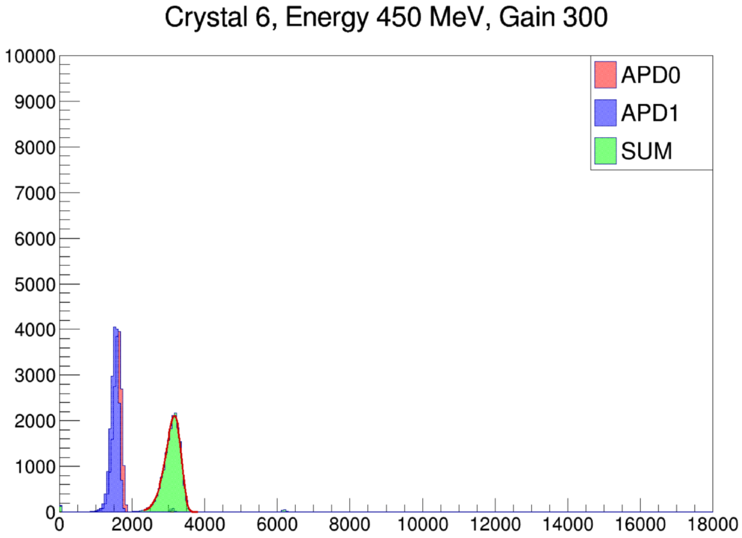
Setup

- PROTO16-2 (4x4)
- SADC with Mainz firmware
- Triggerless
- Reference scintillator

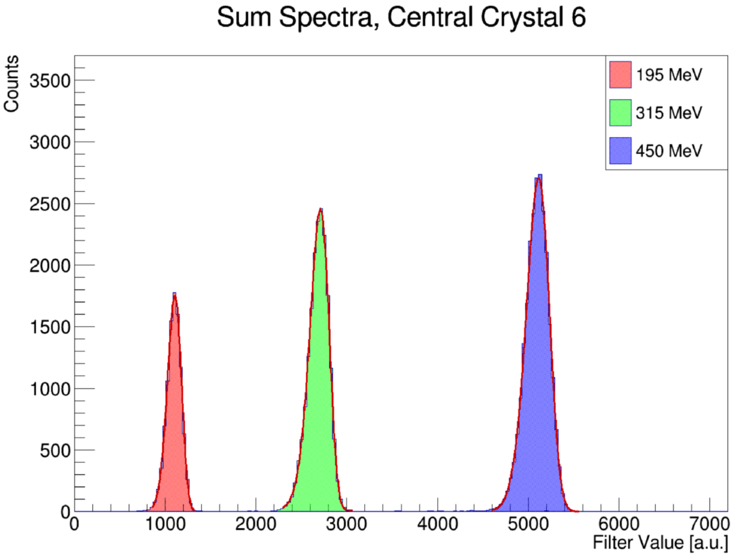
Measuring Program

- Energies: 195,450,855 MeV
- Different APD gains
- Central shot in every crystal
  - Linearity
  - Energy resolution
- Rate scan (up to 400 kHz)
- FIR tap scan

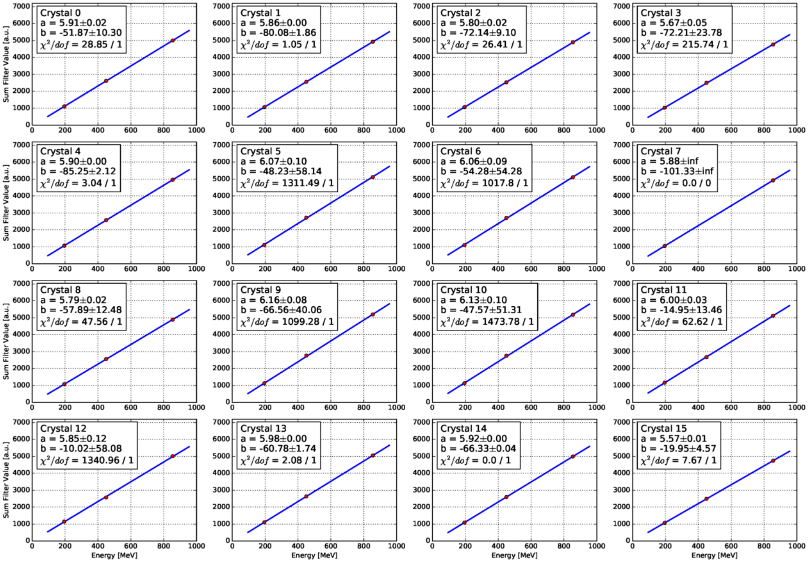
Single Spectra Example



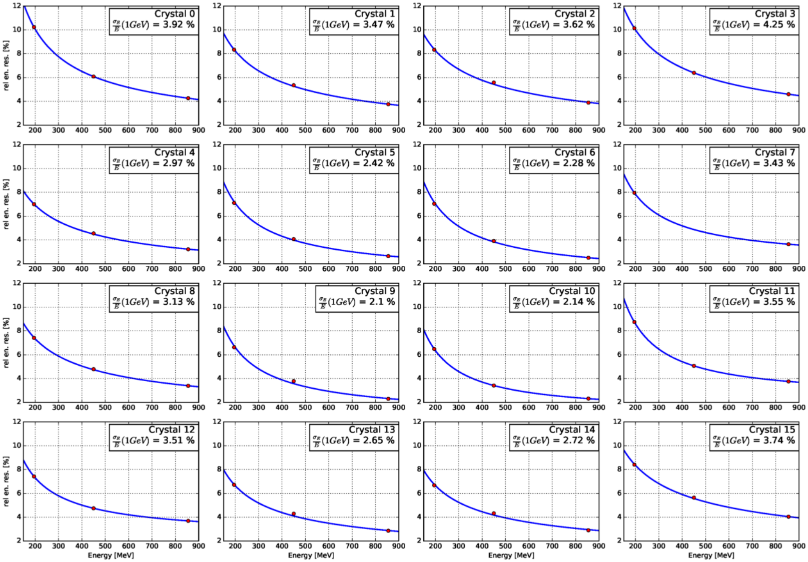
Sum Spectra Example



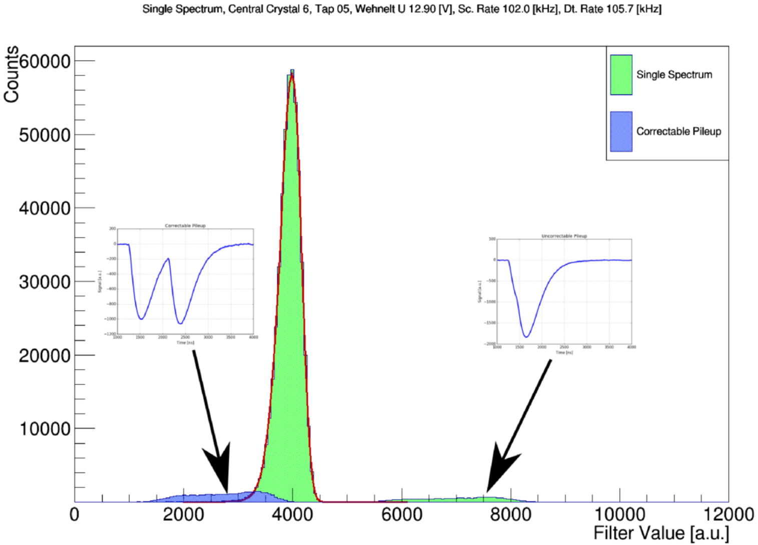
Linearity


Crystal 0
a = 5.91±0.02
b = -51.87±10.30
χ^2/dof = 28.85 / 1
Crystal 1
a = 5.86±0.00
b = -80.08±1.86
χ^2/dof = 1.05 / 1
Crystal 2
a = 5.80±0.02
b = -72.14±9.10
χ^2/dof = 26.41 / 1
Crystal 3
a = 5.67±0.05
b = -72.21±23.78
χ^2/dof = 215.74 / 1
Crystal 4
a = 5.90±0.00
b = -85.25±2.12
χ^2/dof = 3.04 / 1
Crystal 5
a = 6.07±0.10
b = -48.23±58.14
χ^2/dof = 1311.49 / 1
Crystal 6
a = 6.06±0.09
b = -54.28±54.28
χ^2/dof = 1017.8 / 1
Crystal 7
a = 5.88±inf
b = -101.33±inf
χ^2/dof = 0.0 / 0
Crystal 8
a = 5.79±0.02
b = -57.89±12.48
χ^2/dof = 47.56 / 1
Crystal 9
a = 6.16±0.08
b = -66.56±40.06
χ^2/dof = 1099.28 / 1
Crystal 10
a = 6.13±0.10
b = -47.57±51.31
χ^2/dof = 1473.78 / 1
Crystal 11
a = 6.00±0.03
b = -14.95±13.46
χ^2/dof = 62.62 / 1
Crystal 12
a = 5.85±0.12
b = -10.02±58.08
χ^2/dof = 1340.96 / 1
Crystal 13
a = 5.98±0.00
b = -60.78±1.74
χ^2/dof = 2.08 / 1
Crystal 14
a = 5.92±0.00
b = -66.33±0.04
χ^2/dof = 0.0 / 1
Crystal 15
a = 5.57±0.01
b = -19.95±4.57
χ^2/dof = 7.67 / 1
Sum Filter Value [a.u.]
0
1000
2000
3000
4000
5000
6000
7000
Energy [MeV]
0
200
400
600
800
1000

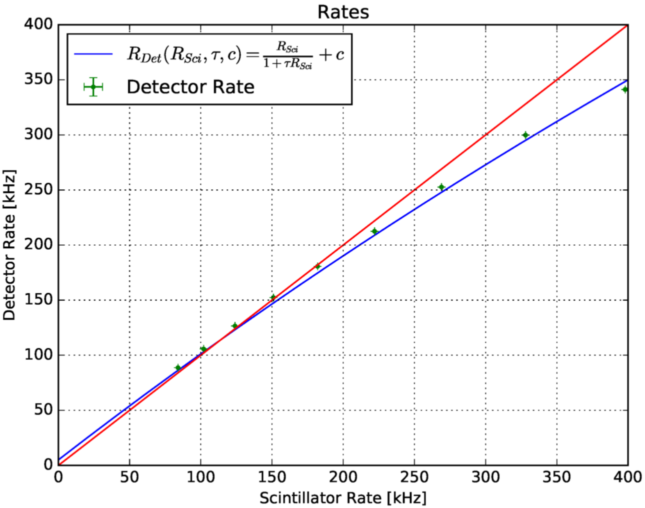
Relative Energy Resolution



Rate scan


Single Spectrum, Central Crystal 6, Tap 05, Wehnelt U 12.90 [V], Sc. Rate 102.0 [kHz], Dt. Rate 105.7 [kHz]
Counts
60000
50000
40000
30000
20000
10000
0
2000
4000
6000
8000
10000
12000
Filter Value [a.u.]
Single Spectrum
Correctable Pileup
Correctable Pileup
Signal [a.u.]
Time [ns]
Uncorrectable Pileup
Signal [a.u.]
Time [ns]

Rate scan



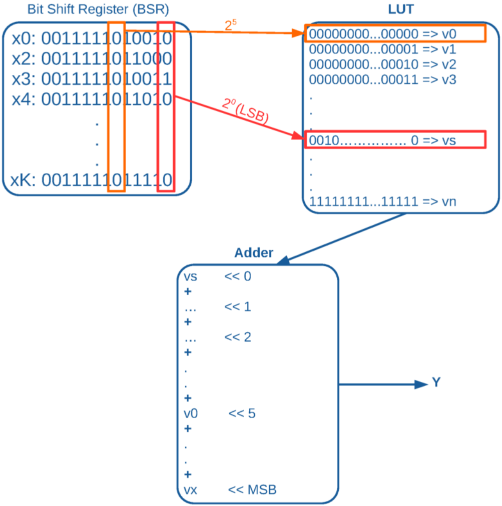
With $\tau = 400$ ns and c $=$ 5 kHz

Conclusion

- Development of APFEL feature extraction is finished
- Performance tested with hardware and software simulations
- First implementation into SADC
- Successful beamtest at MAMI

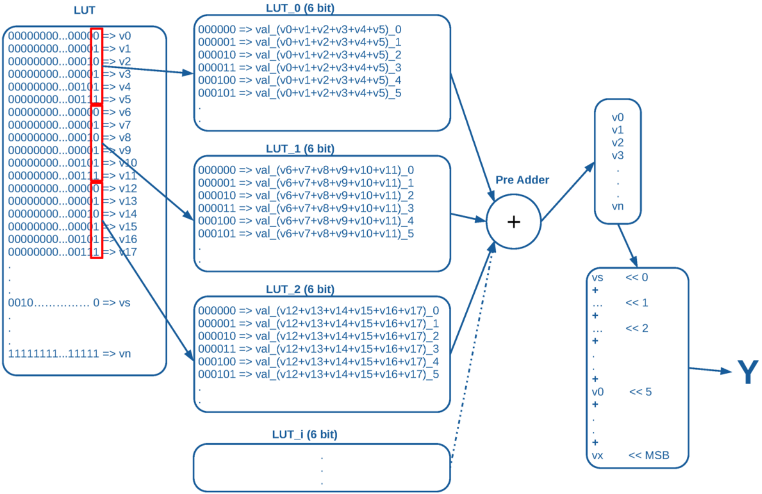
Backup

FIR with Distributed Arithmetic



$$y = \sum_{n=0}^{N} \left[\sum_{k=0}^{K} h_k \cdot b_{kn} \right] 2^n$$

FIR with Distributed Arithmetic



LUT

00000000...00000 => v0
00000000...00001 => v1
00000000...00010 => v2
00000000...00001 => v3
00000000...00101 => v4
00000000...00111 => v5
00000000...00000 => v6
00000000...00001 => v7
00000000...00010 => v8
00000000...00001 => v9
00000000...00101 => v10
00000000...00111 => v11
00000000...00000 => v12
00000000...00001 => v13
00000000...00010 => v14
00000000...00001 => v15
00000000...00101 => v16
00000000...00111 => v17
.
.
.
0010............... 0 => vs
.
.
.
11111111...11111 => vn

LUT_0 (6 bit)

000000 => val_(v0+v1+v2+v3+v4+v5)_0
000001 => val_(v0+v1+v2+v3+v4+v5)_1
000010 => val_(v0+v1+v2+v3+v4+v5)_2
000011 => val_(v0+v1+v2+v3+v4+v5)_3
000100 => val_(v0+v1+v2+v3+v4+v5)_4
000101 => val_(v0+v1+v2+v3+v4+v5)_5
.
.

LUT_1 (6 bit)

000000 => val_(v6+v7+v8+v9+v10+v11)_0
000001 => val_(v6+v7+v8+v9+v10+v11)_1
000010 => val_(v6+v7+v8+v9+v10+v11)_2
000011 => val_(v6+v7+v8+v9+v10+v11)_3
000100 => val_(v6+v7+v8+v9+v10+v11)_4
000101 => val_(v6+v7+v8+v9+v10+v11)_5
.
.

LUT_2 (6 bit)

000000 => val_(v12+v13+v14+v15+v16+v17)_0
000001 => val_(v12+v13+v14+v15+v16+v17)_1
000010 => val_(v12+v13+v14+v15+v16+v17)_2
000011 => val_(v12+v13+v14+v15+v16+v17)_3
000100 => val_(v12+v13+v14+v15+v16+v17)_4
000101 => val_(v12+v13+v14+v15+v16+v17)_5
.
.

LUT_i (6 bit)

.
.
.

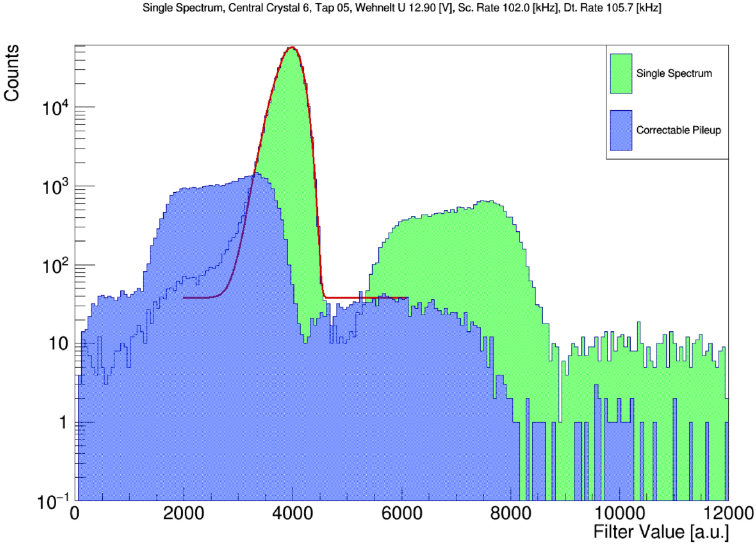
Pre Adder

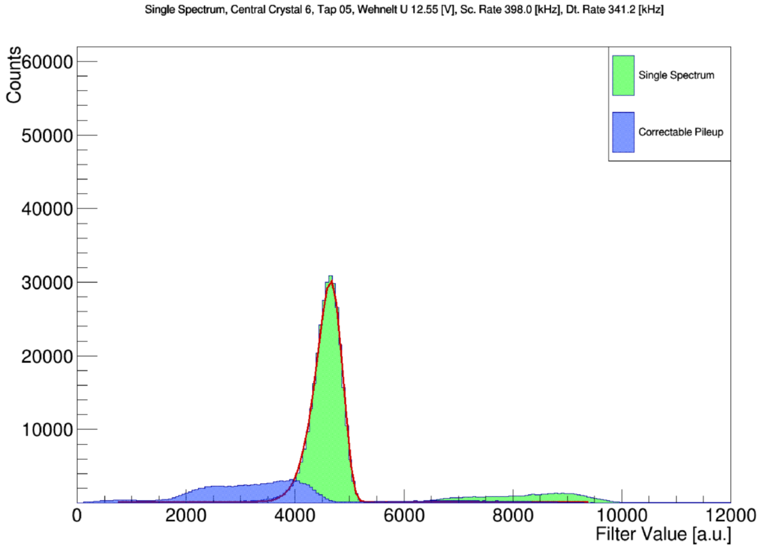
+

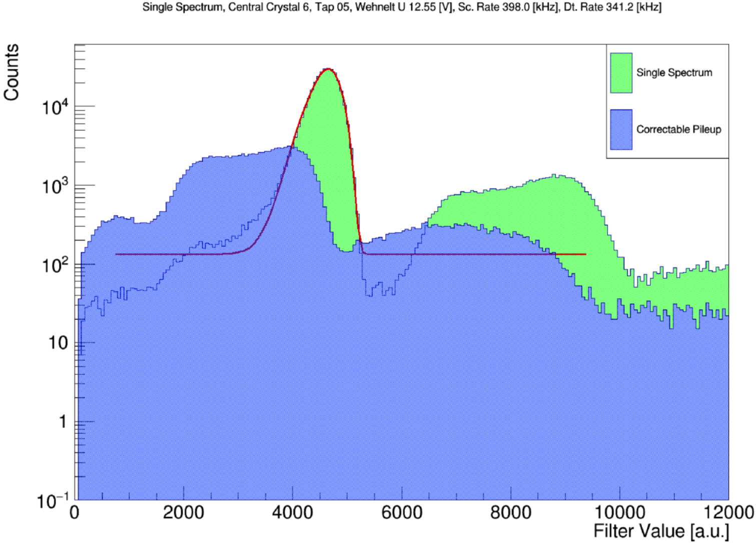
v0
v1
v2
v3
.
.
.
vn

vs << 0
+
... << 1
+
... << 2
+
.
.
+
v0 << 5
+
.
.
+
vx << MSB

Y


Single Spectrum, Central Crystal 6, Tap 05, Wehnelt U 12.90 [V], Sc. Rate 102.0 [kHz], Dt. Rate 105.7 [kHz]
Counts
10^4
10^3
10^2
10
1
10^{-1}
0
2000
4000
6000
8000
10000
12000
Filter Value [a.u.]
Single Spectrum
Correctable Pileup


Single Spectrum, Central Crystal 6, Tap 05, Wehnelt U 12.55 [V], Sc. Rate 398.0 [kHz], Dt. Rate 341.2 [kHz]
Counts
60000
50000
40000
30000
20000
10000
0
2000
4000
6000
8000
10000
12000
Filter Value [a.u.]
🟩 Single Spectrum
🟦 Correctable Pileup


Single Spectrum, Central Crystal 6, Tap 05, Wehnelt U 12.55 [V], Sc. Rate 398.0 [kHz], Dt. Rate 341.2 [kHz]
Counts
10^4
10^3
10^2
10
1
10^{-1}
0
2000
4000
6000
8000
10000
12000
Filter Value [a.u.]
Single Spectrum
Correctable Pileup