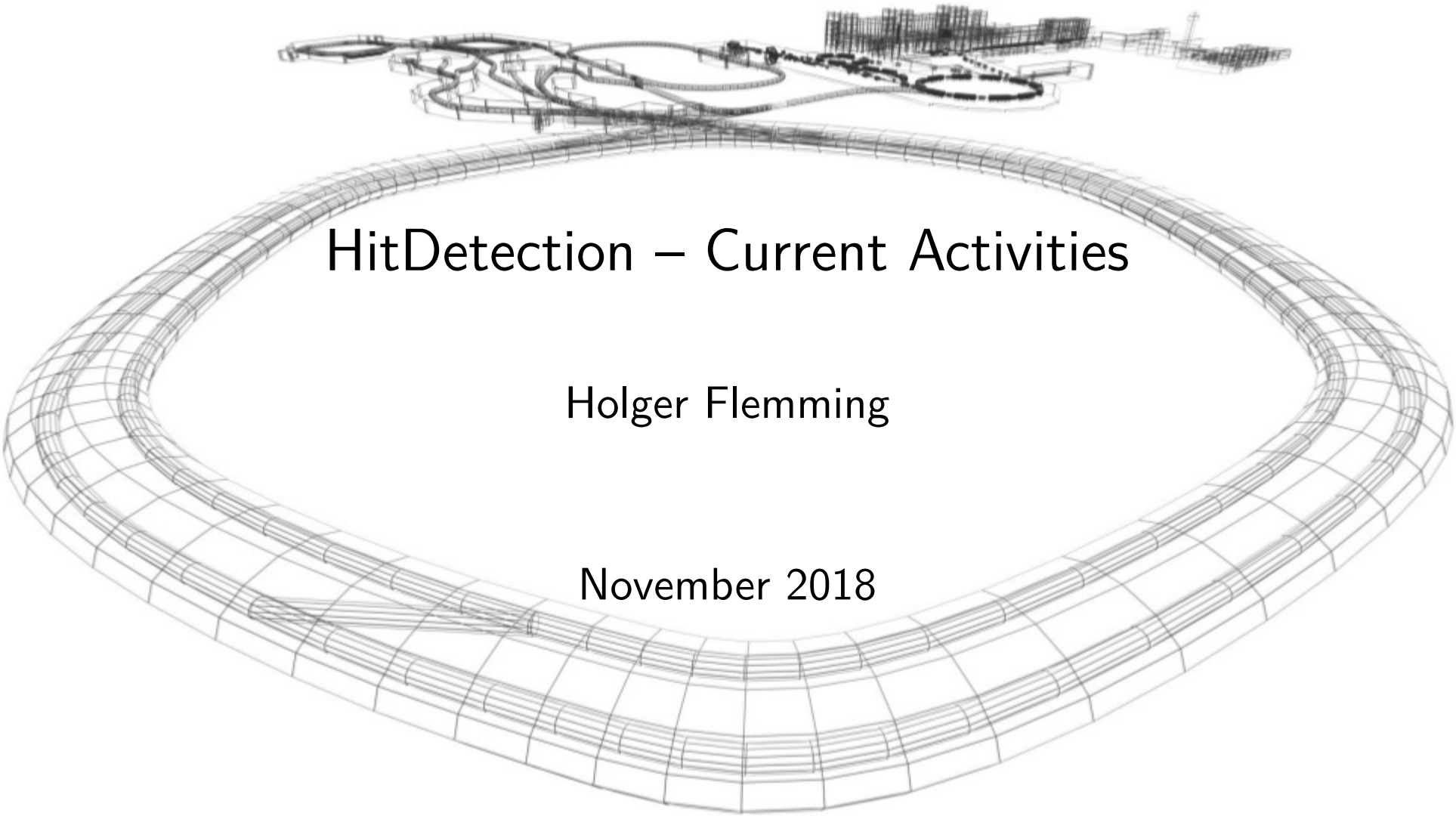


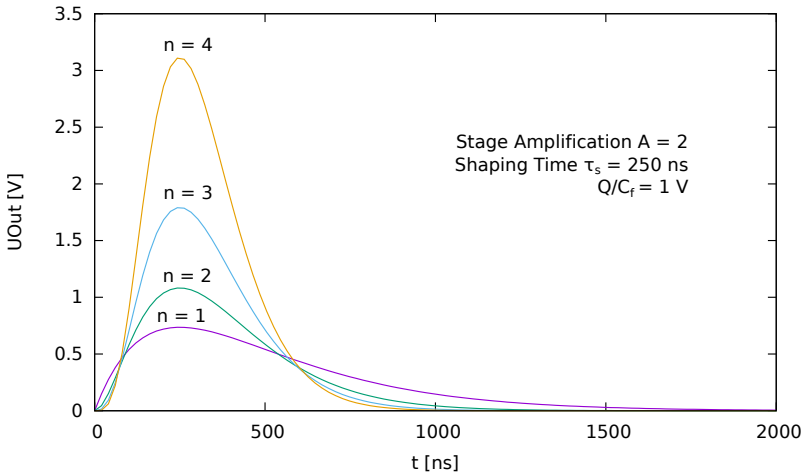
HitDetection – Current Activities

Holger Flemming

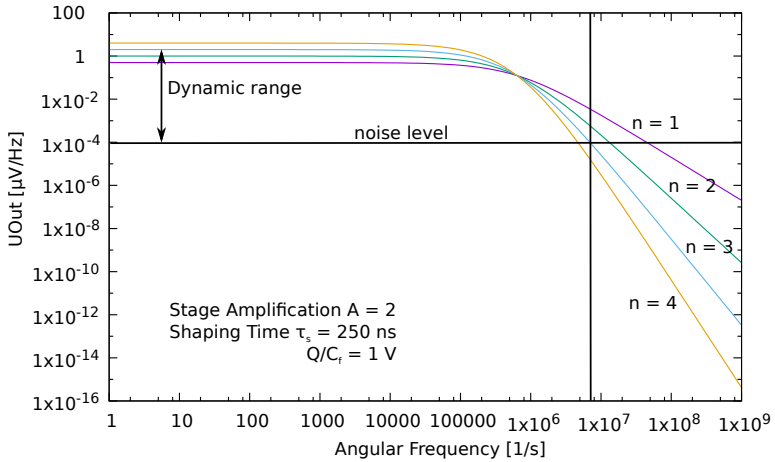
November 2018

Outline

In May FEE workshop: Motivation of Analogue transients parameter:



PASA output signal



PASA output spectrum

- 99.9 % of signal in the spectrum below 3.17 MHz
  ⇒ Sampling frequency: 8 MS/s
  ⇒ 8 samples to cover full pulse
  ⇒ 16 sample traces

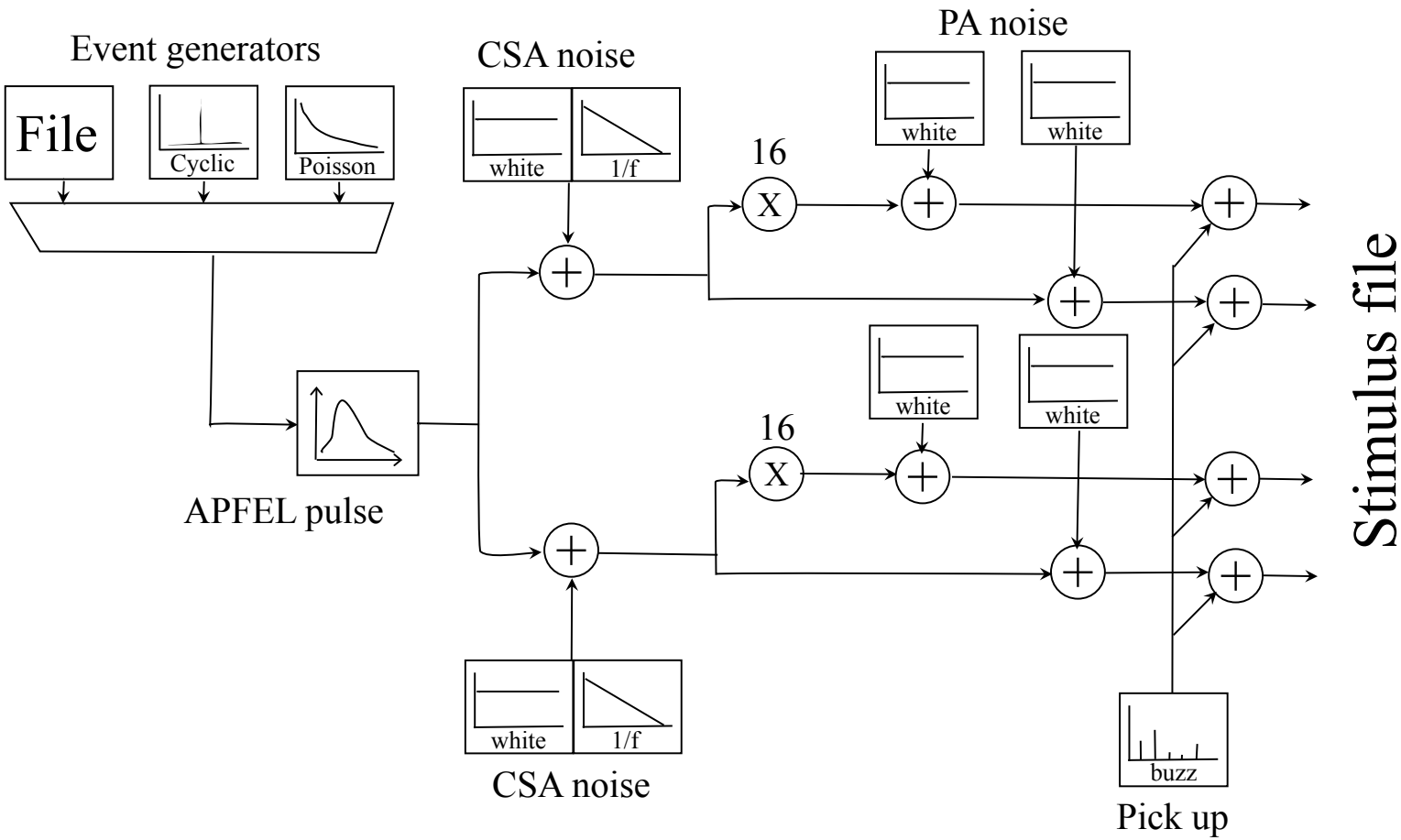
Are theses traces really sufficient for feature extraction?

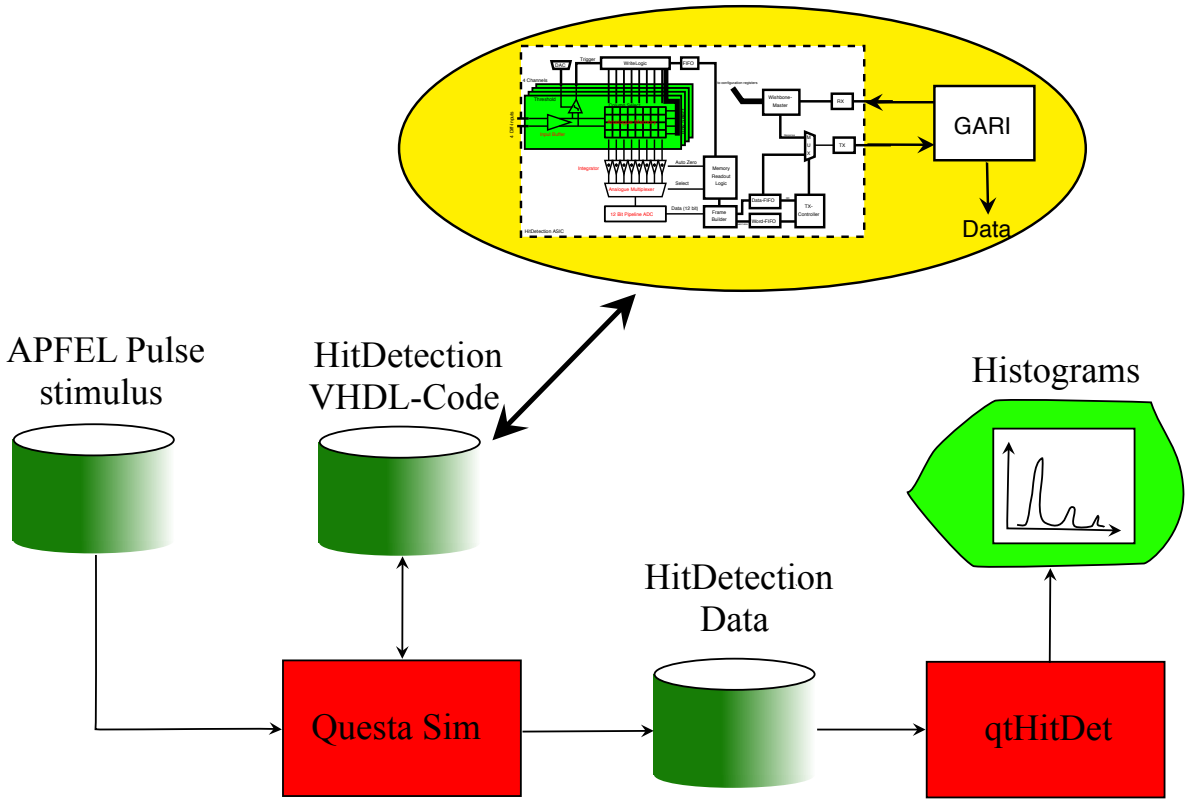
Different algorithms for time and amplitude extraction have been tested
As the latest HitDetection prototype ASIC has a bug in digital readout simulated HitDetection data was used

- Time
  - Zero crossing of derivation
- Amplitude
  - Maximum value
  - Integral
  - Window integral
  - Parabolic interpolation
  - Linear regression of transient and standardised pulse shape

Stimulus generator

- Generating noisy APFEL pulses for Full Chip Simulation

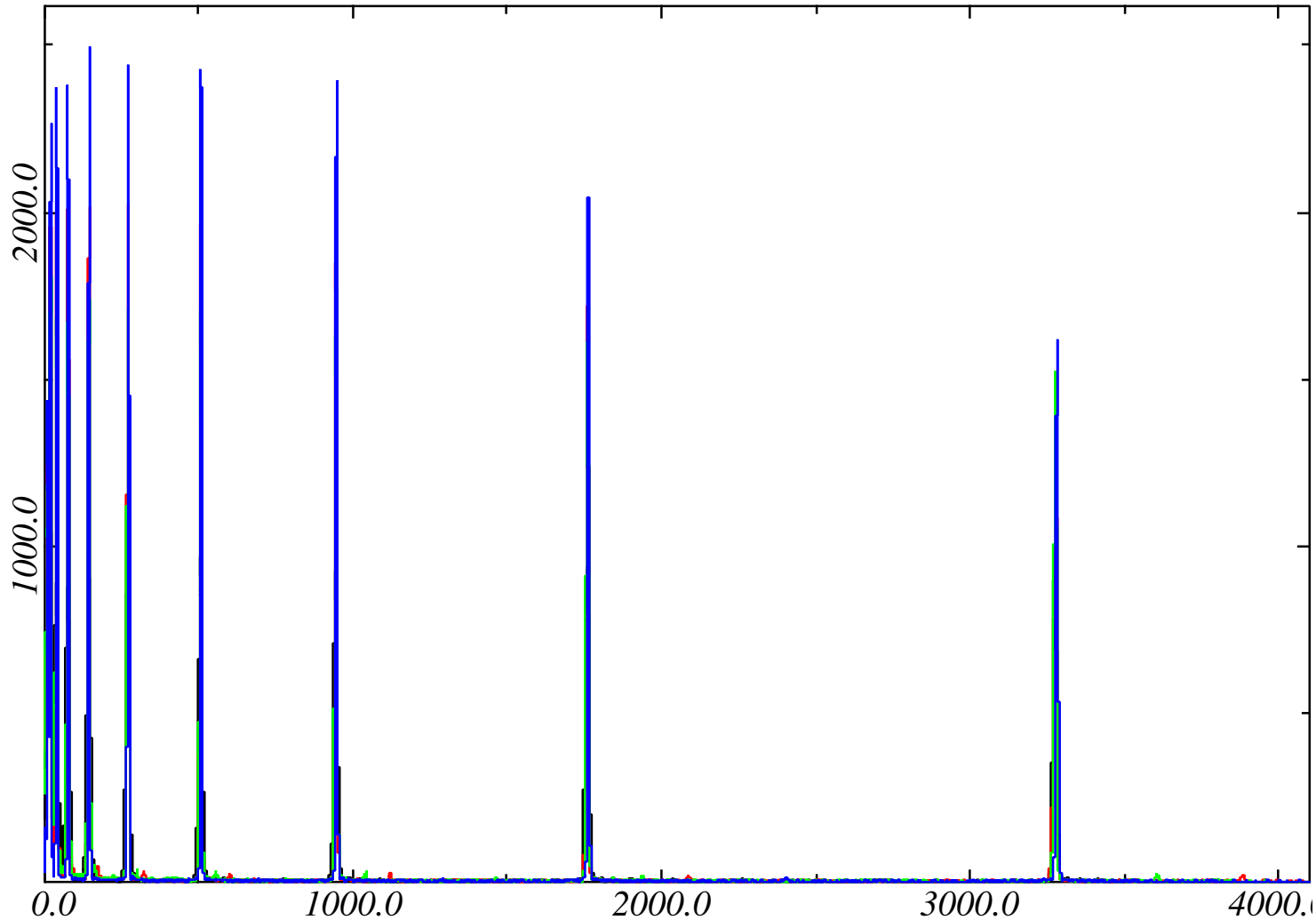




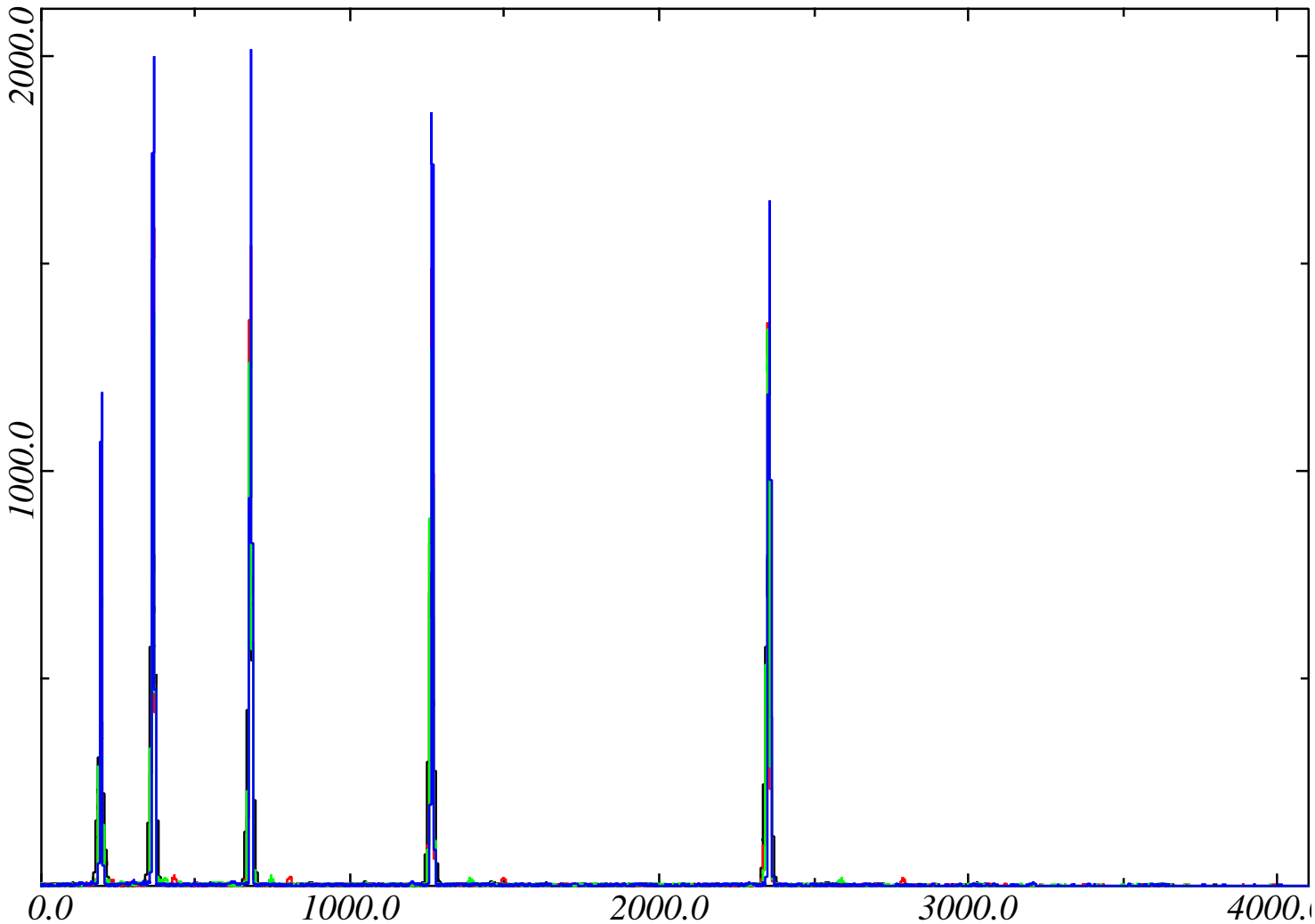
- Feeding Stimulus data info QuestaSim simulation of HitDetection VHDL code
- HitDetection data output is written into file
- Data is analysed with described feature extraction algorithms

- Poisson distributed pulses, 50 kHz rate
- 10 discrete amplitudes 6 mV ... 1.6 V
- Logarithmic steps
- CSA white noise: 0.1 mV / 0.5 mV
- No CSA 1/f noise
- PA white noise: 2 mV / 5 mV
- No Pick up / 20 mV 50 Hz + 5 mV 100 Hz

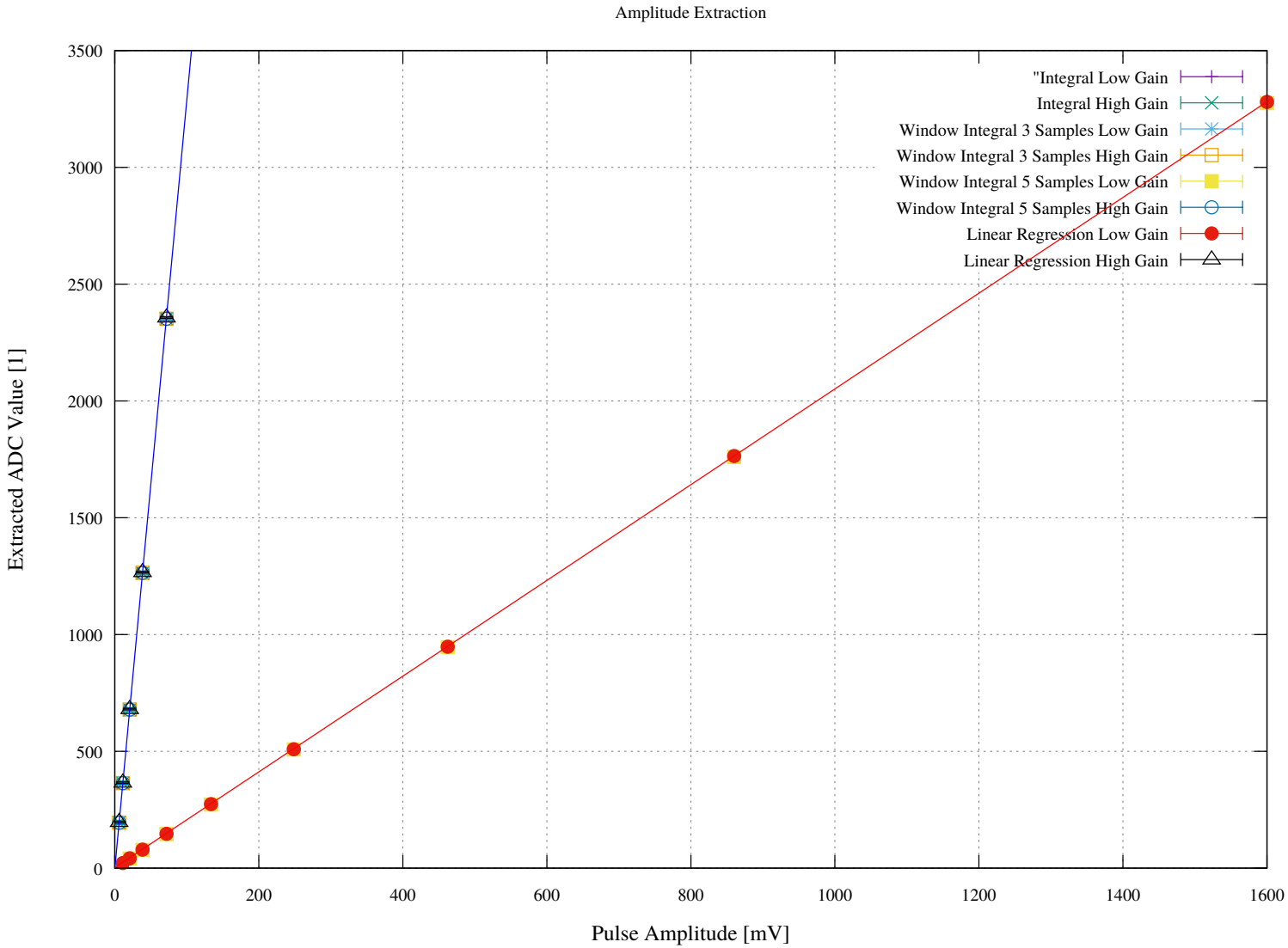
Low Gain Amplitude Spectrum



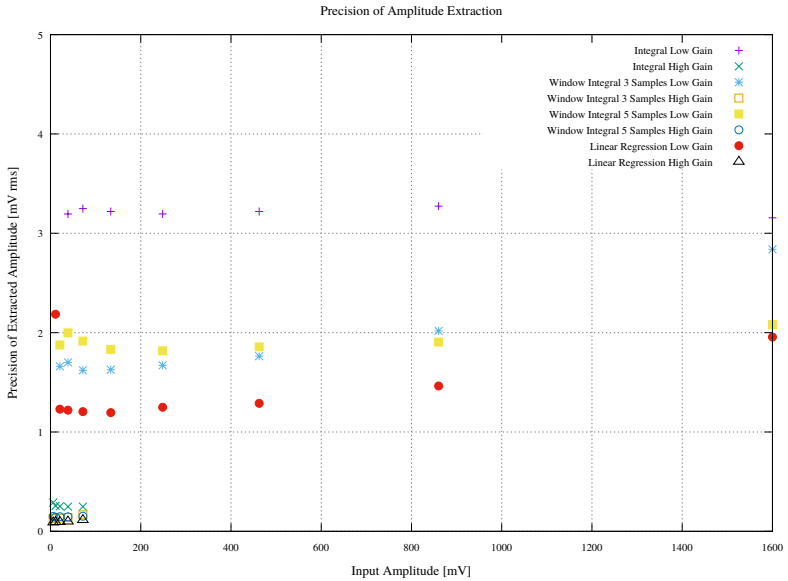
High Gain Amplitude Spectrum



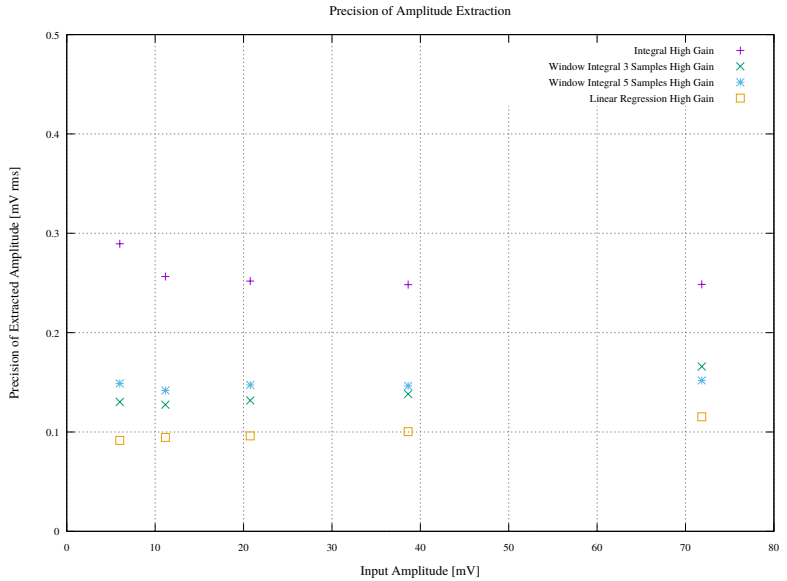
Amplitude Extraction



Precision of Amplitude Extraction



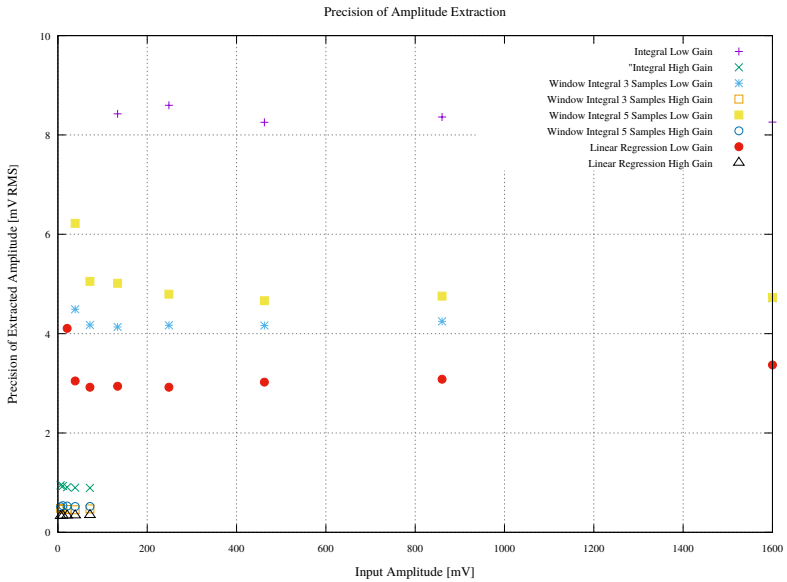
Low and high gain



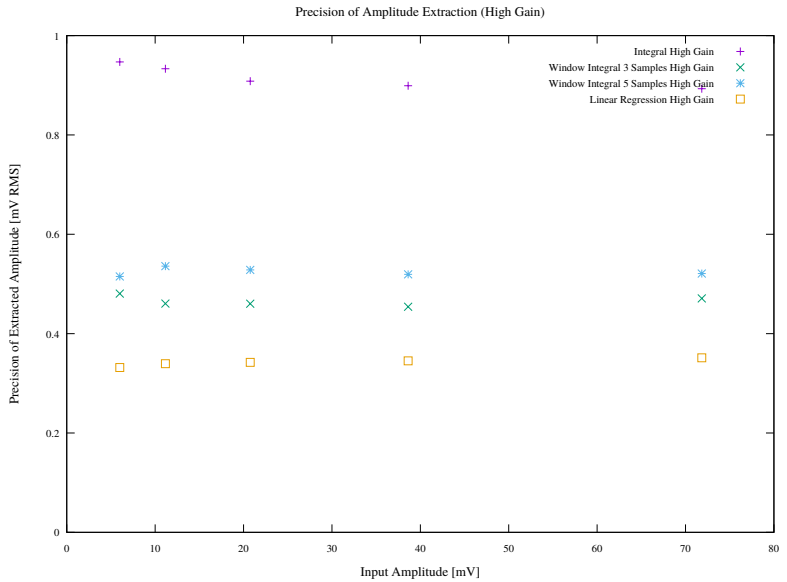
High gain

- CSA white noise: 0.1 mV
- No CSA 1/f noise
- PA white noise: 2 mV
- No Pick up

Precision of Amplitude Extraction



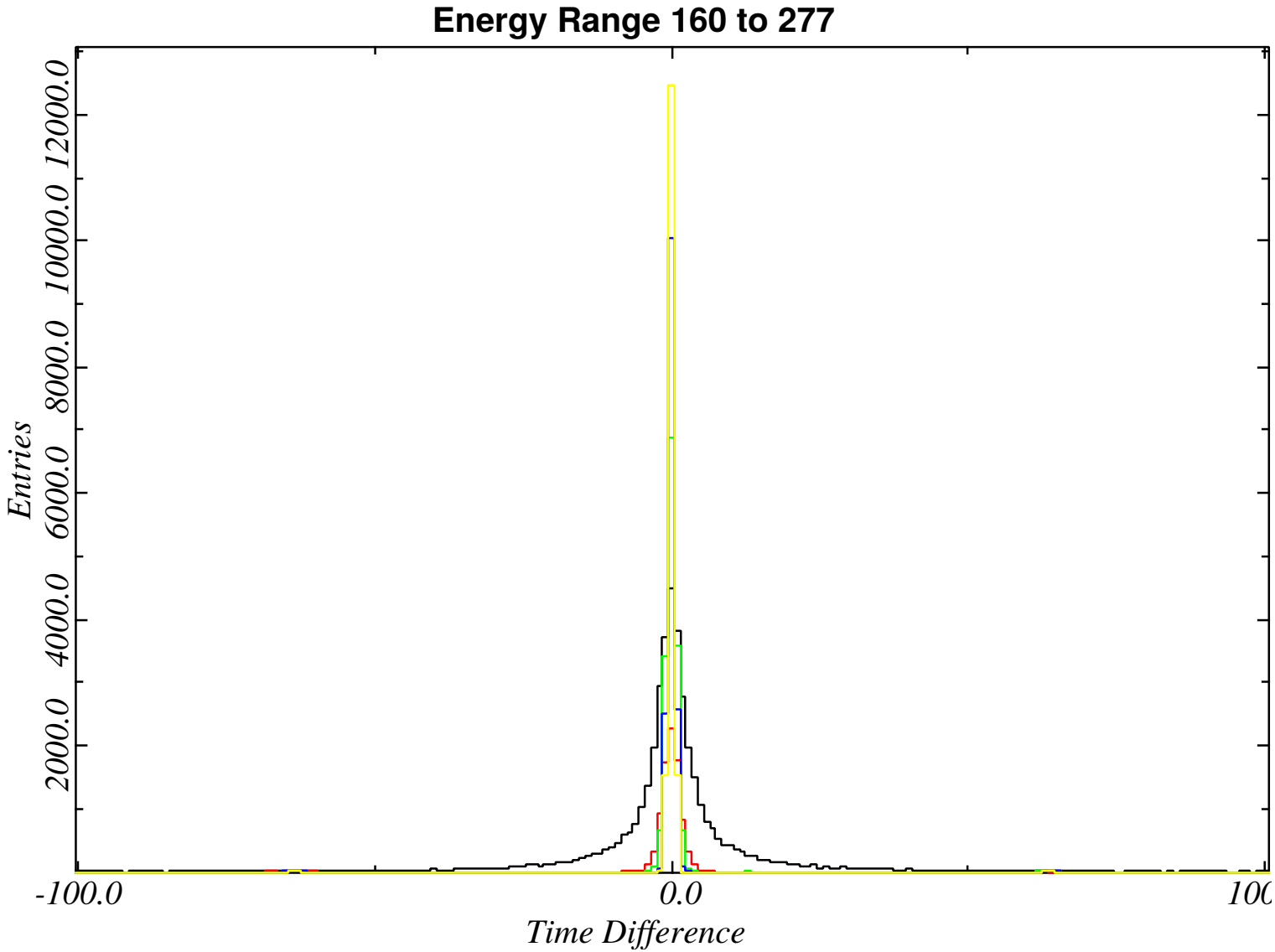
Low and high gain



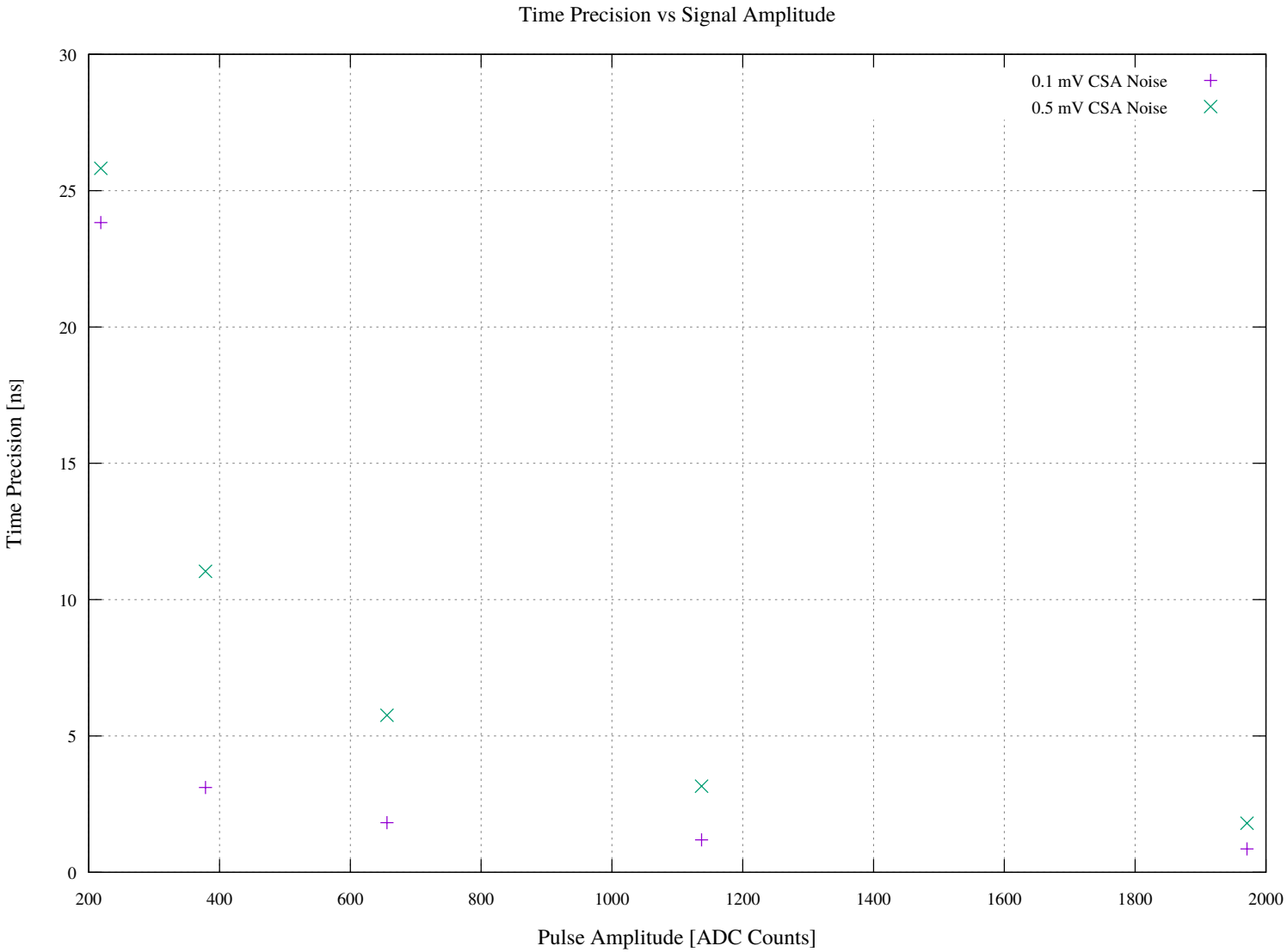
High gain

- CSA white noise: 0.5 mV
- No CSA 1/f noise
- PA white noise: 5 mV
- Pick up: 20 mV 50 Hz + 5 mV 100 Hz

Time Extraction



Precision of Time Extraction

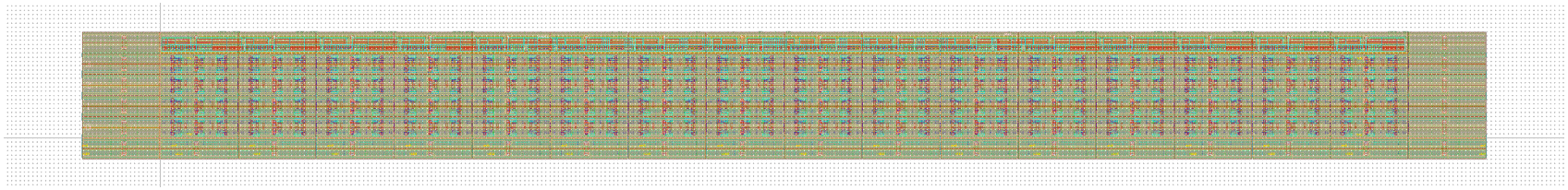


Outline

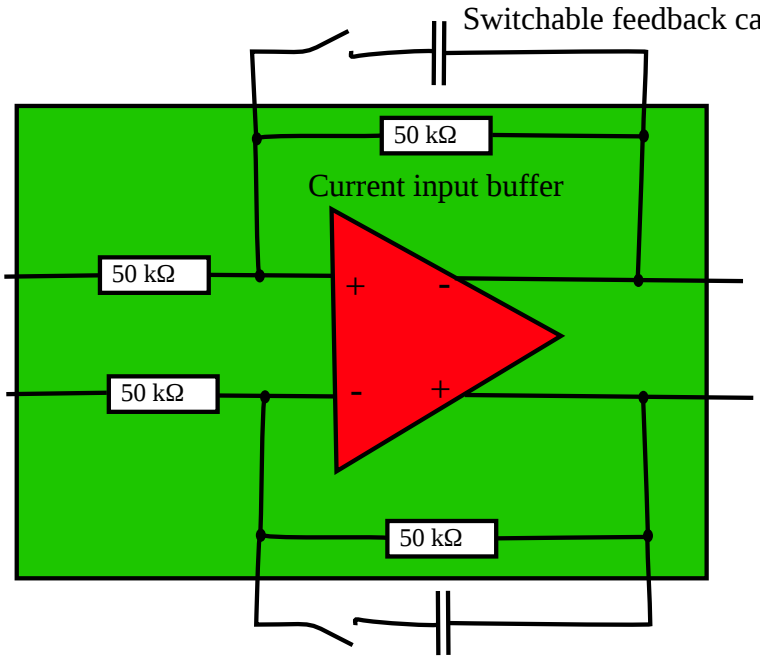
Chip design activities towards a 16 channel prototype for barrel readout are ongoing

- Scaling analogue memory
- Input buffer and discriminator
- Floor planning

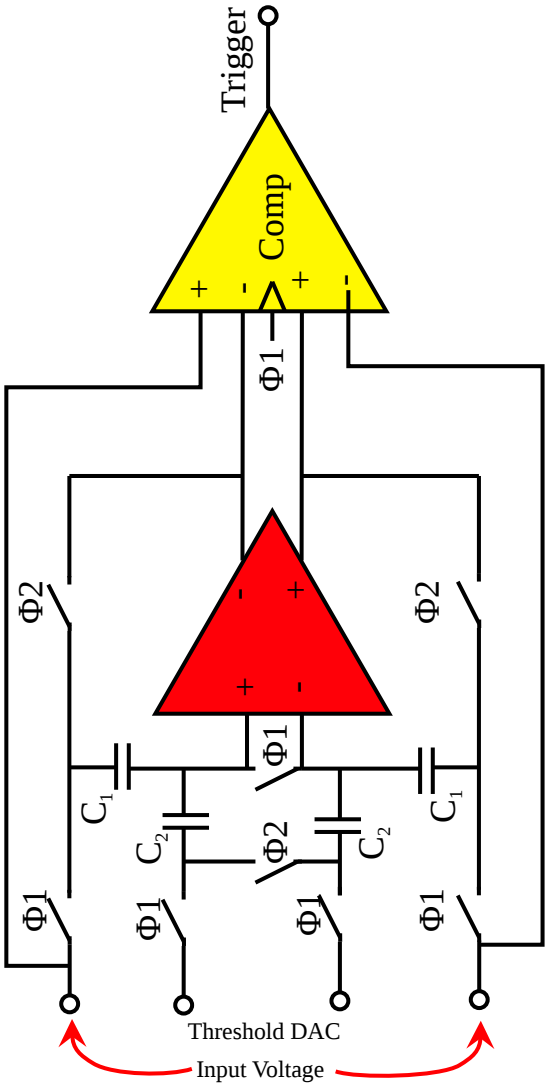
Analogue Memory Scaling



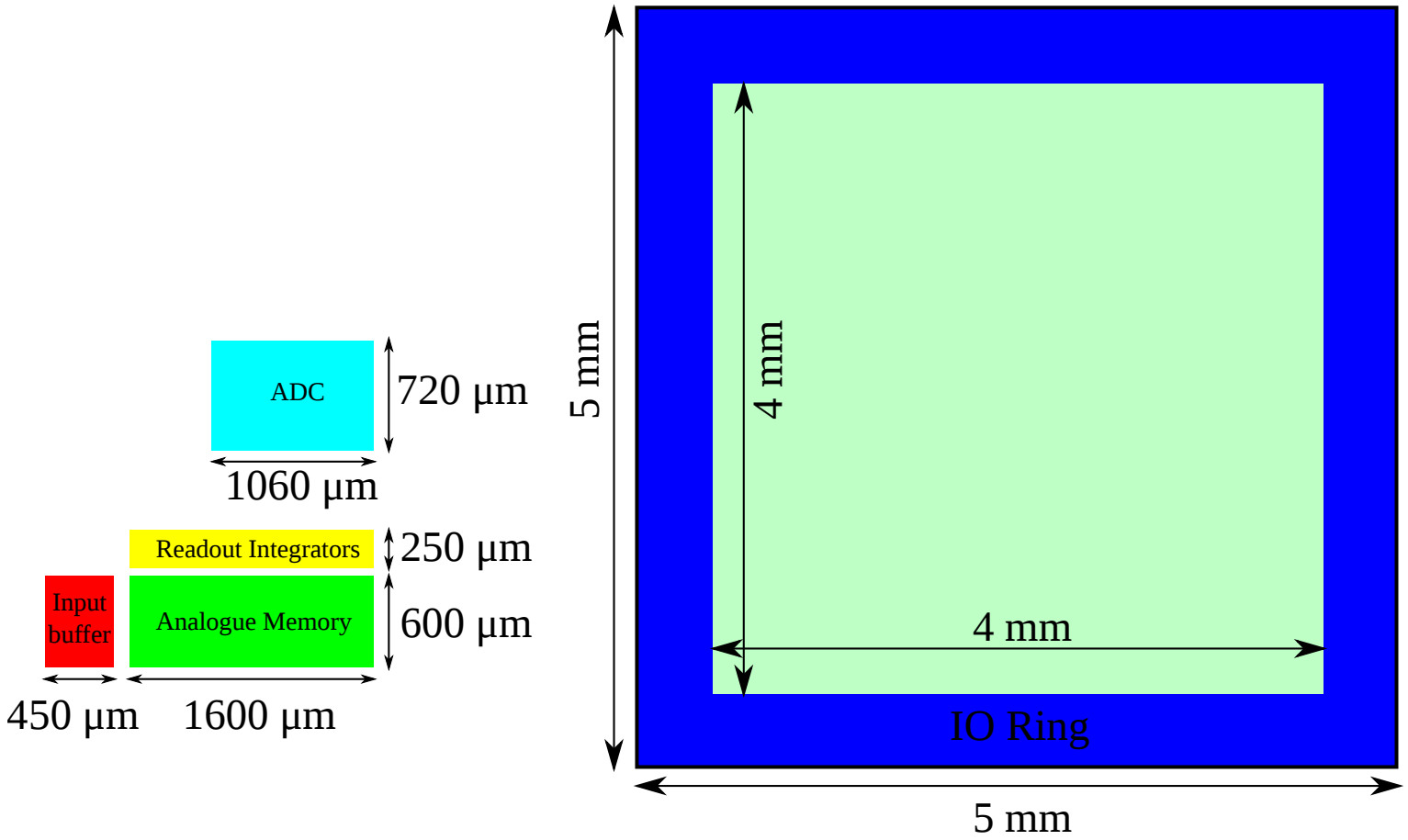
- Current analogue memory has four rows per channel with 8 columns
- Number of columns is increased to 16
- Schematic and layout design is finished
- Currently owing:
  - Simulation of parasitic extraction
  - Matching with read out integrators



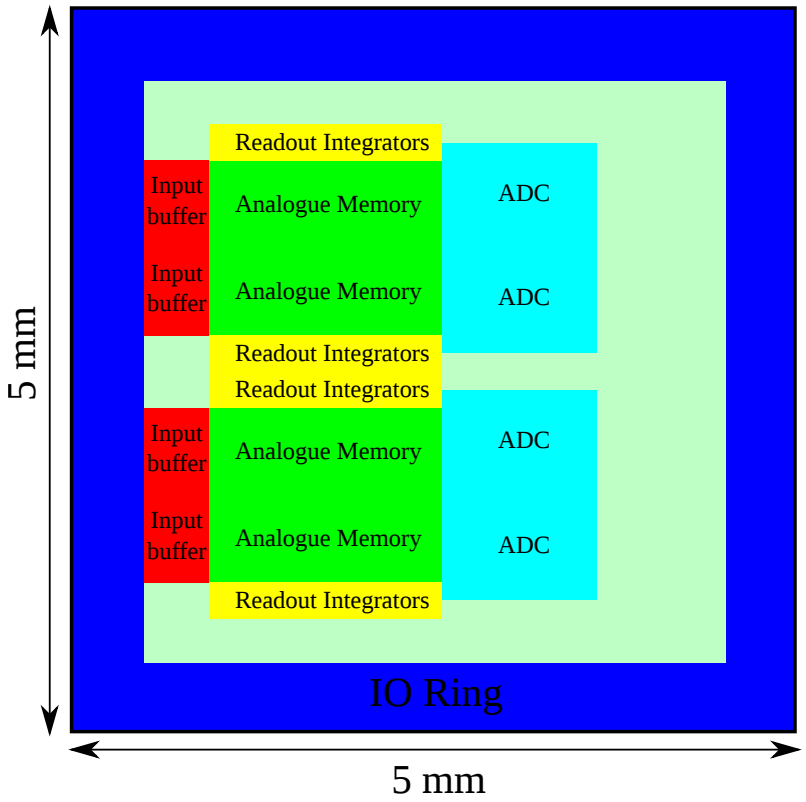
- Fully differential, gain 1
- 100 kΩ differential input resistor
- $>$ 50 MHz bandwidth
- Possible modification:
  - Low pass characteristic by switchable feedback capacitances
  - Anti aliasing
  - Suppression of high frequency pick-up
  - Noise reduction
  - First simulations very promising



- Φ_1
  - Storing input voltage in C_1
  - Storing threshold Voltage in C_2
- Φ_2
  - Switching C_1 into feedback
  - Transferring charge from C_2 to C_1
  - Output voltage: $U_{in} - C_2/C_1 U_{thres}$
  - Used as comparator threshold
- Leading edge of Φ_1
  - Taking comparator decision $U_{in}(t) > U_{in}(t-\Delta t) - \frac{C_2}{C_1} U_{Thres}$ $\Rightarrow \frac{\Delta U_{in}}{\Delta t} < \frac{C_2}{C_1} U_{Thres}$



- For MPW prototype runs the design has to fit into 5 by 5 mm^2 blocks
- approx. 15 kEuro / block



- 9.58 mm^2 for full custom blocks will fit into 1 $5 \times 5\ \mathrm{mm}^2$ block
- 6.42 mm^2 for power routing and digital logic Sufficient area??

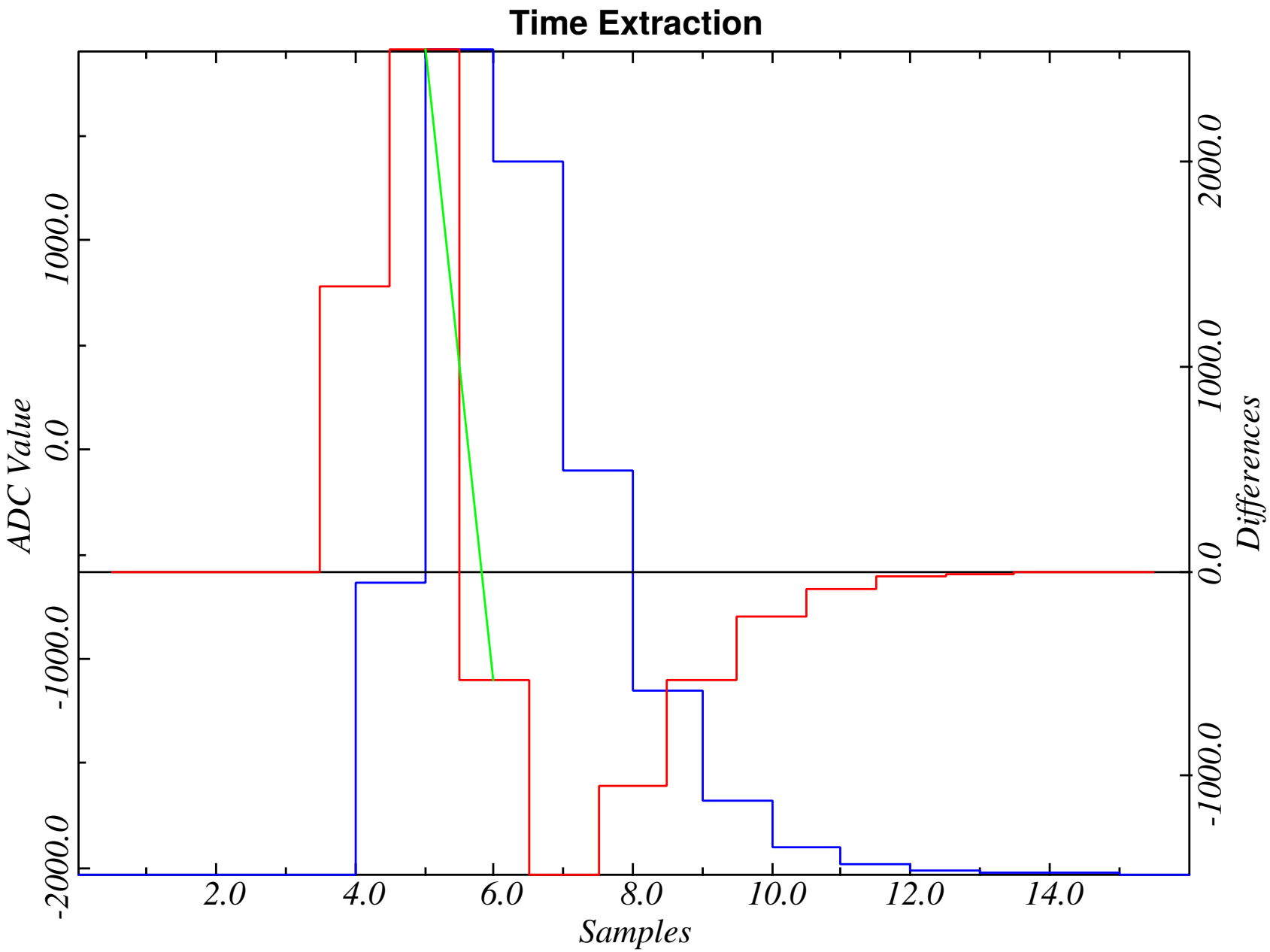
Outline

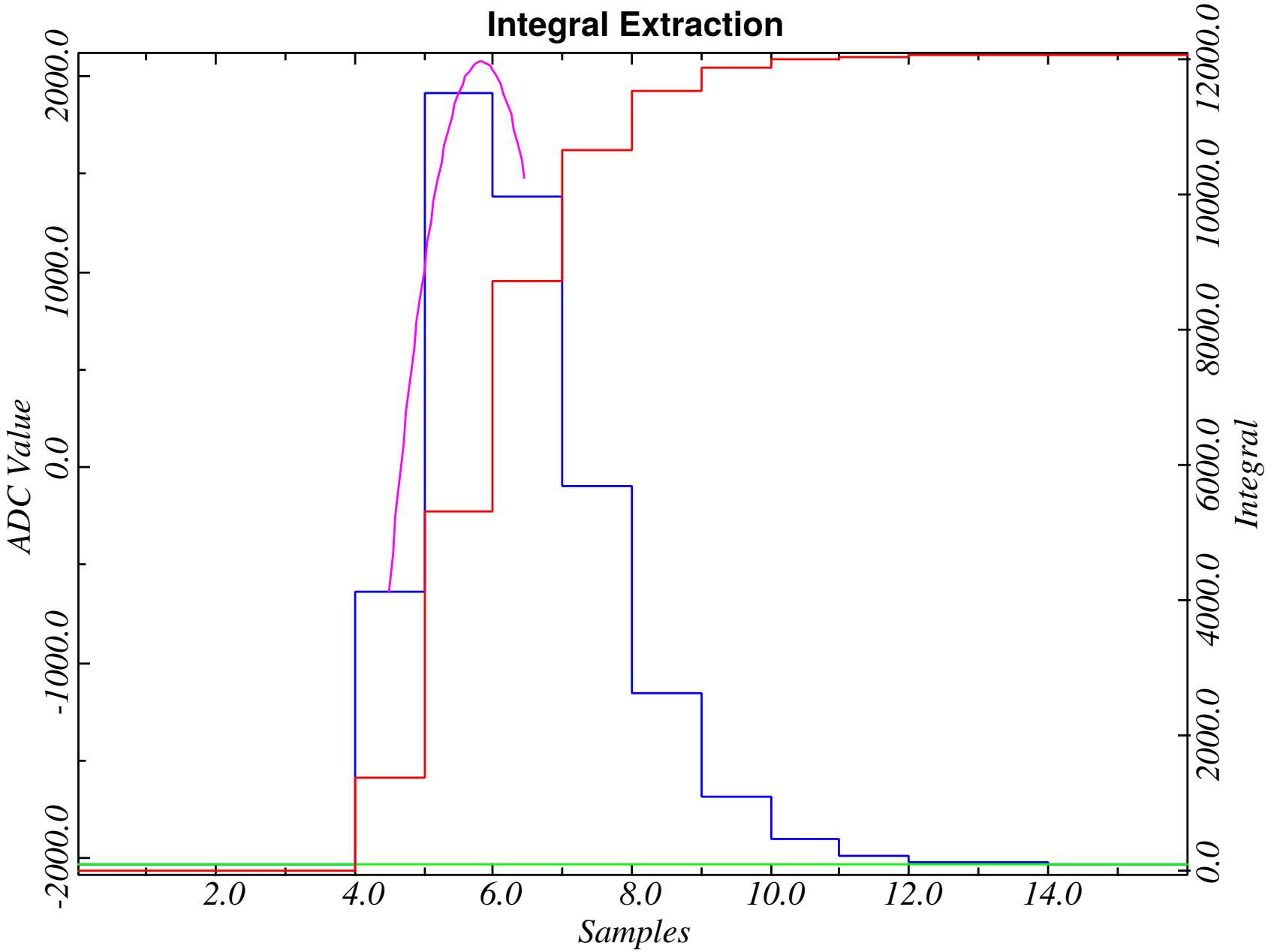
Summary and Outlook

- Different feature extraction algorithms have been tested with simulated HitDetection data
- Time as well as amplitude extraction works very well
- Extraction quality depends on numerical effort
- High quality feature extraction from 16 sample traces is feasable!
- Analyses have to be checked with measured data. Corrected HitDetection prototype is expected this month.
- Design work towards a 16 channel prototype for barrel readout is ongoing

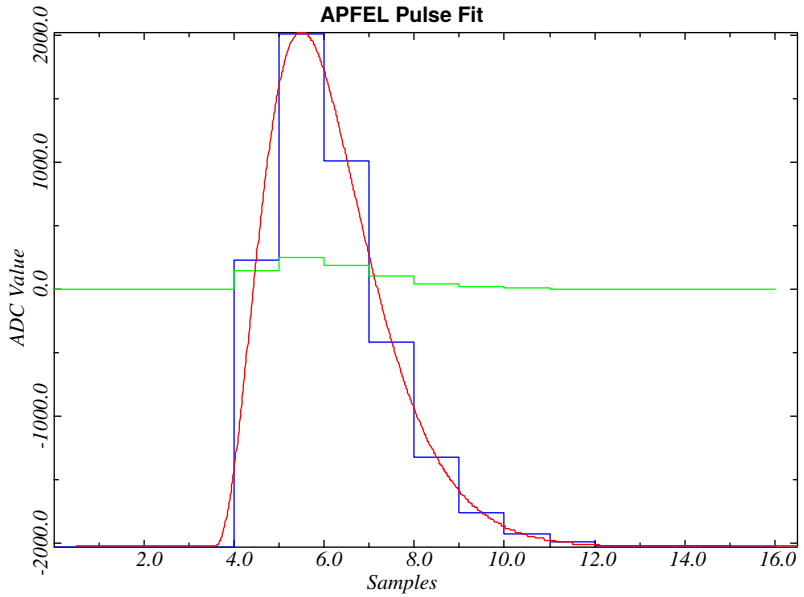
Thank you for your attention

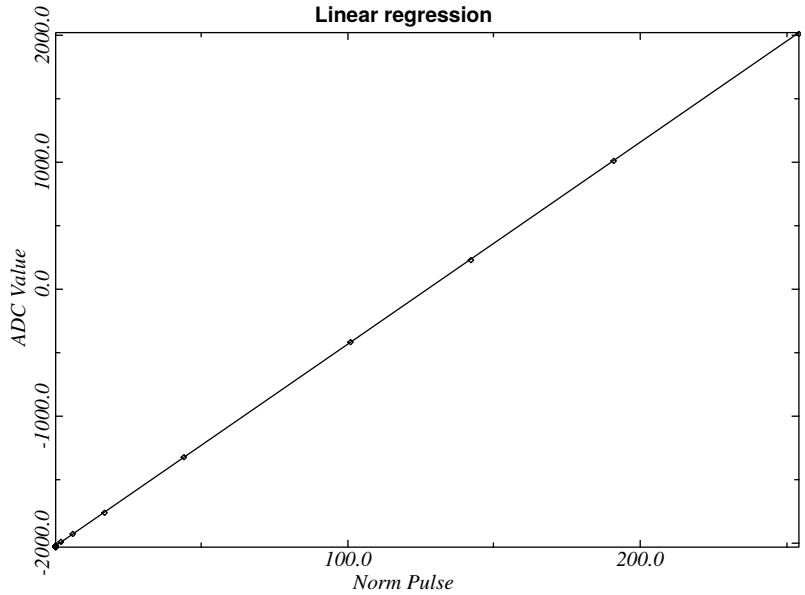
Backup


Time Extraction
ADC Value
Differences
Samples
2000.0
1000.0
0.0
-1000.0
-2000.0
2.0
4.0
6.0
8.0
10.0
12.0
14.0


Integral Extraction
ADC Value
Integral
Samples
2000.0
1000.0
0.0
-1000.0
-2000.0
12000.0
10000.0
8000.0
6000.0
4000.0
2000.0
0.0
2.0
4.0
6.0
8.0
10.0
12.0
14.0

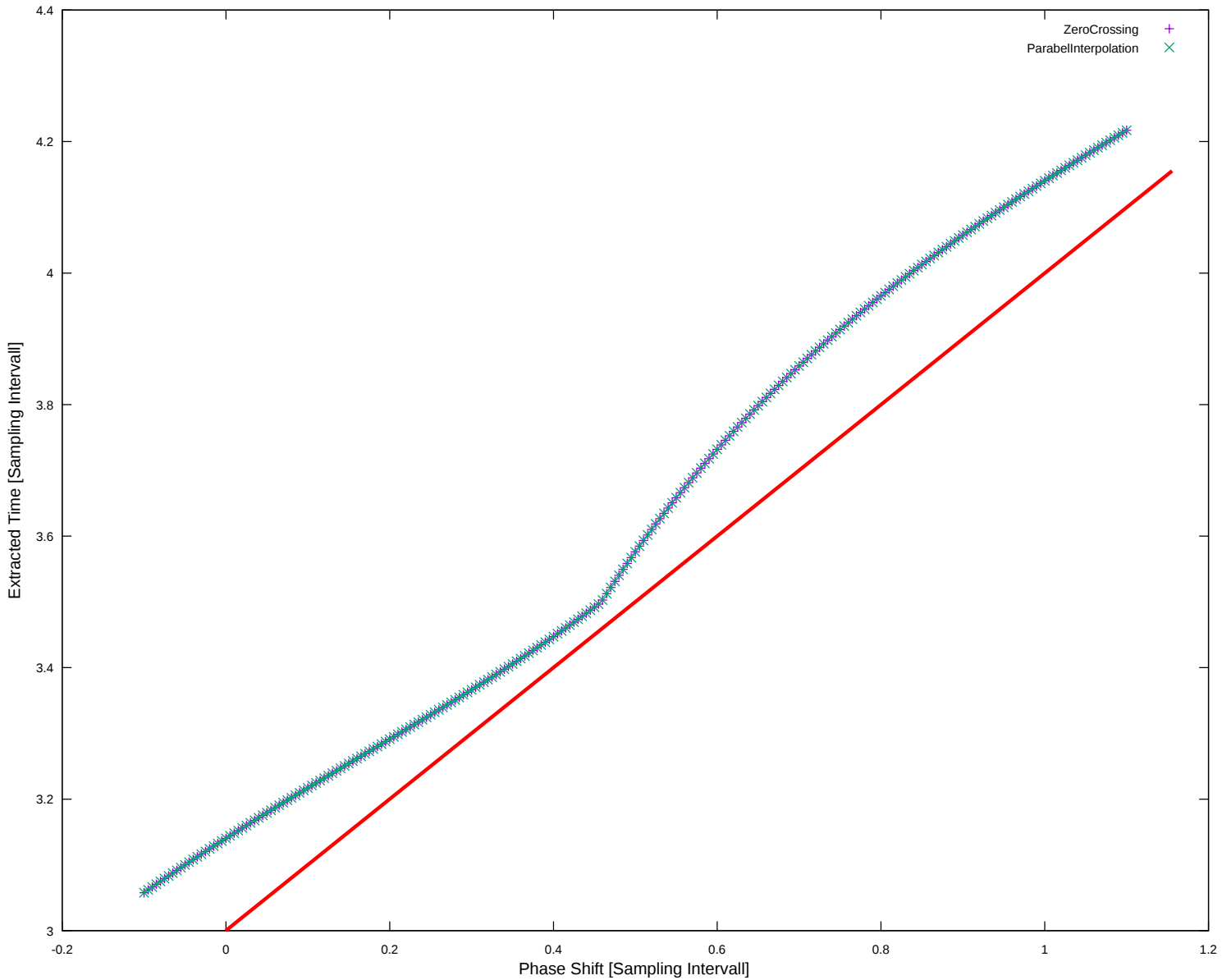
Linear regression of transient and standardised pulse shape

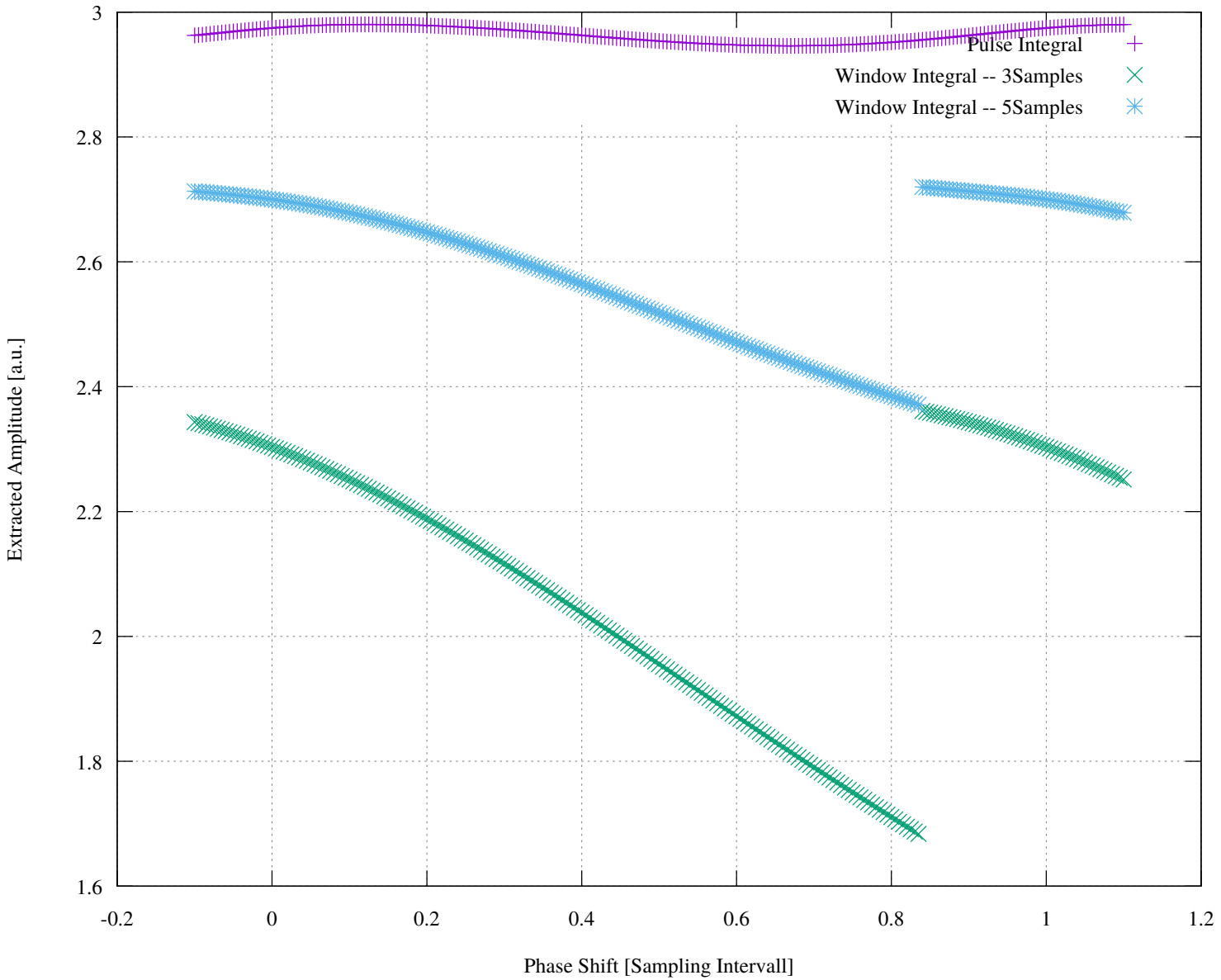


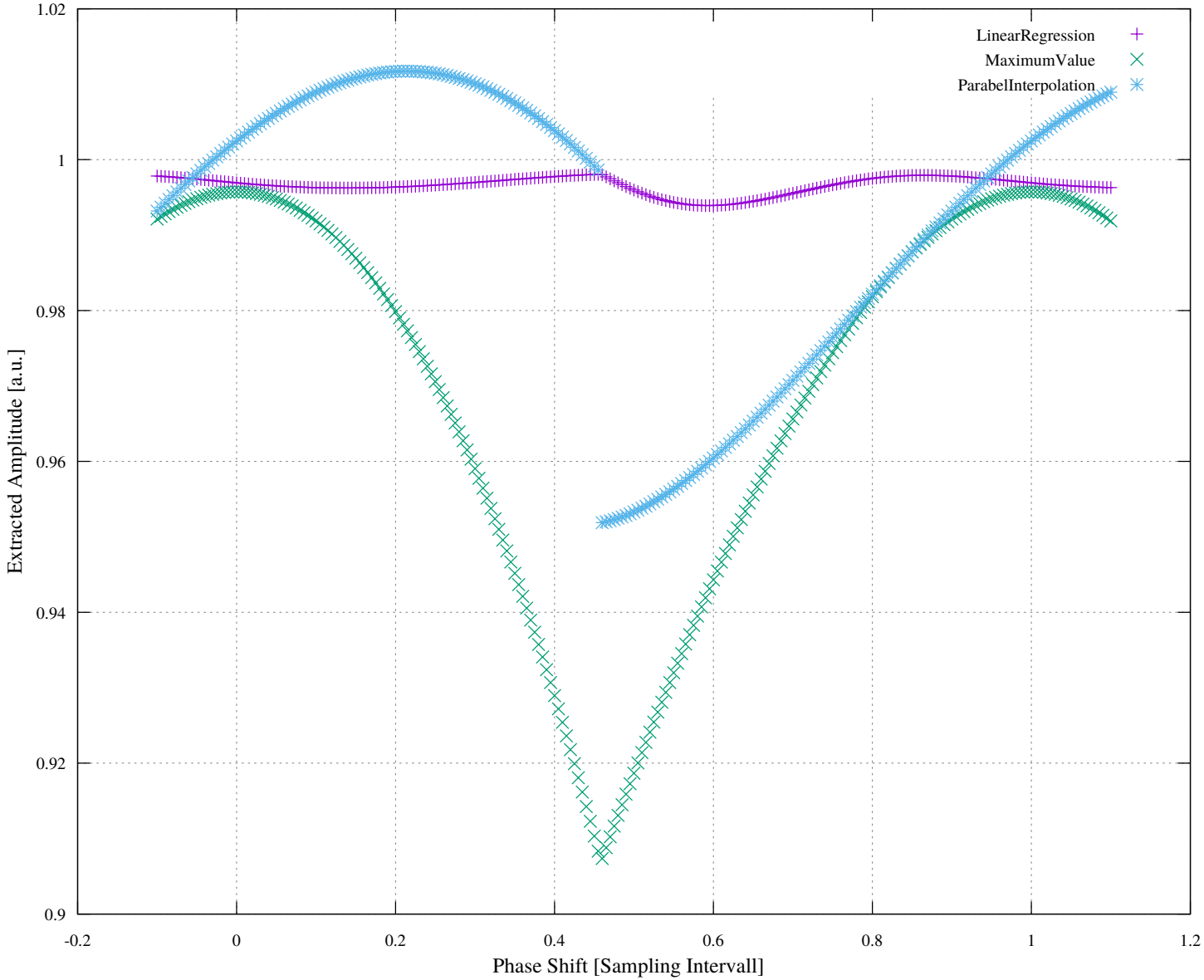


- Based on extracted time a standardised APFEL pulse is generated (green)
- For each sample: Standard APFEL pulse value and transient ADC value
- Linear regression (right side) $\Rightarrow$ baseline, amplitude

$\Rightarrow$ reconstructed APFEL pulse (red)


ZeroCrossing
ParabelInterpolation
Extracted Time [Sampling Intervall]
Phase Shift [Sampling Intervall]
4.4
4.2
4
3.8
3.6
3.4
3.2
3
-0.2
0
0.2
0.4
0.6
0.8
1
1.2


Pulse Integral
Window Integral -- 3Samples
Window Integral -- 5Samples
Extracted Amplitude [a.u.]
Phase Shift [Sampling Intervall]
3
2.8
2.6
2.4
2.2
2
1.8
1.6
-0.2
0
0.2
0.4
0.6
0.8
1
1.2


LinearRegression
MaximumValue
ParabelInterpolation
Extracted Amplitude [a.u.]
Phase Shift [Sampling Intervall]
1.02
1
0.98
0.96
0.94
0.92
0.9
-0.2
0
0.2
0.4
0.6
0.8
1
1.2