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ADC Radiation Mitigation: Fast Reboot

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for the PANDA collaboration

Push-Only Readout

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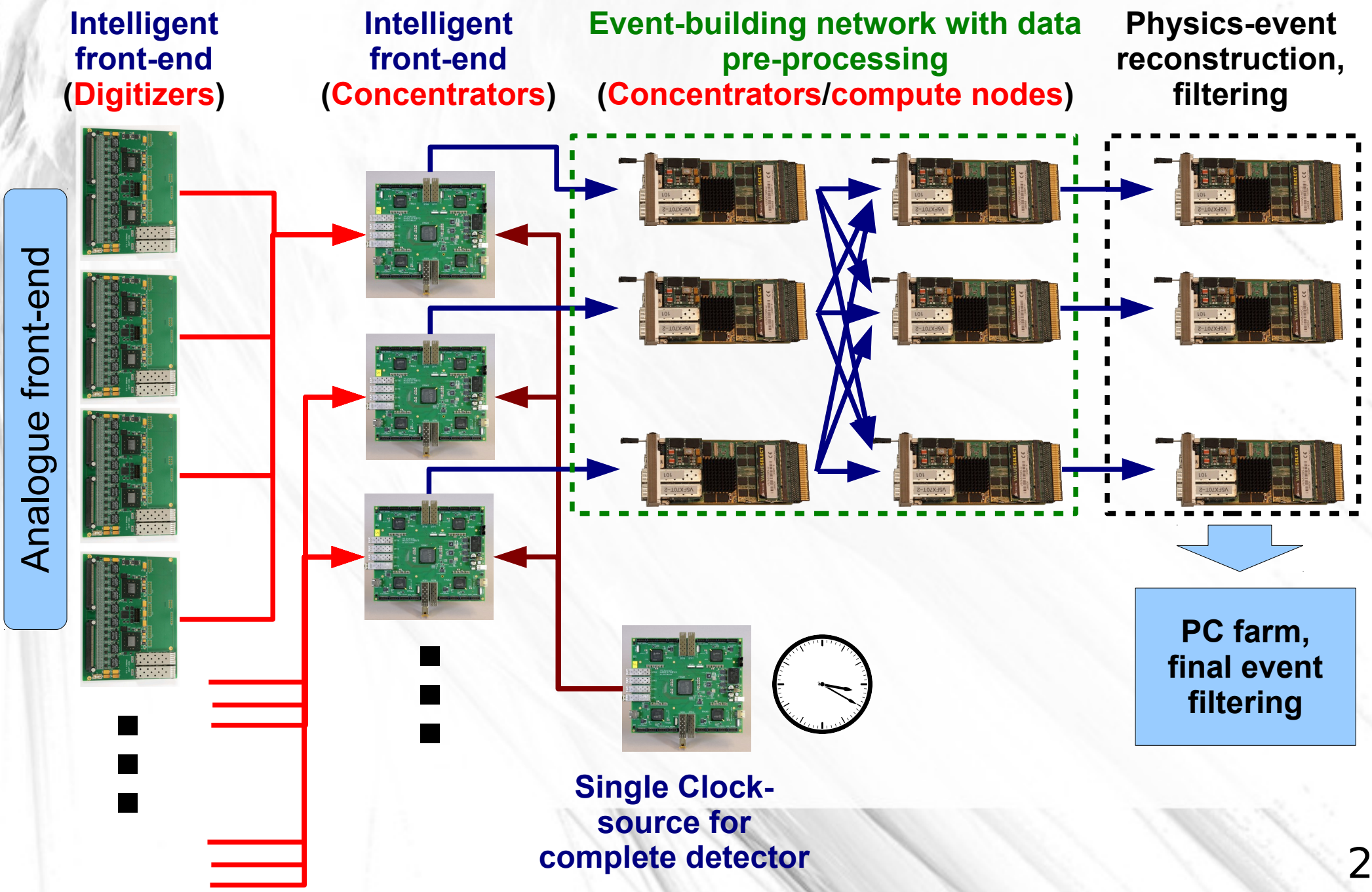

Push-Only Readout

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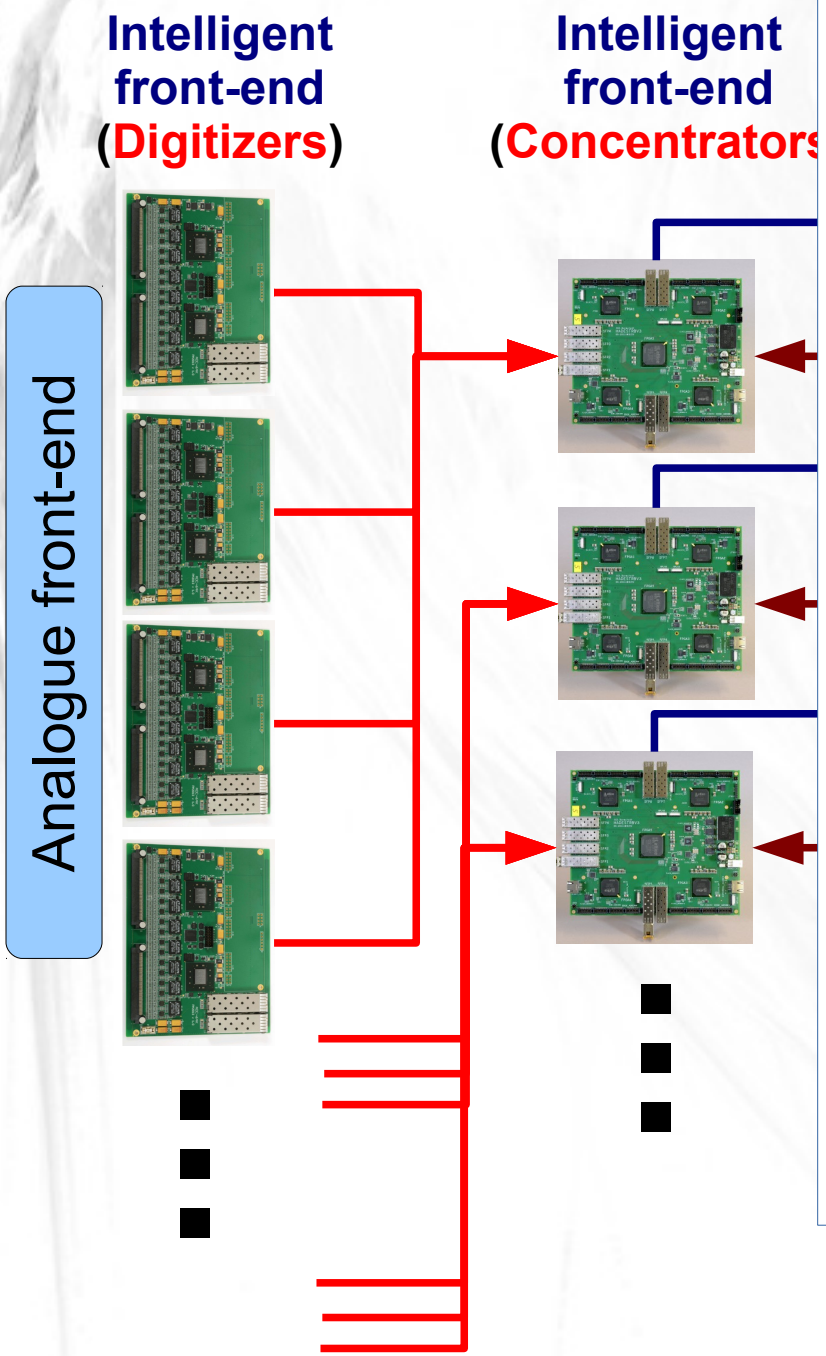

In case FPGA configuration is damaged and cannot be automatically recovered (single-bit errors), compete ADC module has to reboot:

- ADC is power cycled or dedicated “reboot” signal is sent via backplane;
- once booted ADC automatically fetches all required configuration from the data concentrator and start to produce valid data.

ADC Power Cycle

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Power supply

Main Clock, FPGA 1

Main Clock, FPGA 2

The boot time from 'power switched on' to 'clock available' is about 180ms.

Functionality Recovery

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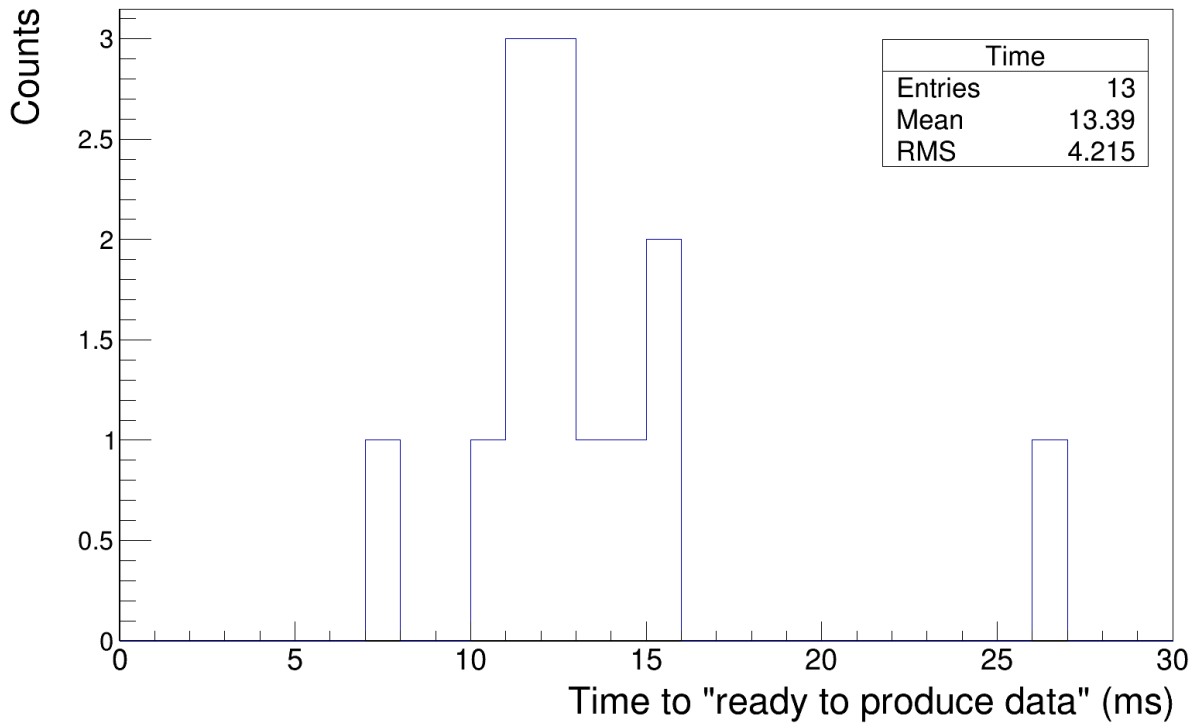
Once FPGA clock is available register values and DAQ status are fetched from the data concentrator – ADC starts to produce data



Additional ~15 ms are required before ADC starts to produce data

FPGA “Reboot”

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Power supply

Main Clock, FPGA 1

Main Clock, FPGA 2

The reboot sequence requires about 150ms.

Summary

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The fast recovery (reboot/reset) sequence is tested:

- **ADC recovers from radiation damage (FPGA configuration) within 200 ms**

Thank you for your attention!