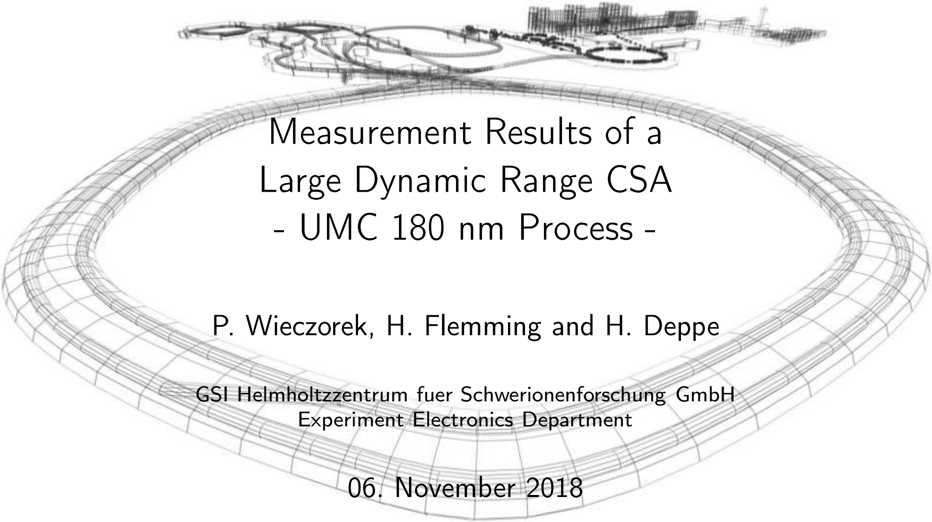

Measurement Results of a Large Dynamic Range CSA - UMC 180 nm Process -

P. Wieczorek, H. Flemming and H. Deppe

GSI Helmholtzzentrum fuer Schwerionenforschung GmbH
Experiment Electronics Department

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Outline

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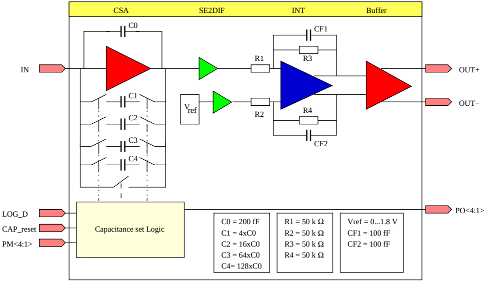
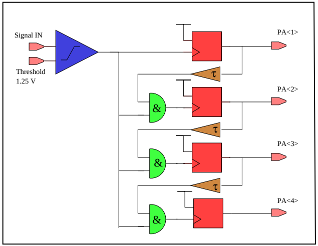


- Charge sensitive amplifier input stage
- Switched feedback capacitances architecture
- Signal transformation: single-end to differential
- Analogue filter and buffer at the output

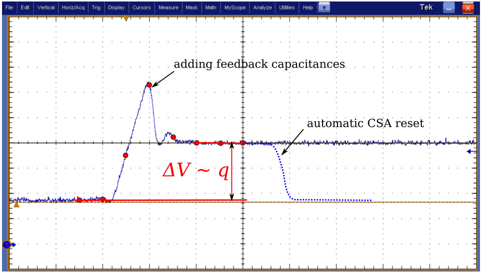
- Large dynamic range of $> 10^5$
- Charge coverage: from noise level up to 45 pC
- Differential output voltage: 1V
- Active reset
- Automatic and manual mode to set feedback capacitances

No.		Unit	Area	Unit
C_0	200	fF	220	µm^2
C_1	$4 \times C_0$	fF	880	µm^2
C_2	$16 \times C_0$	fF	3523	µm^2
C_3	$64 \times C_0$	fF	14080	µm^2
C_4	$128 \times C_0$	fF	28160	µm^2

Outline

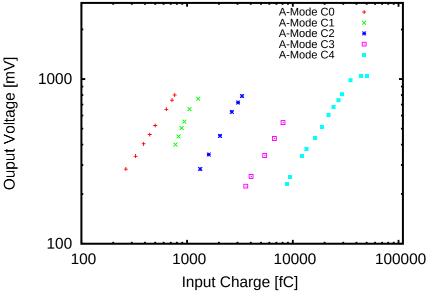


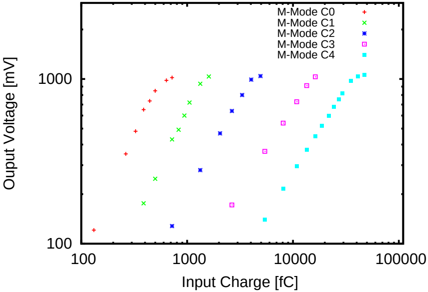
- Manual mode: set fixed feedback capacitances to the amplifier
  - Known feedback cap. configuration
  - Chosen dynamic range is mapped on 1V
- Auto mode: dynamic extension of feedback capacitance
  - Each subrange is 1V
  - Additional readout of feedback configuration is necessary



- Measured transient during capacitance extension to the feedback is depicted
- Adding capacitance keeps the amplifier from saturation (up to 42pC)
- But: dynamic loss of 20%

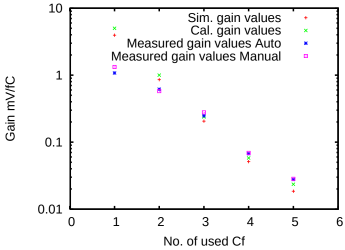
Outline





- Measured with auto mode
- Measured with manual mode

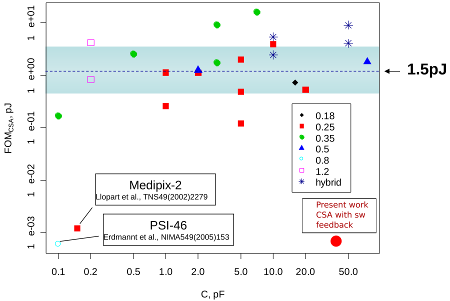
- Max. measured charge: up to 42pC
- Different slope for cap. $C1$ in auto mode



Simulation mV/fC	Measured A mV/fC	Measured M mV/fC
3.94	1.330	1.892
0.855	0.922	0.818
0.205	0.255	0.253
0.0511	0.071	0.068
0.0185	0.028	0.028

- Gain for C_0 capacitance is about 3x lower as expected $\Rightarrow$ influence of the RC - parasitic effects
- Optimization in next version

- Summary of the noise calculation
  (compare: FEE Workshop 2018 at GSI)
  - $C_T = C_{gs} + C_{det} + C_f$ optimise parameter
  - C_T as small as possible $\Rightarrow$ low noise contribution
  - C_{det} (detector capacitance): fixed
  - C_{gs} increases with the transistor geometry
    $\Rightarrow$ trade off between transistor width and capacitance
  - Feedback capacitance C_f: $\Rightarrow$ trade off between noise and dynamic range
- C_{gs}=20 pF; C_{det}=50 pF; C_f=1 pF .... 30 pF
  $\Rightarrow$ C_T=71...100 pF
- Measured CSA noise ($C_0 = 200fF$) is $\sigma > 0.38$ fC



- Following O'Conner a figure of merit (FOM) defined as

$$FOM_{Preamp} = \frac{Power \times \tau_s}{Q_{max}/\sigma_Q}$$

- Short peaking time of $\tau_s = 20\,\mathrm{ns}$
- Measured noise of $\sigma_Q = 0.4\,\mathrm{fC}$
- Large dynamic range of >100 000

- Present design: FOM = 2fJ (excellent result)

Outline

- First Prototype works excellent
- Optimize in the next version:
  - Gain in the initial state (with cap. $C0$)
  - Noise: blocking of voltage references
  - Active filter in the feedback of the output stage
  - Resistance of the capacitance switches

- First customer is beam diagnostics for the readout of the SEM - grids
- A 4 channel prototyp is submitted in summer 2018

- Noise calculations for the input transistor as dominant noise source

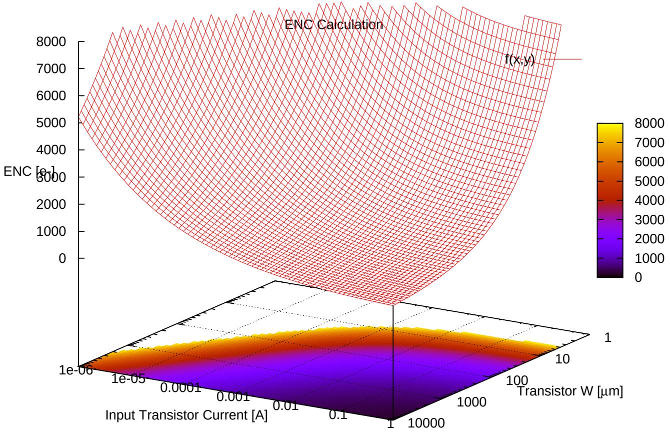
$$ENC_{th}^2[e^2] = \frac{10 \cdot k_B \cdot T}{8 \cdot q^2} \frac{C_T^2}{\tau_s \cdot \sqrt(k_x \cdot W/L \cdot I_{ds})} \quad (1)$$

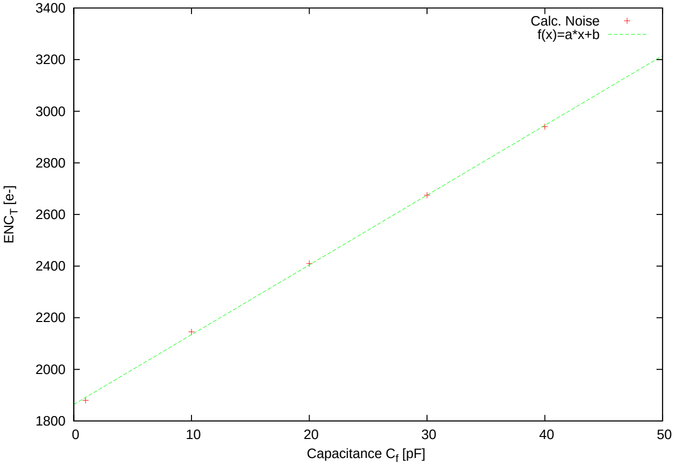
$$ENC_{1/f}^2[e^2] = \frac{4 \cdot K_f}{C_{ox}^2 \cdot q^2} \frac{C_T^2}{W \cdot L} \quad (2)$$

$$ENC_{DET}^2[e^2] = \frac{2}{q} \cdot I_{det} \cdot \tau_s \quad (3)$$

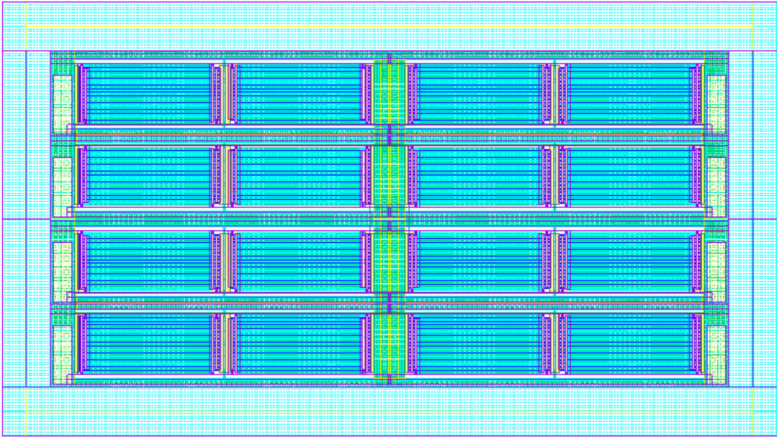
$$ENC_{tot}^2 = ENC_{th}^2 + ENC_{1/f}^2 + ENC_{DET}^2 \quad (4)$$

- Optimise transistor parameter W/L and I_{ds}
  - Input transistor ratio W/L high ⇒ large input capacitance
  - Current through input transistor large ⇒ high power consump.



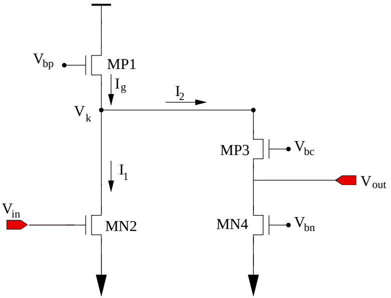


- Small capacitance for small signals ⇒ better SNR



- Layout input transistor with W/L: 35 556 ($256 \times 25/0.18$)
- Input transistor area on chip: 330 µm × 95 µm

- CSA based on folded cascode architecture



No.	Current (TT ; SS ; FF)	Unit
I_g	3.1 ; 2.6 ; 3.81	mA
I_1	2.6 ; 2.2 ; 3.25	mA
I_2	0.5 ; 0.4 ; 0.55	mA

	MN2	MP1	MP3	MN4	Unit
Number	256	20	10	8	1
W	25	15	60	2.5	µm
L	0.18	1	0.5	1.5	µm
I_{ds}(TT)	2.6	3.1	0.5	0.5	mA