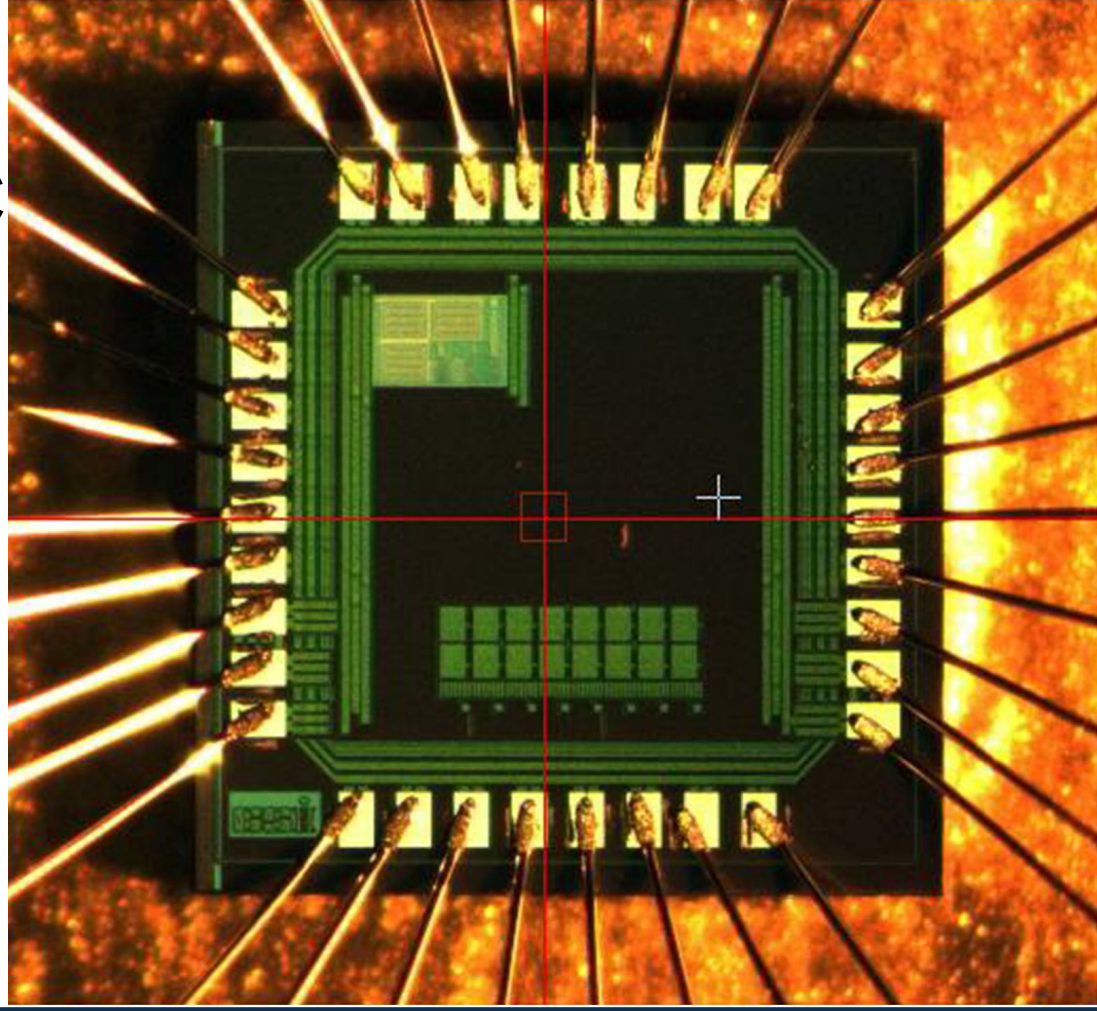
Status of the SerialAdapter ASIC tests



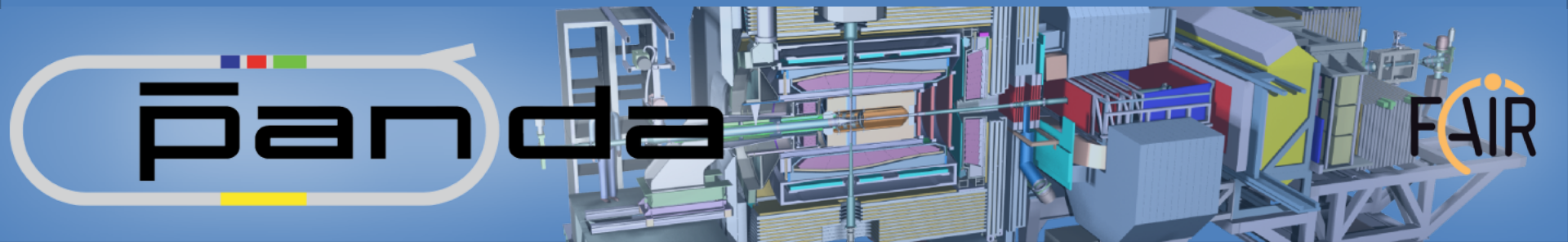
Federal Ministry of Education and Research

JUSTUS-LIEBIG-UNIVERSITÄT GIESSEN

GSI

Christopher Hahn*, and for the PANDA collaboration
*2nd Physics Institute, University Giessen, Germany

HIC for FAIR
Helmholtz International Center

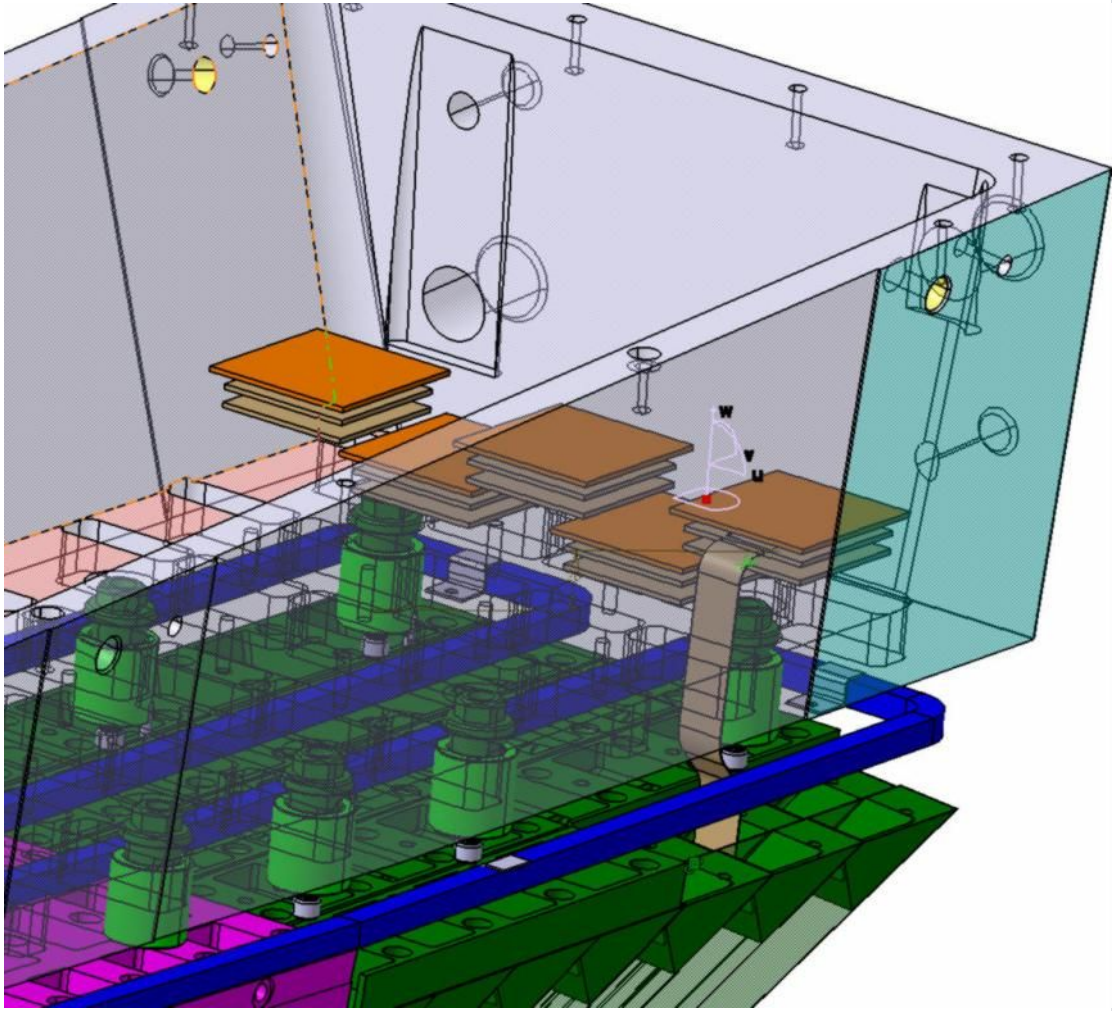


Outline

- **Introduction**
- **Setup description**
- **Readout of the version register**
- **Status of the functionality Tests**
- **DAC measurements**
    - General measurements
    - Stability measurements
- **Conclusion**

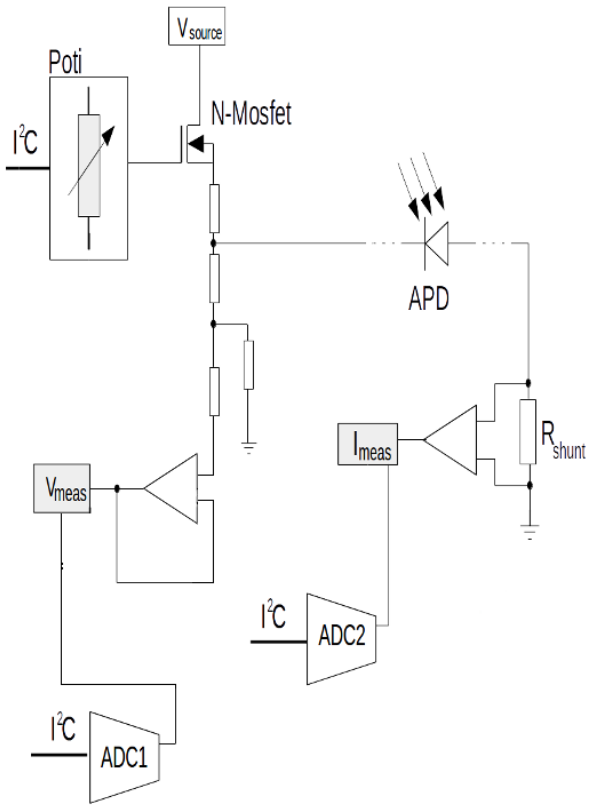
Introduction

- **Present design: 3 Layers**
  - **HV distribution & regulation**
  - **Connector board for custom signal Cables**
  - **Board for FlexPCBs / ASICS**
    - **Connectors to FEs**
    - **8x2 Diff. Line drivers**
    - **APFEL I/F buffers**
    - **Temp/Humidity sensors**

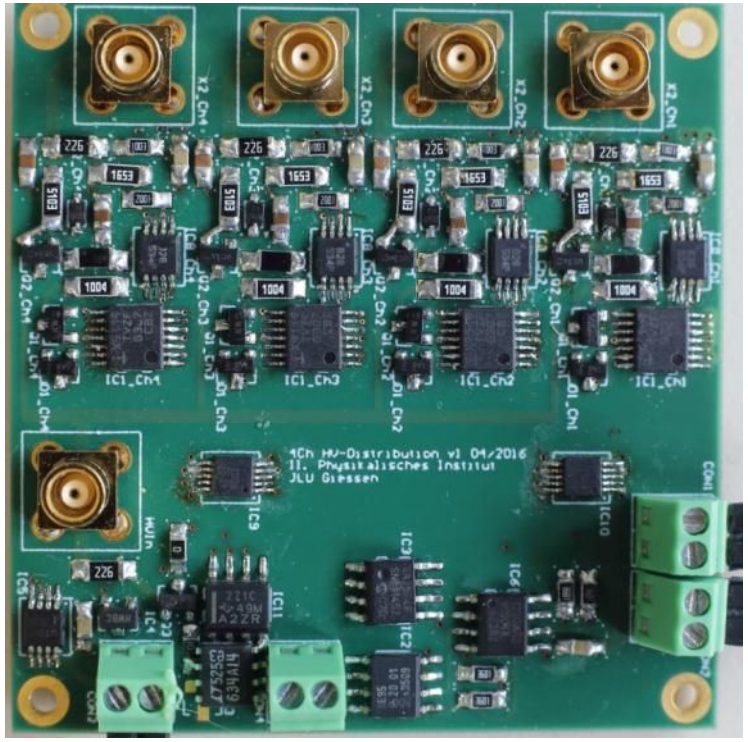


Introduction

- **Device to independently adjust bias voltage of 8 APDs**
  - **50V from HV input downwards in < 0.1V steps**
- **All channels fed from the same HV source**
- **Online measurement of APD voltage and current**



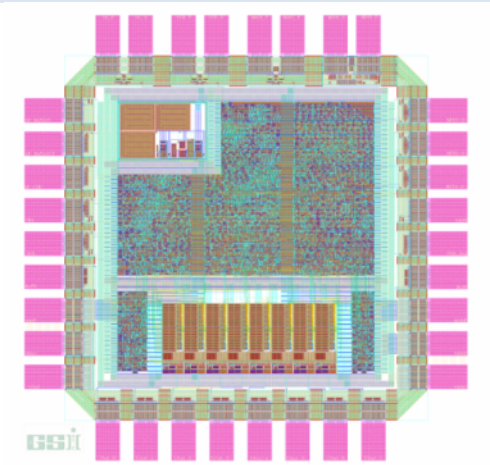
Single channel block schematic

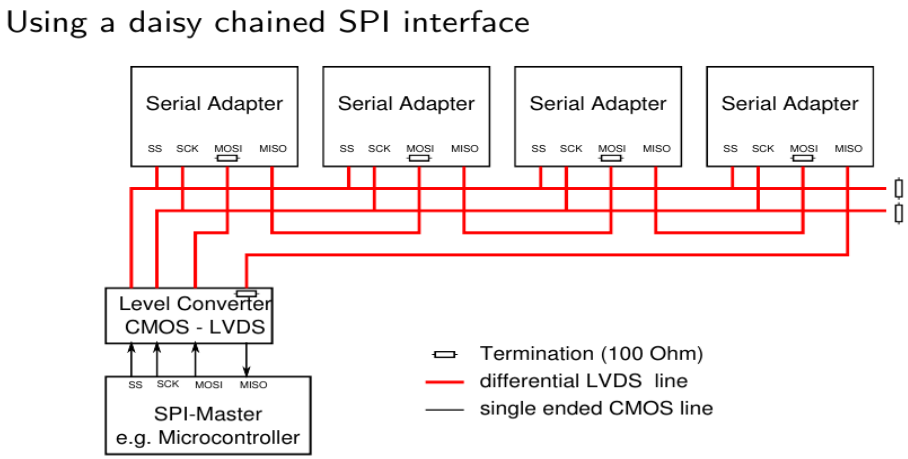


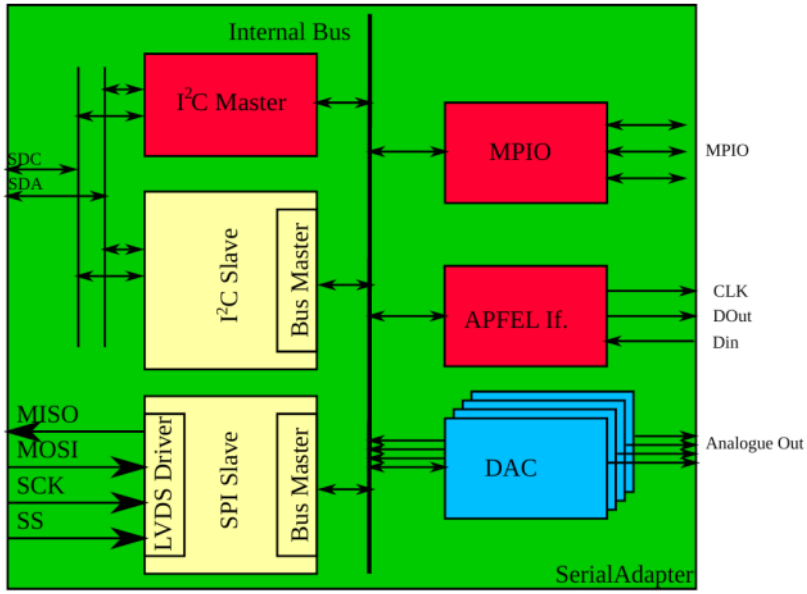
4-ch prototype
size: 6 x 5.5 cm²

Introduction

- **Present design: two different busses for FE and HV regulators**
- **Idea: integrated Slow Control ASIC with common busses**
- **Daisy chaining of Backend-Interface for 5 (10) Backplane PCBs → Saves 4/5 of Slow Control Cables (36 vs. 180)**



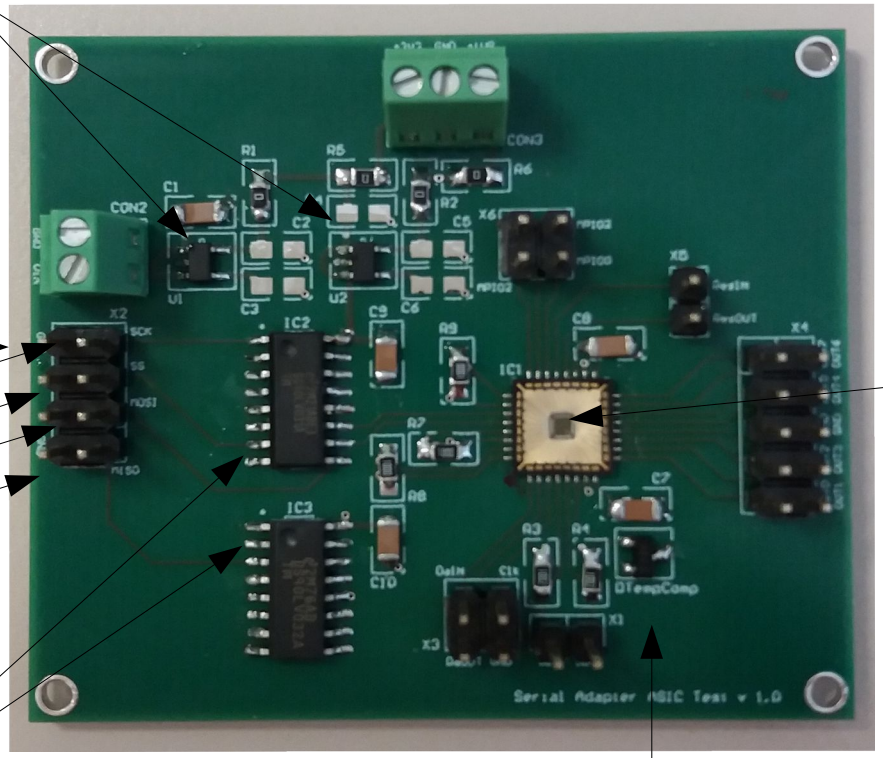




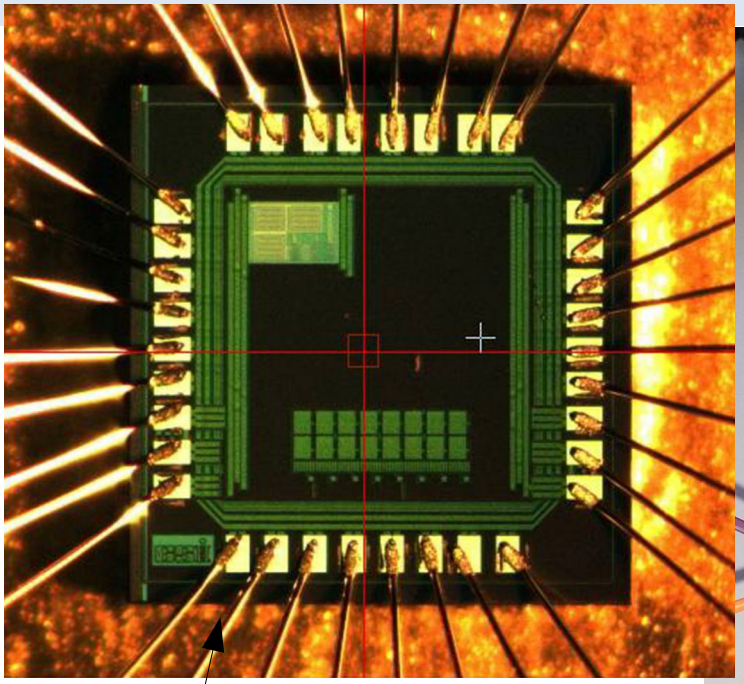
Special Ultra-thin differential cables developed in corporation with company BEDEA (Germany)

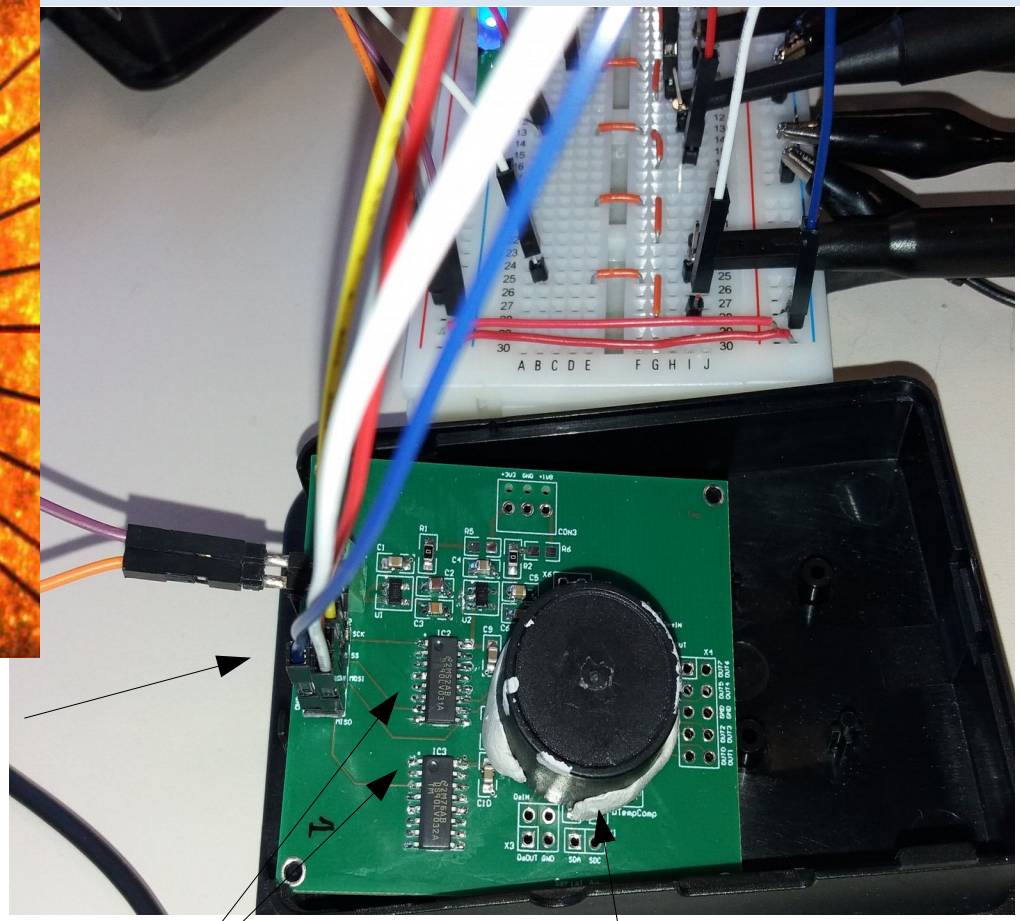
All necessary cables will fit trough the window

Setup – SerialAdapter ASIC Testboard



Setup – SerialAdapter ASIC Testboard





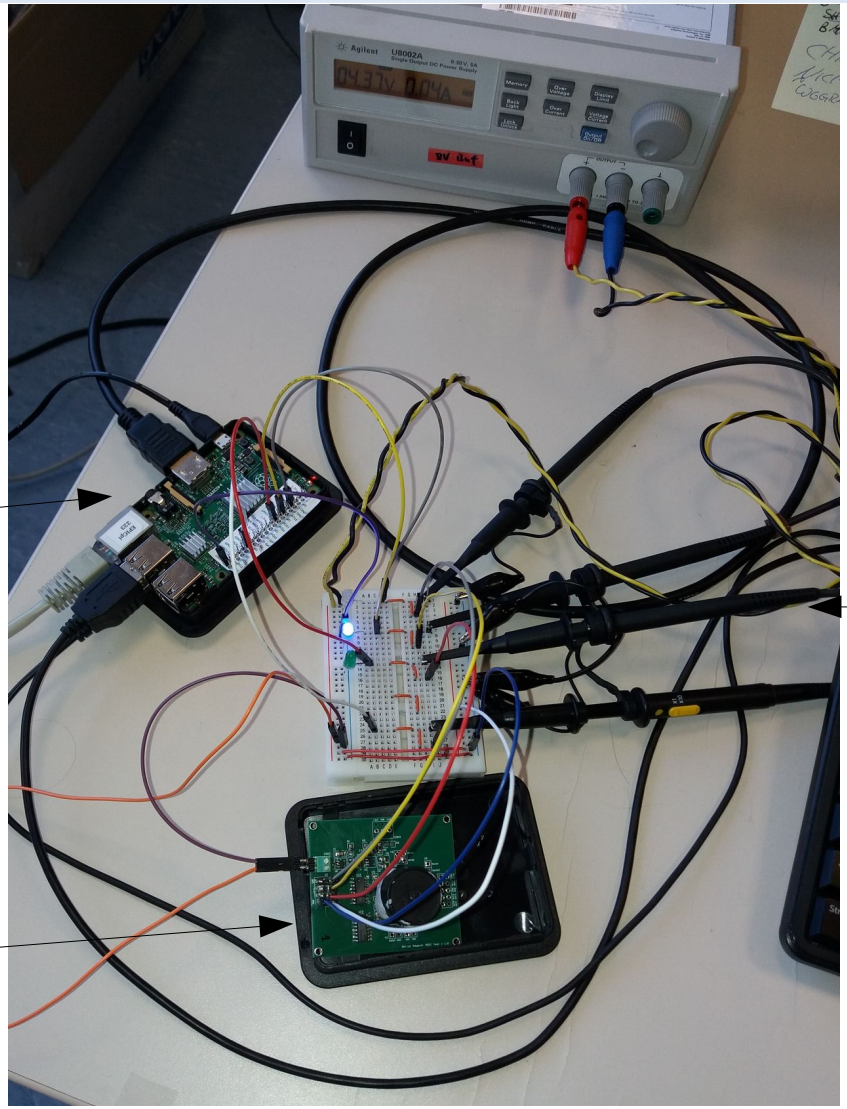
Serial Peripheral Interface lines

SerialAdapter ASIC

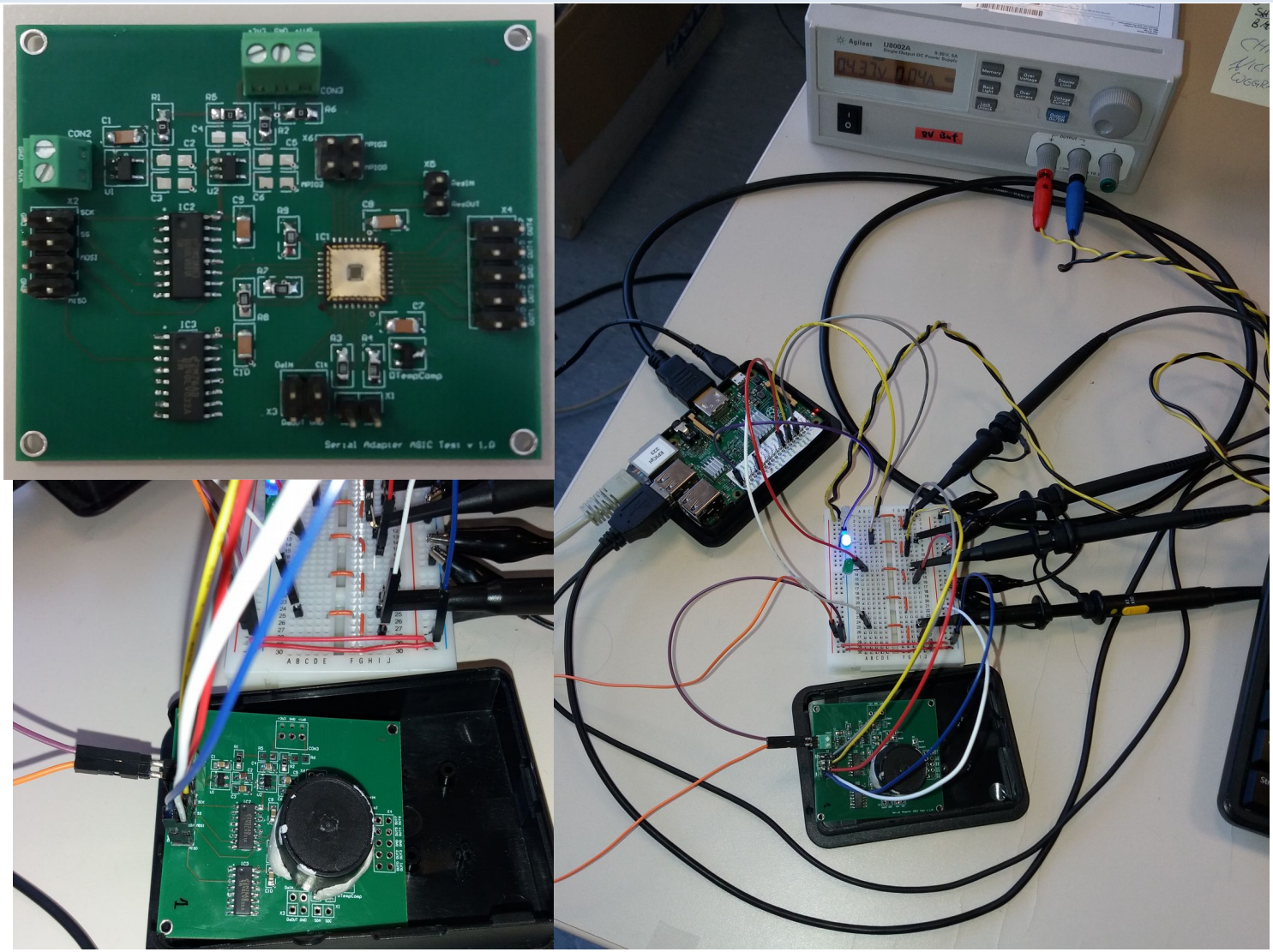
Line Converters

SerialAdapter ASIC

Setup – SerialAdapter ASIC Testboard

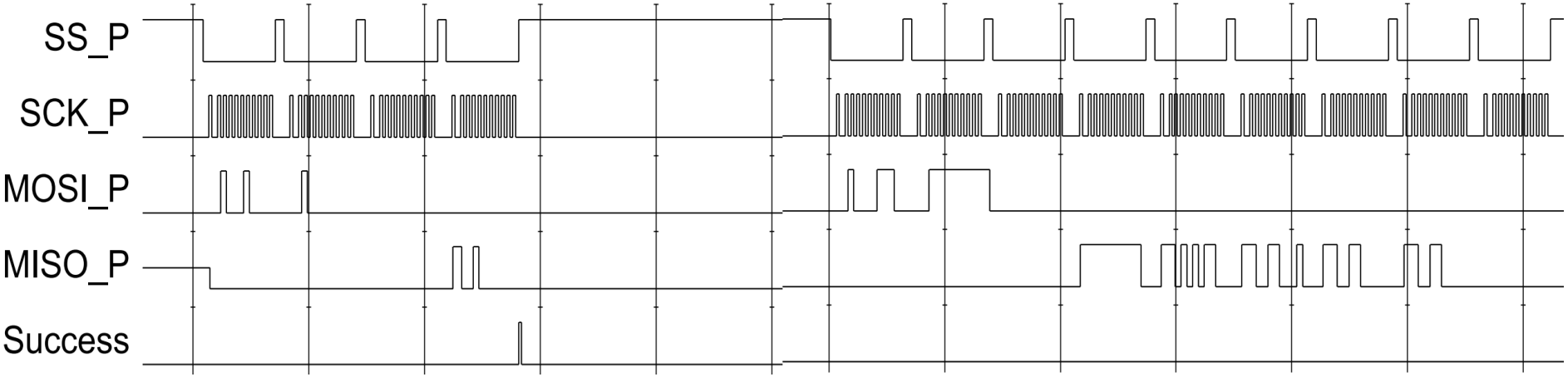


Setup – SerialAdapter ASIC Testboard

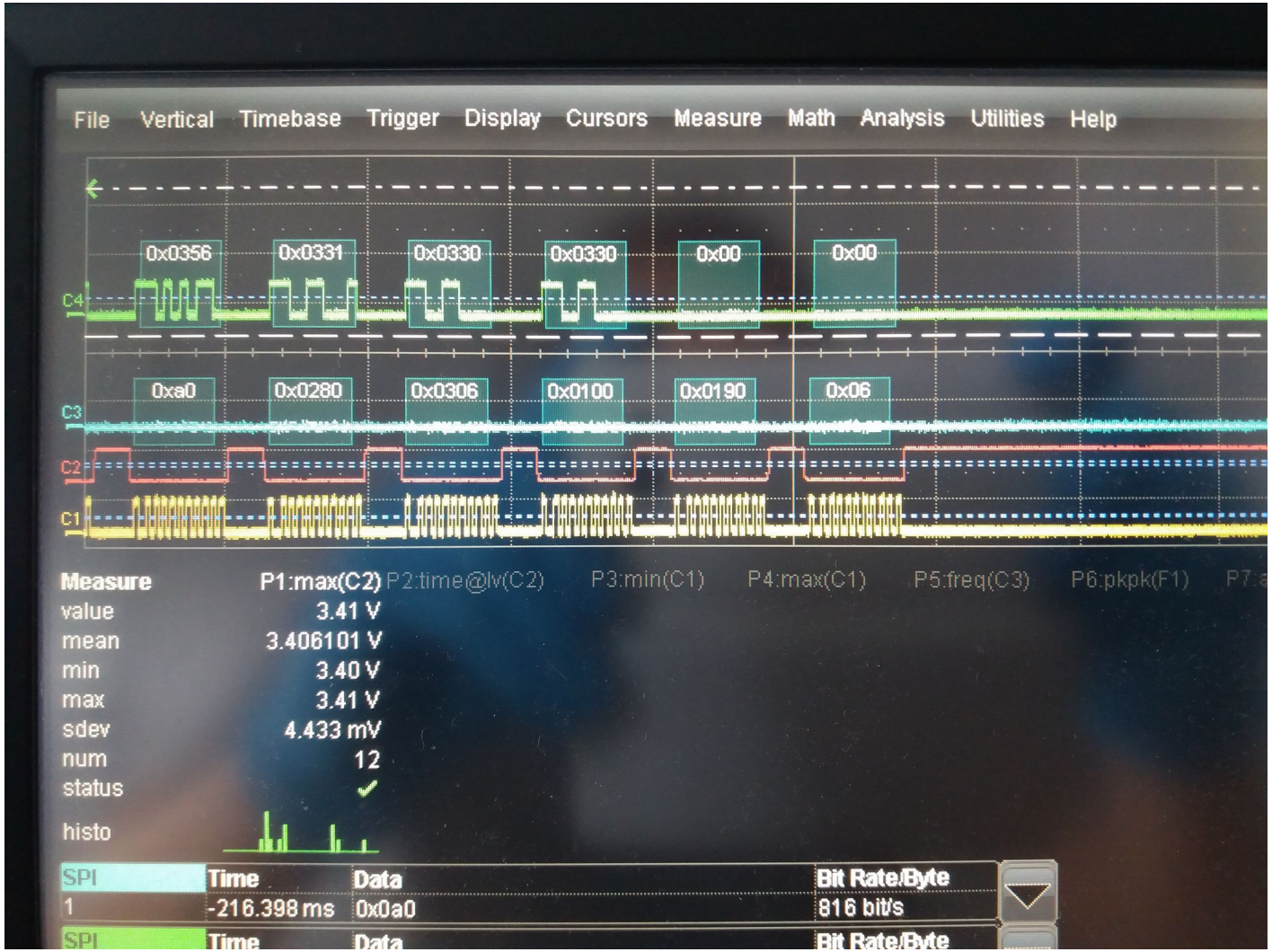


Readout of the Version Register

- **First test**
  → **readout of version register of SerialAdapter ASIC**
- **10-bit SPI (Serial Periphal Interface) command**
- **Answer should be 0x56313030 (hex)**



Readout of the Version Register



MISO
MOSI
SS
CLK

10 bit → 8 bit
→ 0x56313030

✓

Status of the Functionality Tests

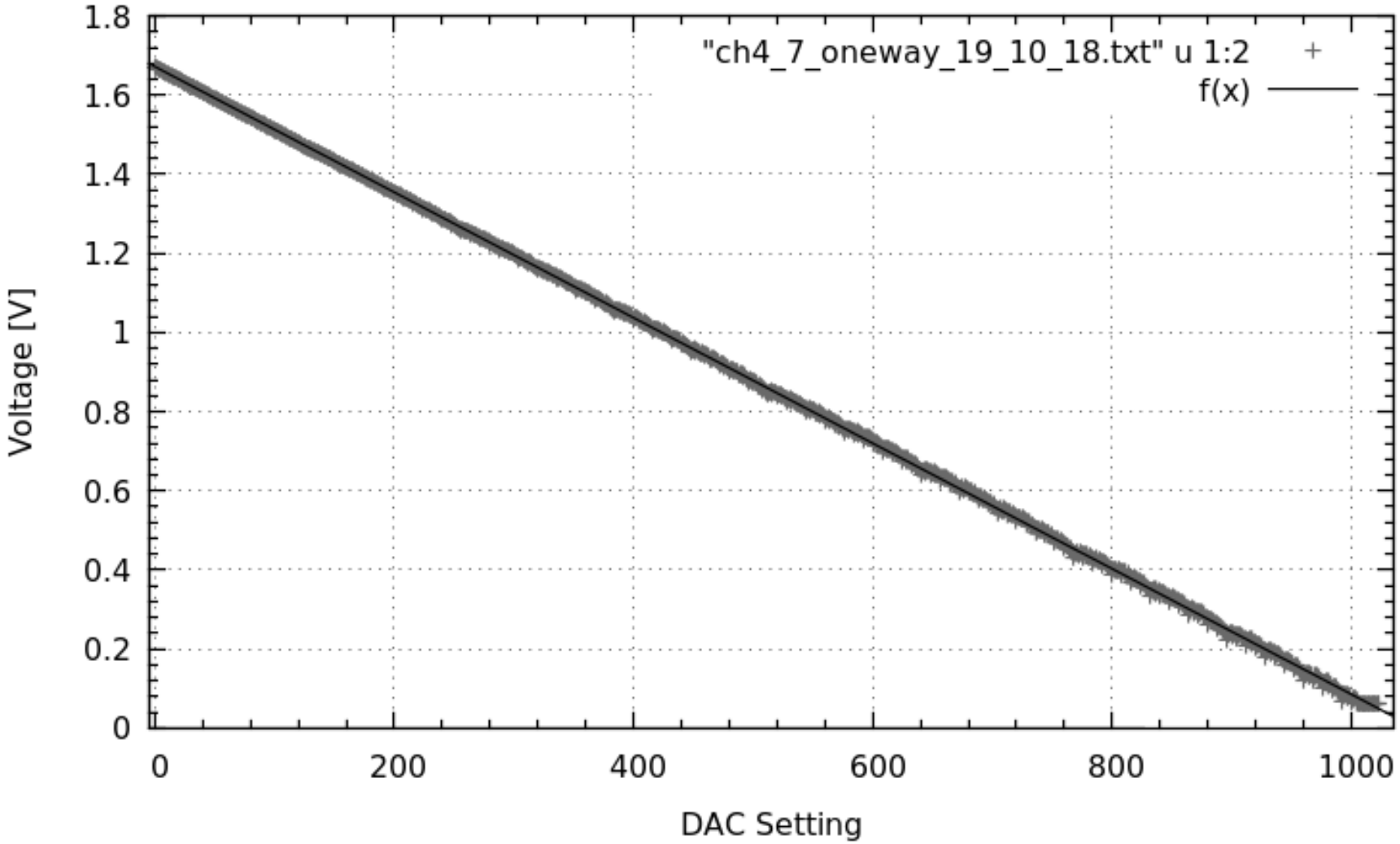
Name	Adress	SPI Response	Signal Measured
Chip version register	0xff	✓	-
I2C Master Interface	0x00-0x23	✓	*first tests* ✓
DAC Control	0x40-0x47	✓	✓
APFEL Interface mode	0x48	✓	*pending*
APFEL Interface data	0x49	✓	*pending*
Hamming Error Counter	0x4a	*pending*	*pending*
Parallel IO Config Register	0x4c	✓	✓
Parallel IO Data Register	0x4d	✓	✓

DAC Measurements

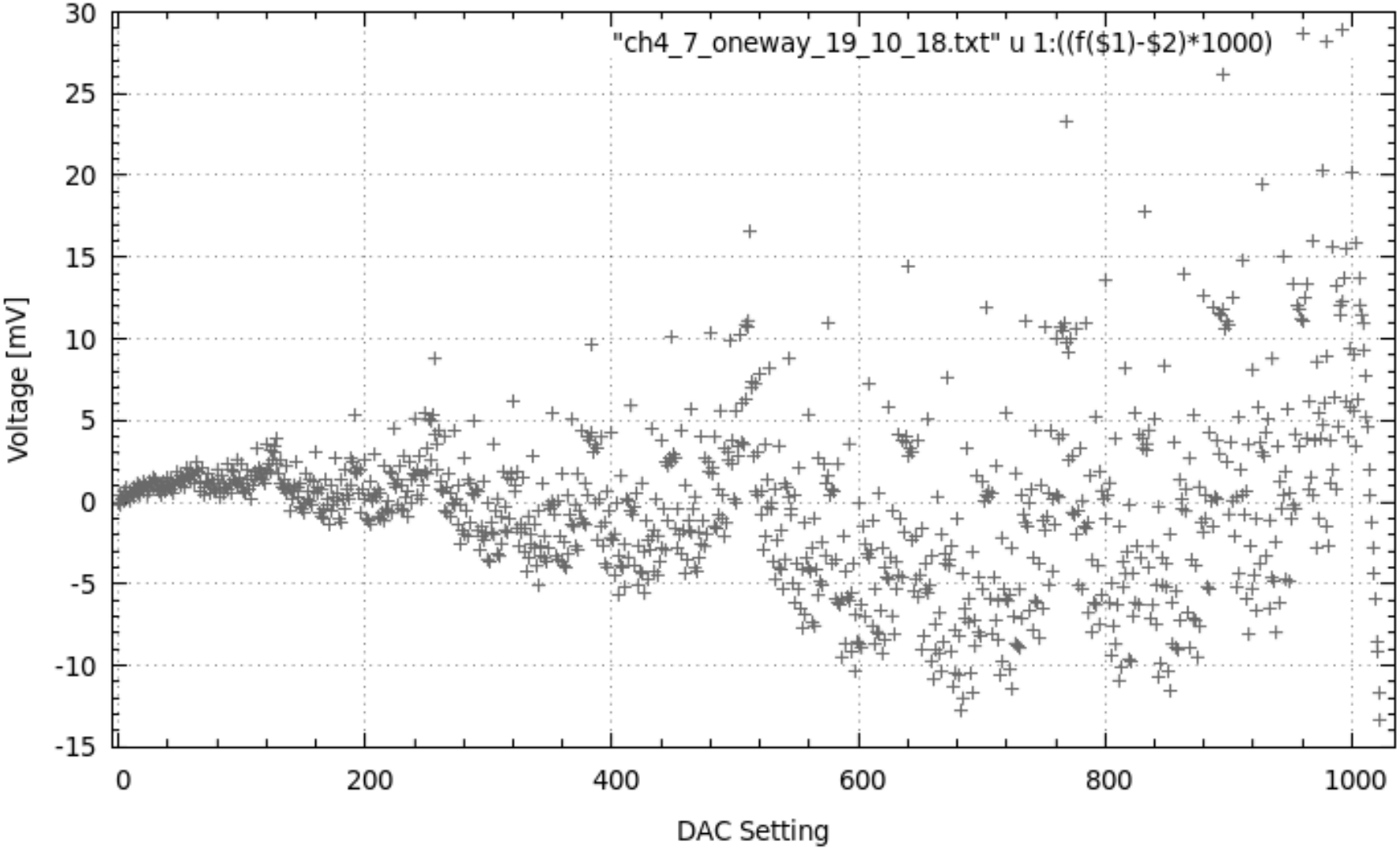
- **Scan over all DAC settings (10bit)**

  → **1,67 V /1023 = 1,63mV = 1 LSB**
- **Voltage measured by ADS1115 (16-bit ADC)**
- **Residual plotted**
- **Time dependency Tests**

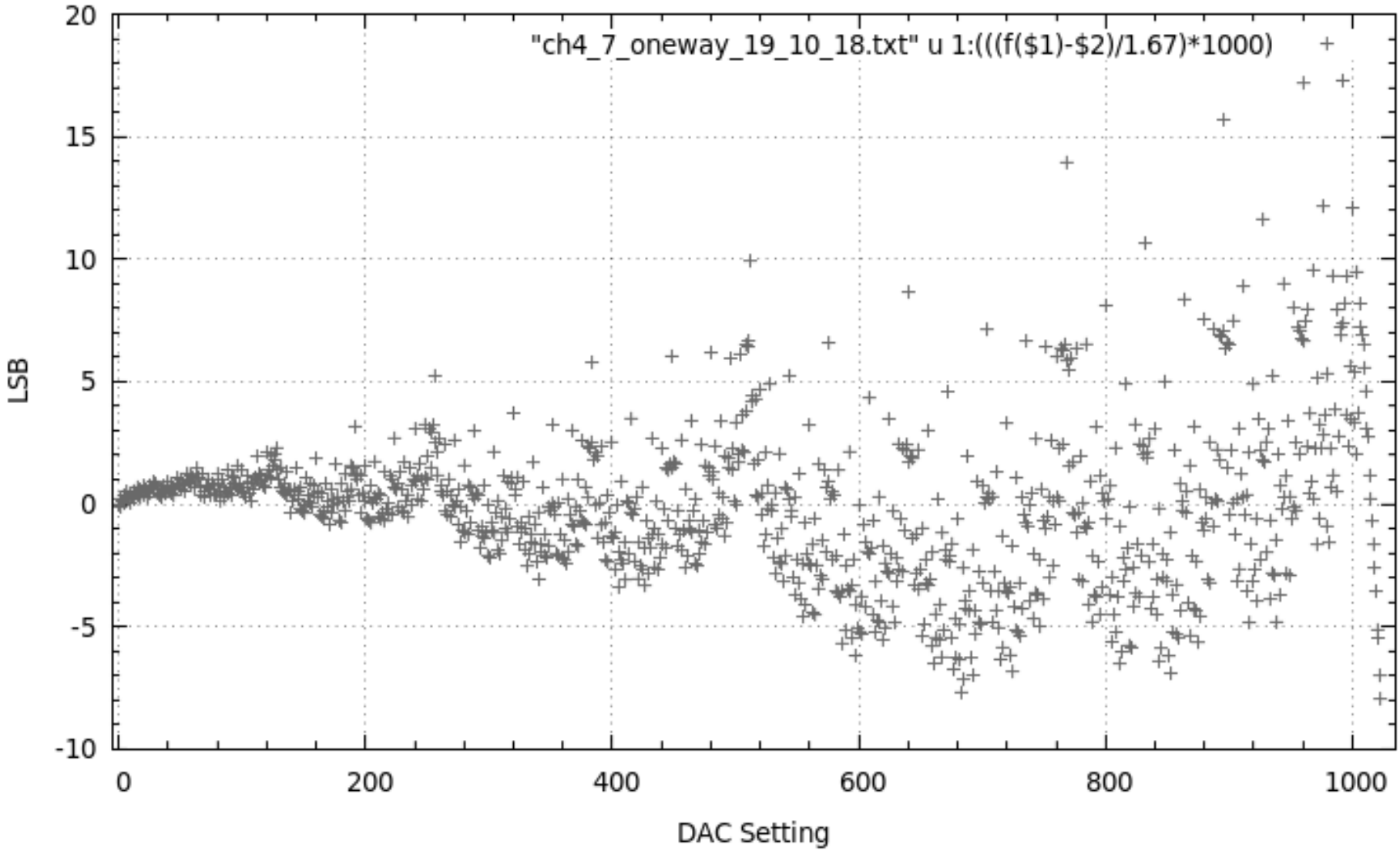
DAC Measurements – General Measurements



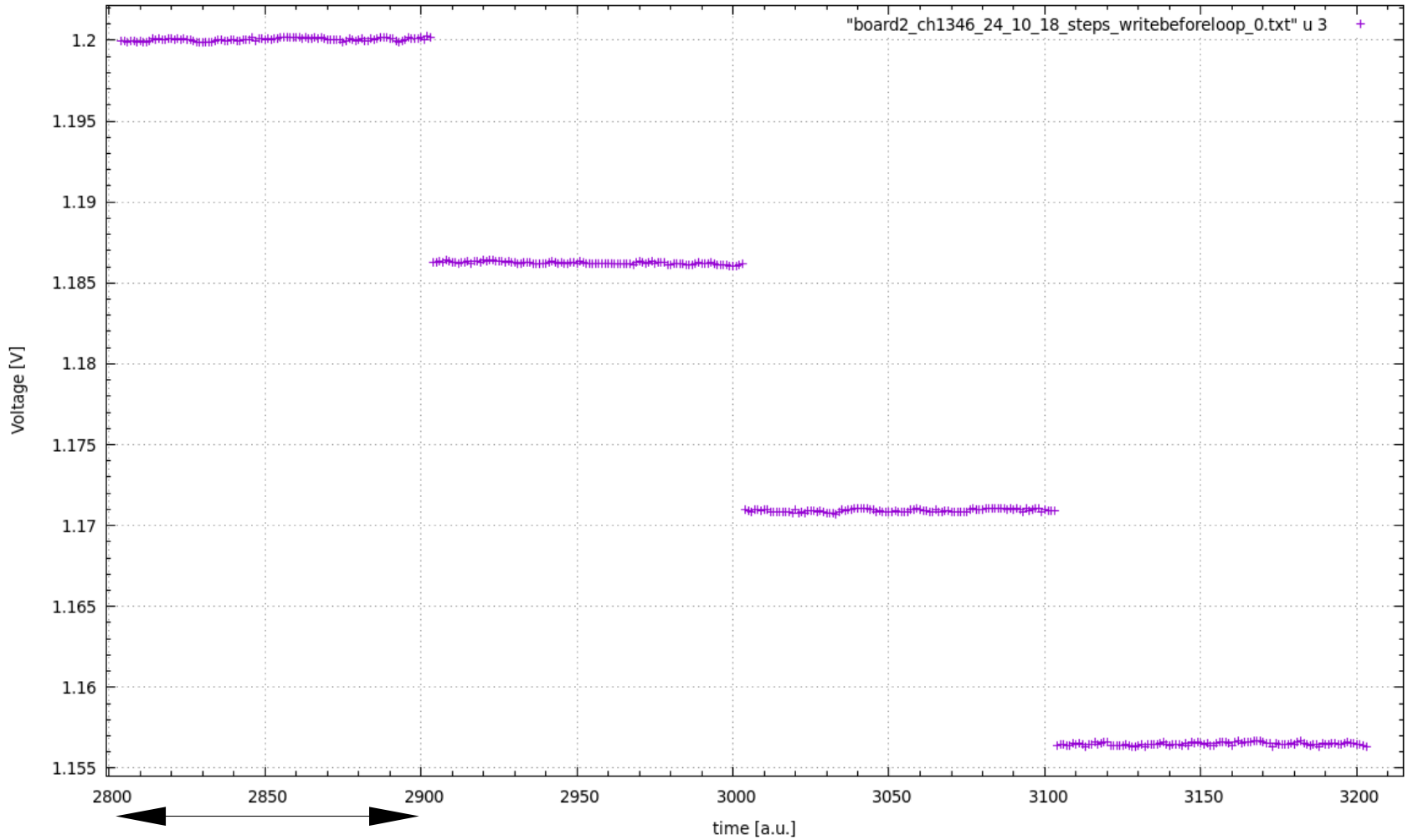
DAC Measurements – General Measurements



DAC Measurements – Stability Measurements



DAC Measurements – Stability Measurements



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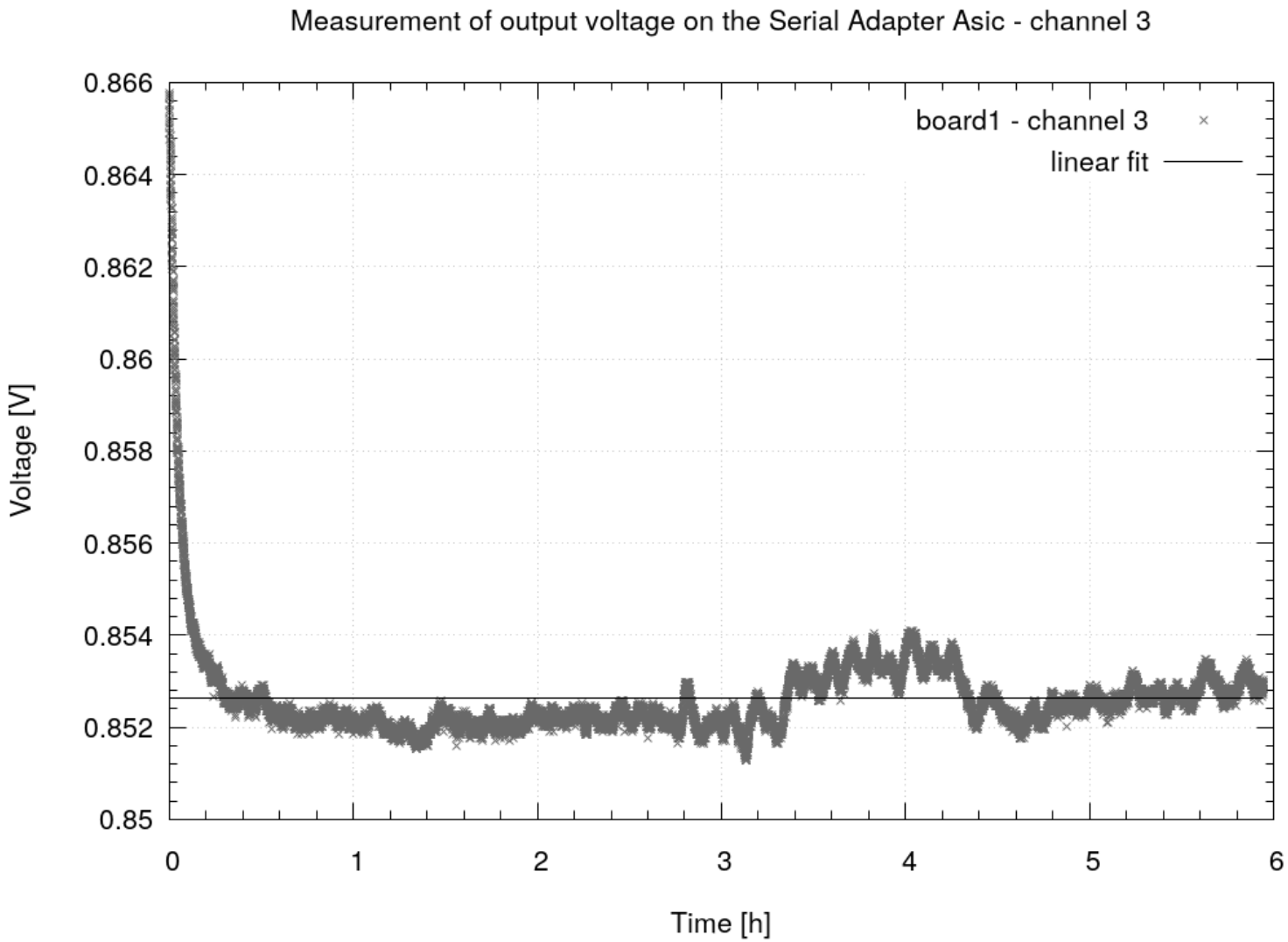

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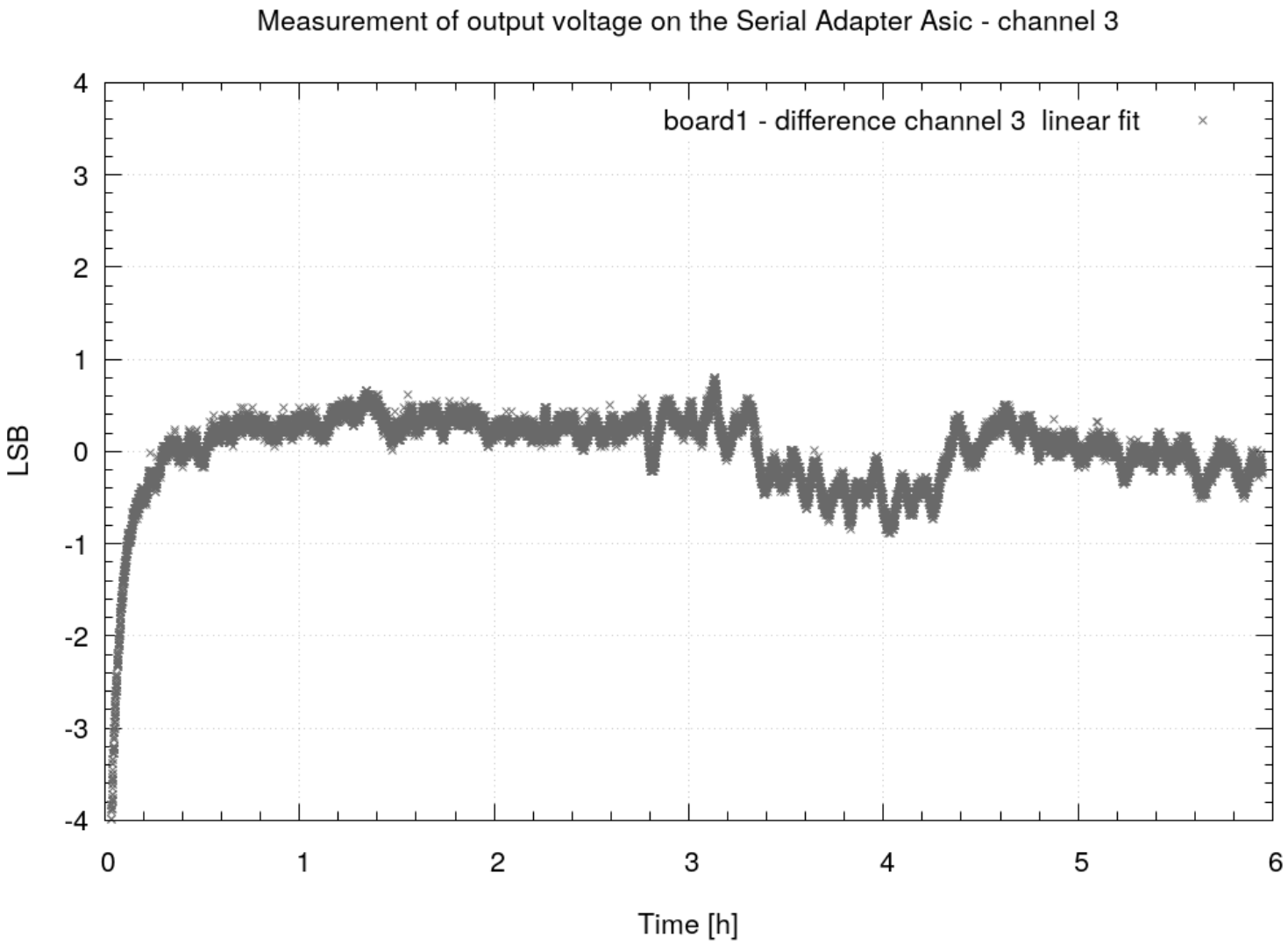


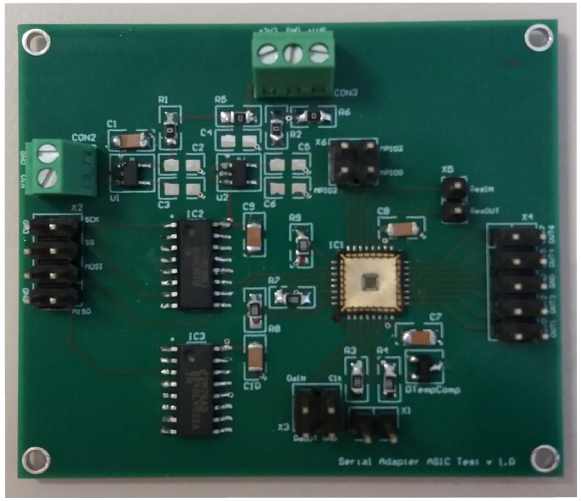
Conclusion/ Outlook

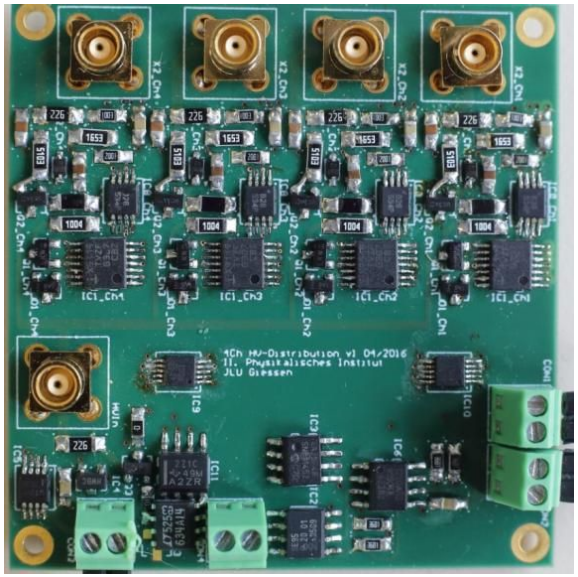
- **All tested functionalities work as expected**
- **DAC register settings indicate a problem with linearity (in current state)**

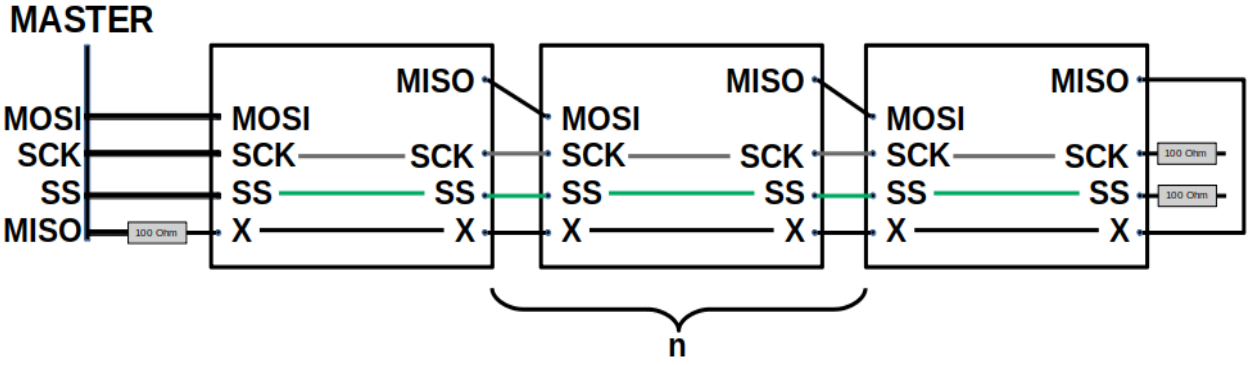
  → designer is looking for suitable solutions
- **Next steps:**

  - Drive a old HV-board via a Testboard

  - Set up a daisy chain with existing Testboards







Thank you for your attention