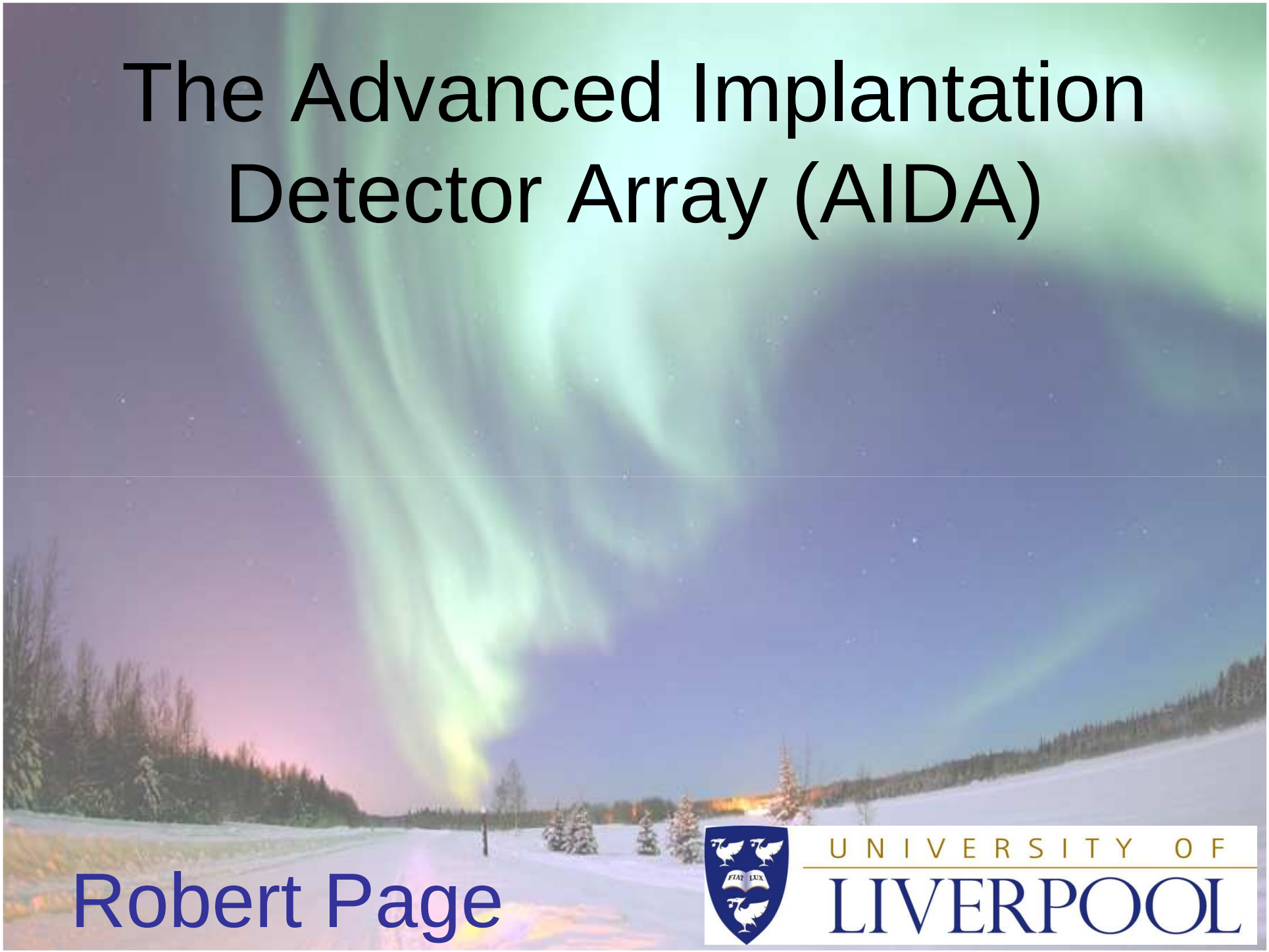
The Advanced Implantation Detector Array (AIDA)



Robert Page

UNIVERSITY OF LIVERPOOL

The AIDA Project

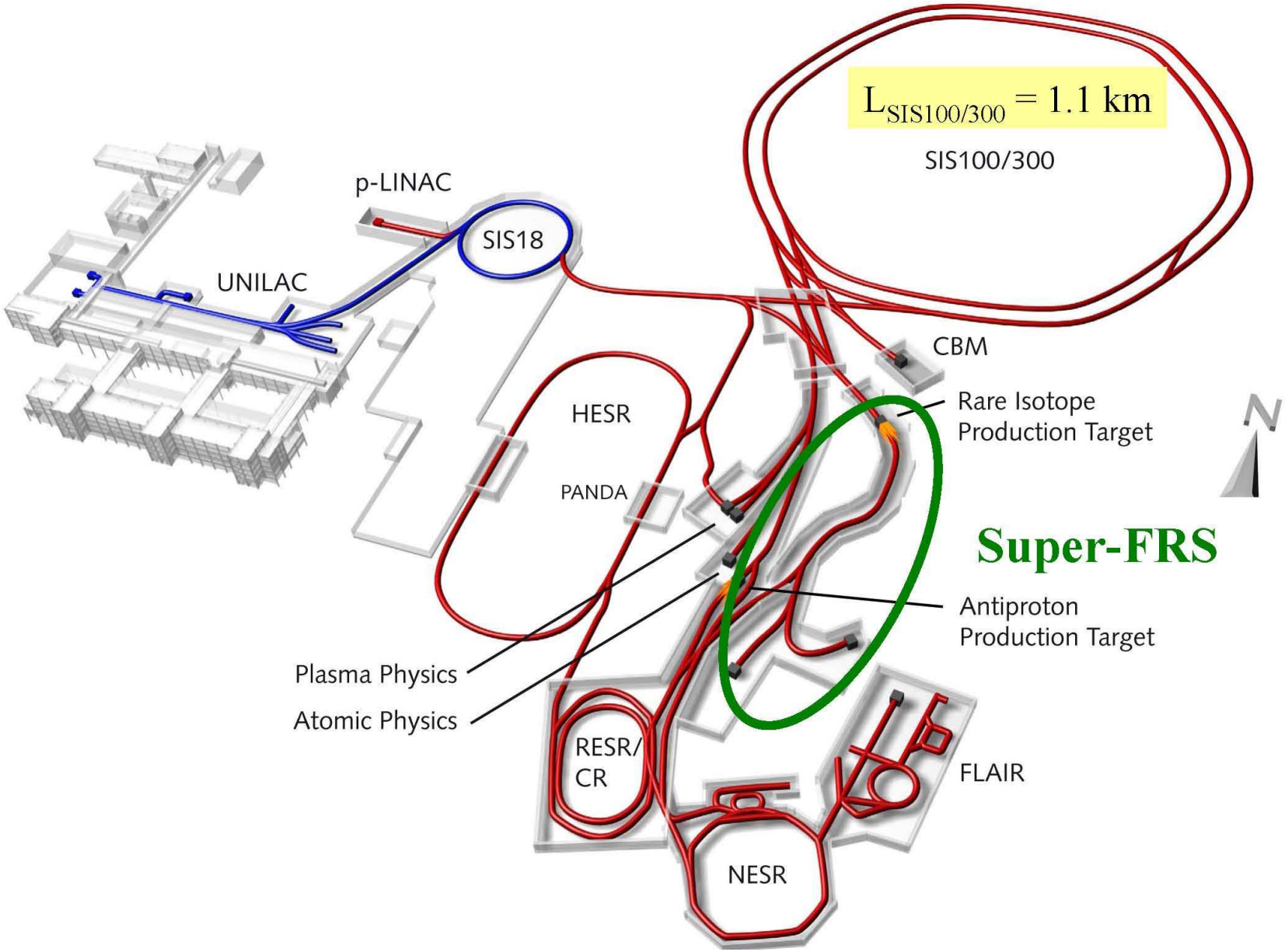
Funded by UK EPSRC/STFC (~£2M)

Collaboration between

University of Liverpool
University of Edinburgh
STFC Daresbury Laboratory
STFC Rutherford Appleton Laboratory

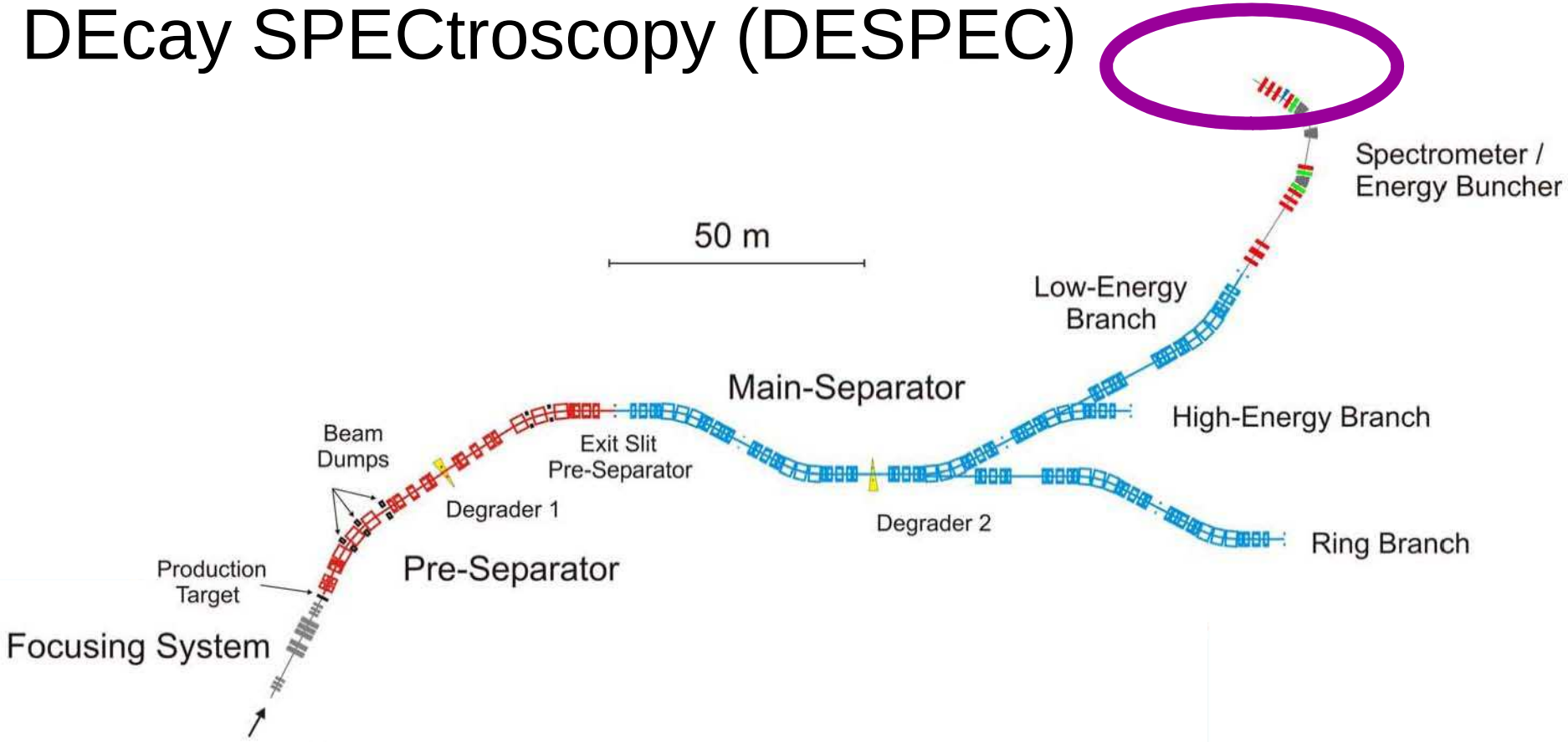
Part of the wider DESPEC collaboration within NUSTAR at GSI/FAIR

FAIR context

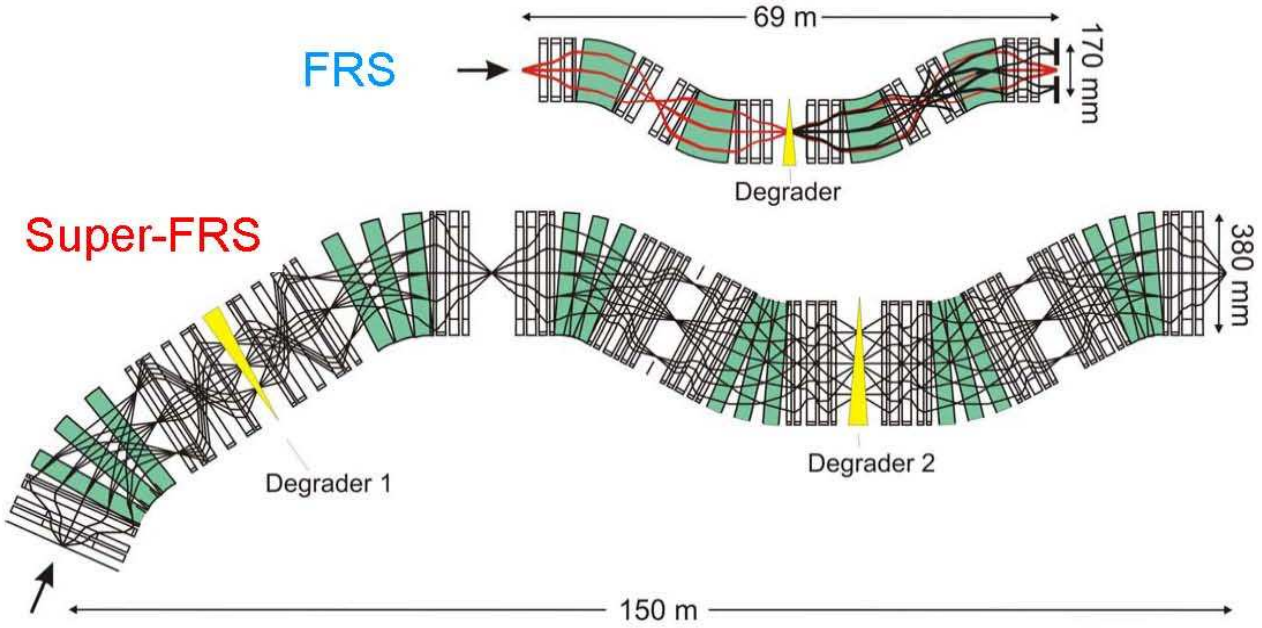


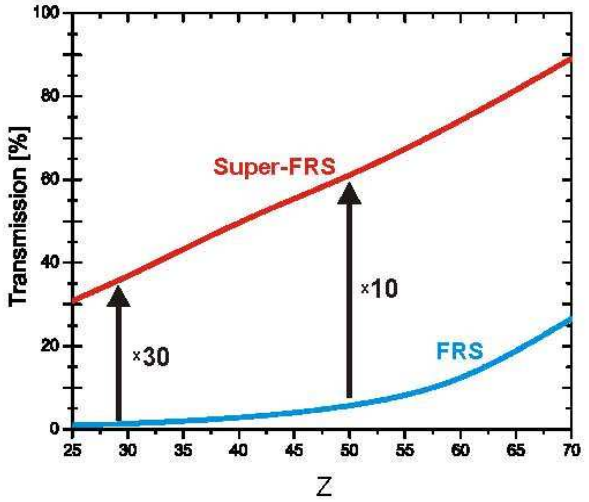
Super FRS

Advanced Implantation Detector Array (AIDA)
DEcay SPECtroscopy (DESPEC)

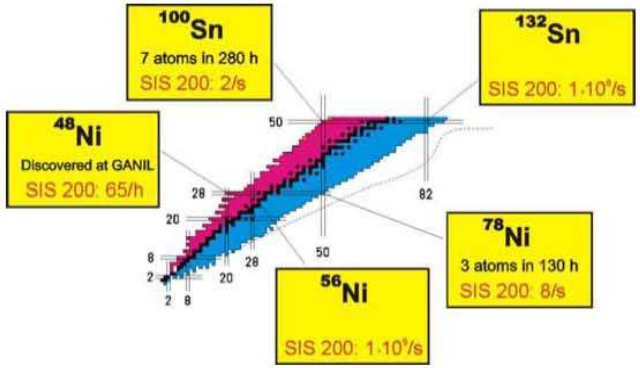


FRS vs. Super FRS



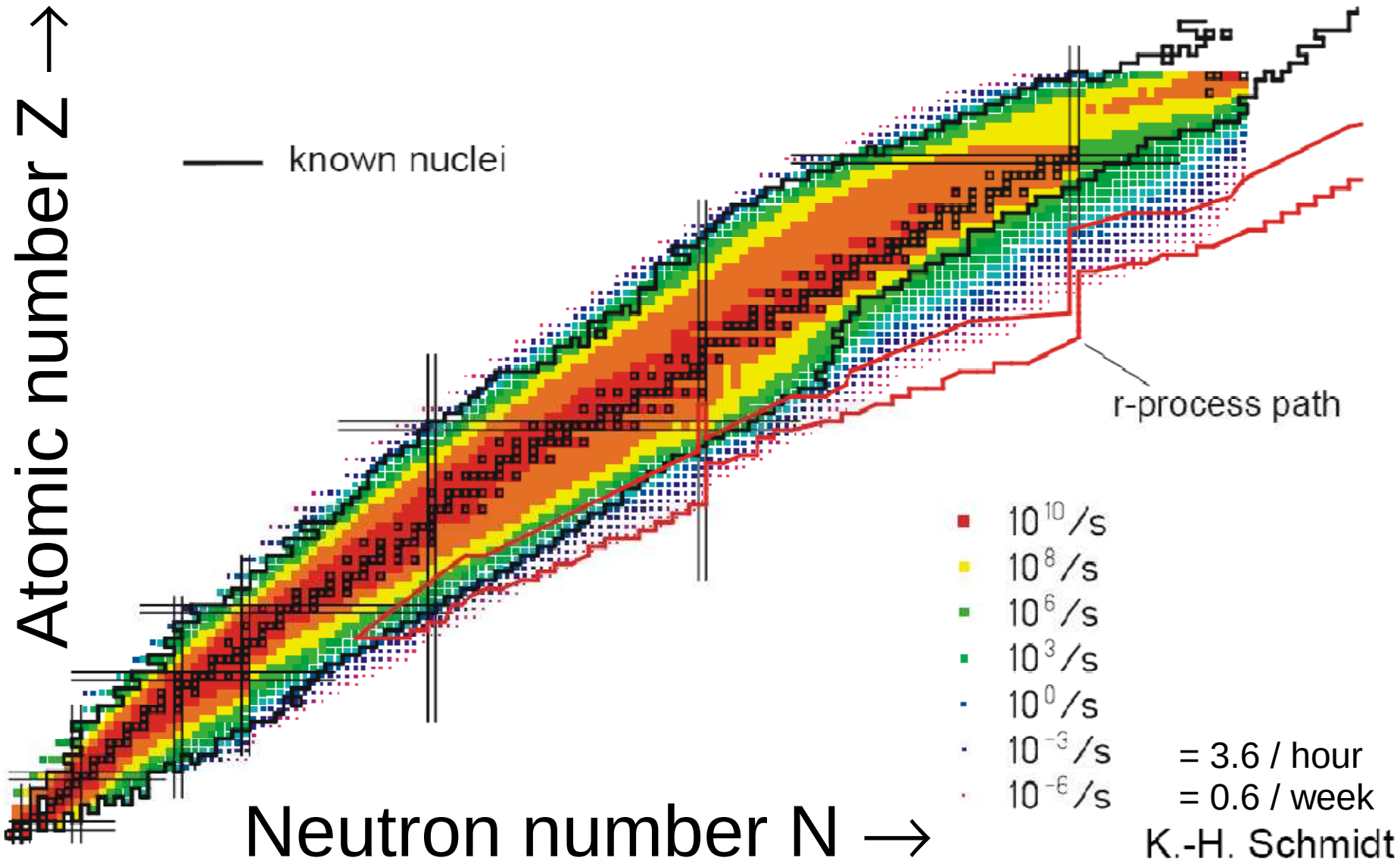


	$B\rho_{max}$	$\Delta p/p$	$\Delta\Phi_x$, $\Delta\Phi_y$	resolving power	gain factor ^{19}C	gain factor ^{132}Sn
FRS	18 Tm	1.0 %	±13, ±13 mrad	1500	1	1
Super-FRS	20 Tm	2.5 %	±40, ±20 mrad	1500	5	10
				including primary rate	250	20 000

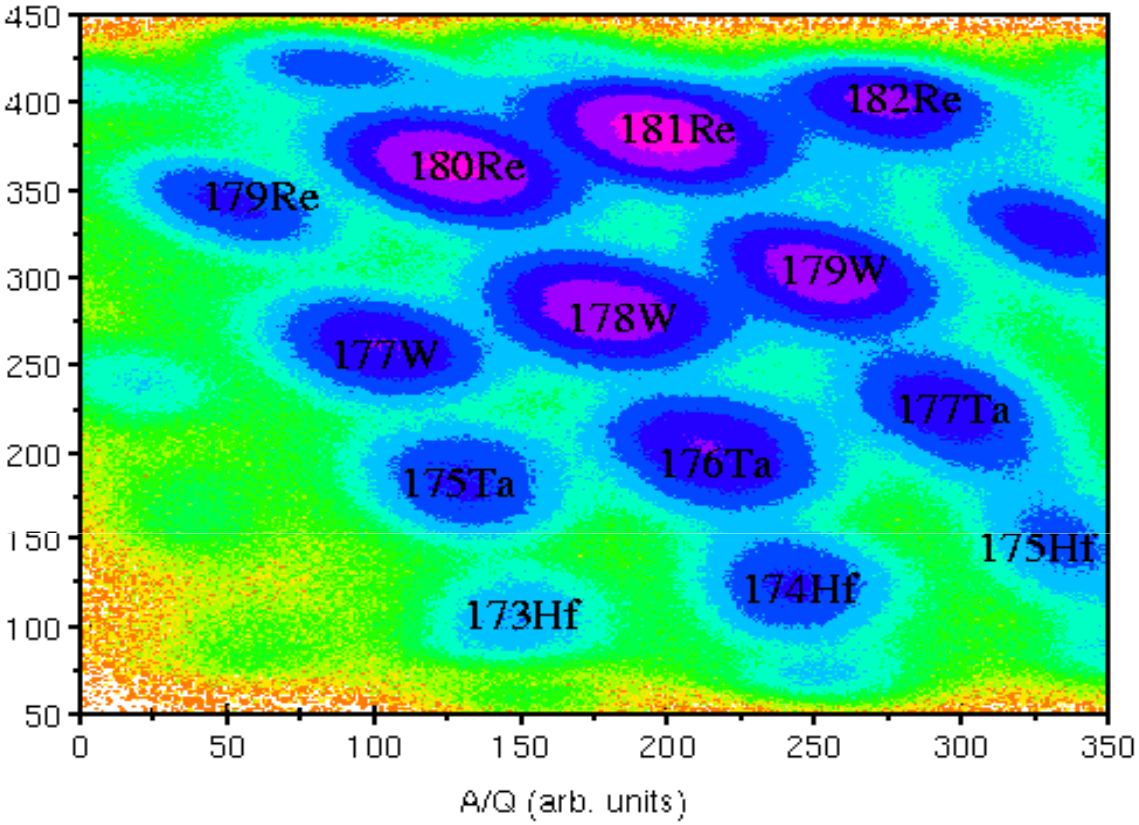


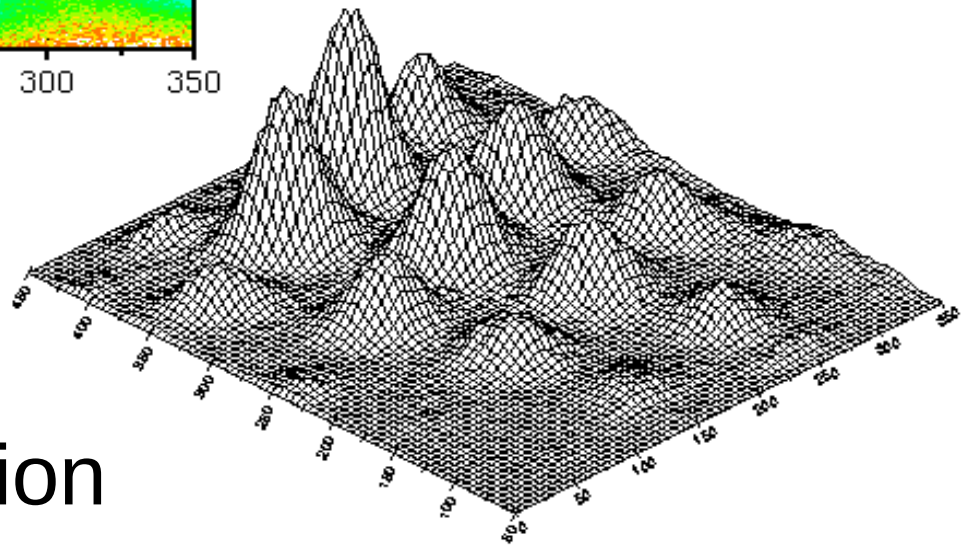
M. Winkler, Artic FIDIPRO-EFES Workshop, April 20-24, 2009, Saariselkä, Finland

Predicted Super FRS Yields @ 10^{12}/s



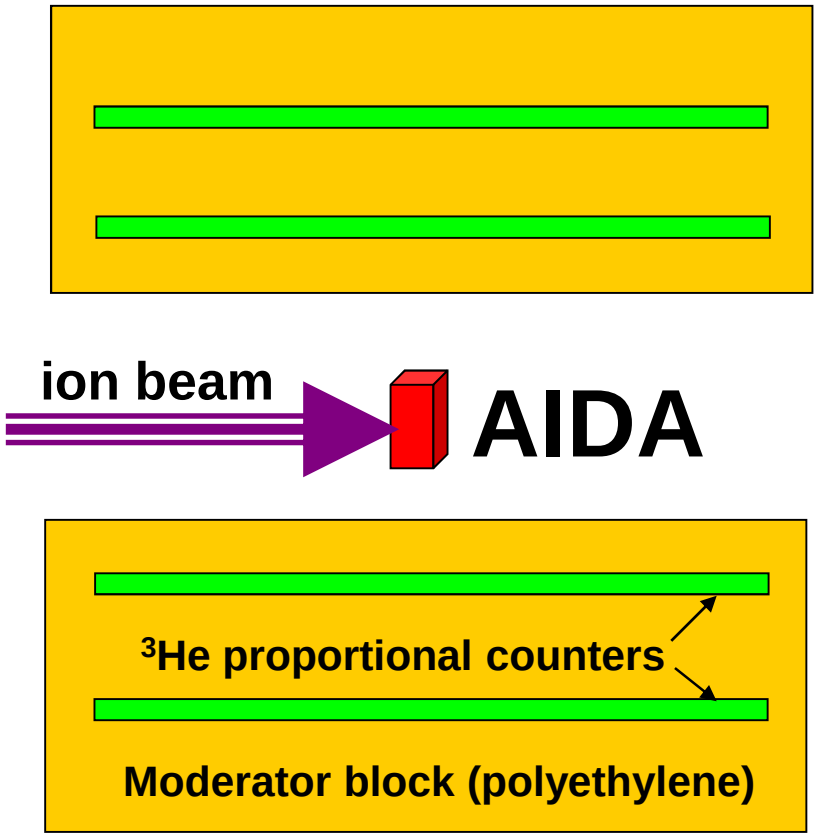
A & Z separation



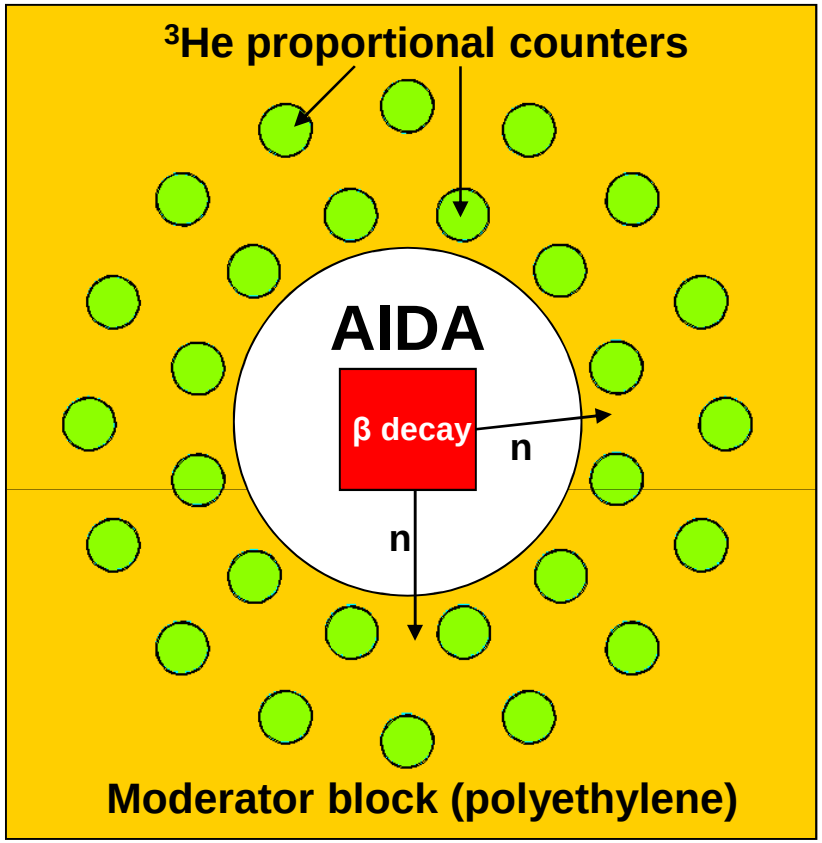


Isomer γ decays for unique A & Z identification

Experimental concept



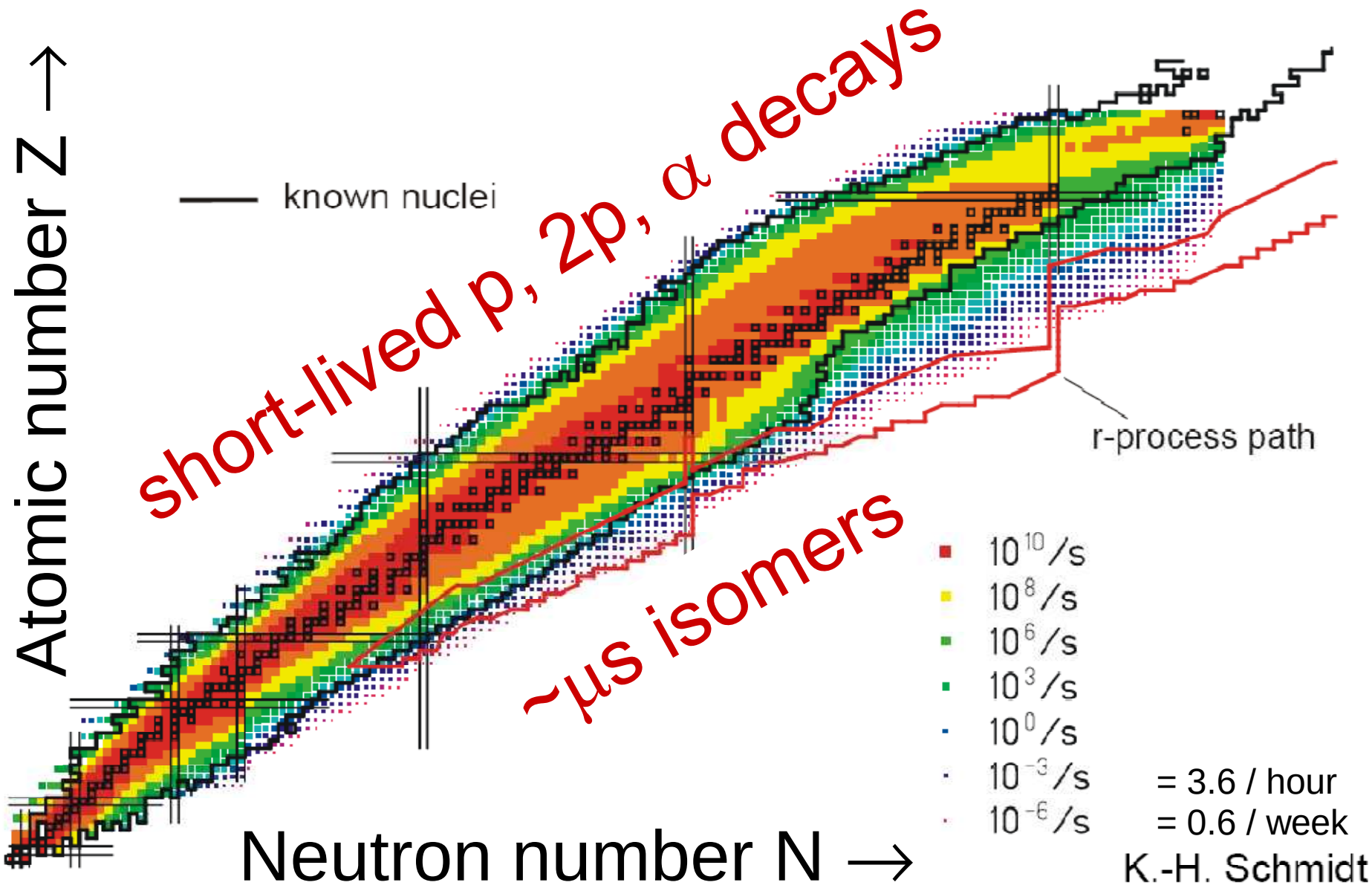
Side view



Front view

Segmented Si detector (DSSD) for ion-β correlations

Predicted Super FRS Yields @ 10^{12}/s

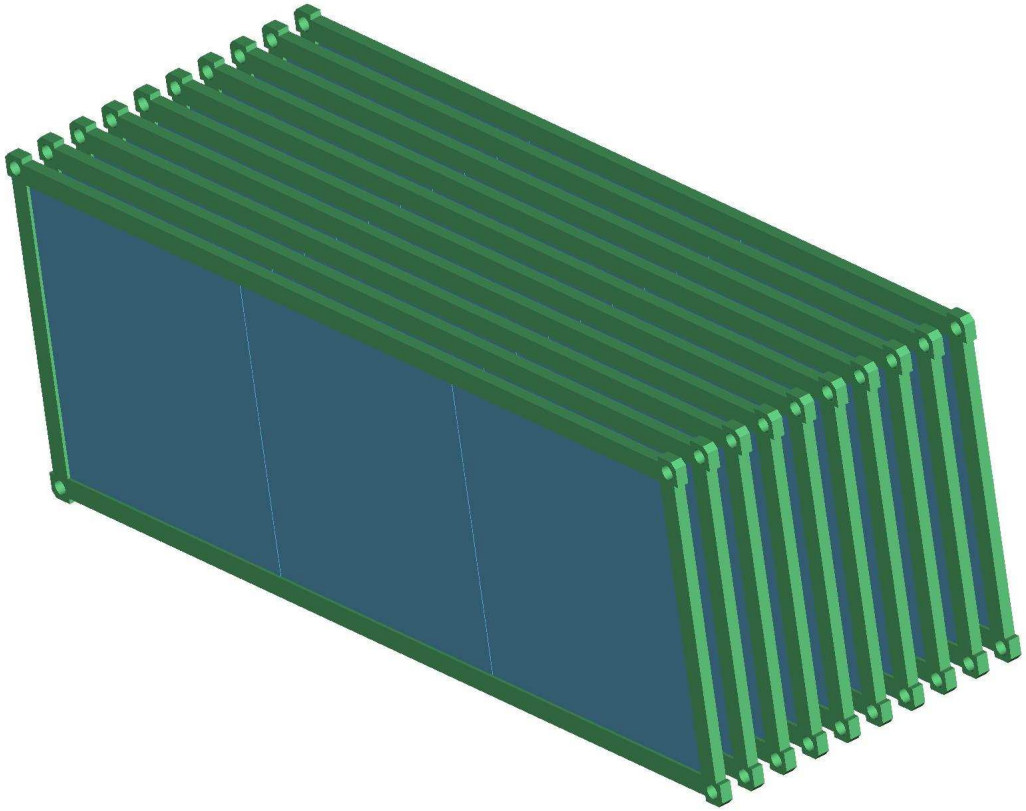


AIDA design – some criteria

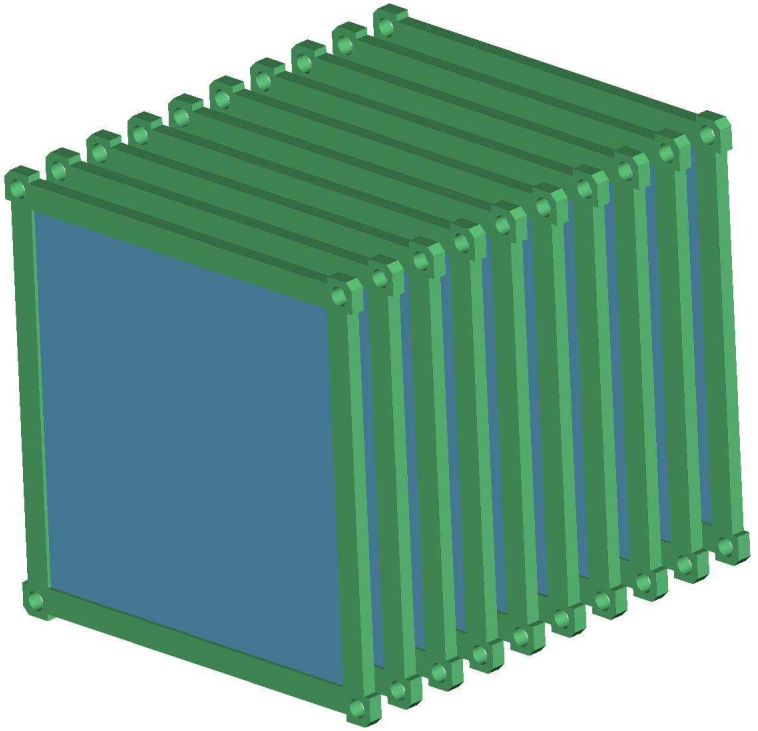
1. Highly segmented for reliable ion-β correlations at high rates
2. Low energy threshold (50 keV) for high β detection efficiency
3. Large energy range to measure ion energies (20 GeV) too!!
4. Many Si planes to stop all ions (~10 mm thickness)
5. Active area to cover (Super) FRS focal plane or single nuclide
6. Compact to fit inside neutron array, RISING Ge array, …
7. Minimum material – n, γ absorption/scattering
8. Good time resolution for n time of flight, …
9. Measure decays within ~μs of ion implantation!
10. Spectroscopic performance for decays

AIDA Design

“standard” configuration
24 cm x 8 cm

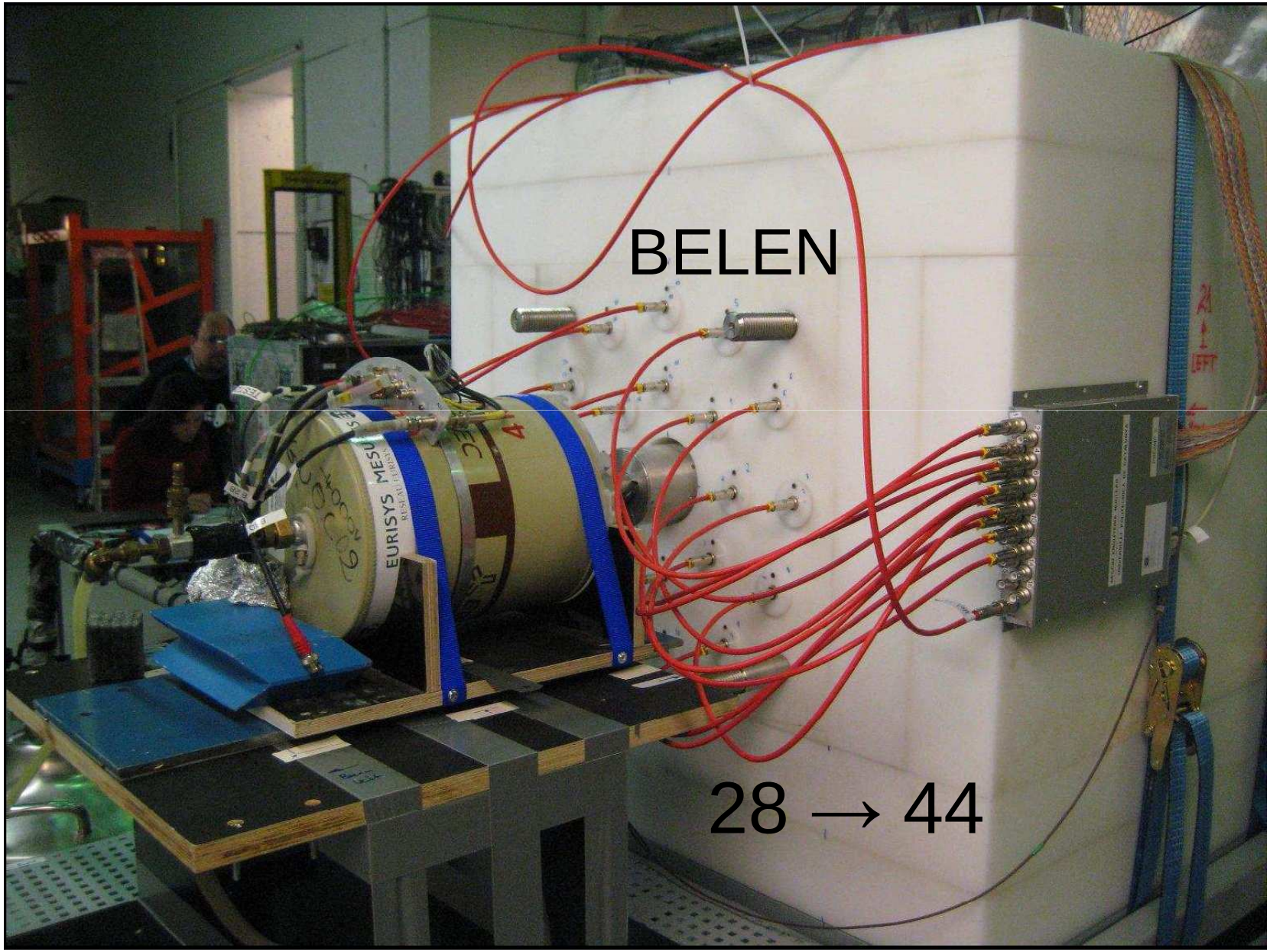


“compact” configuration
8 cm x 8 cm

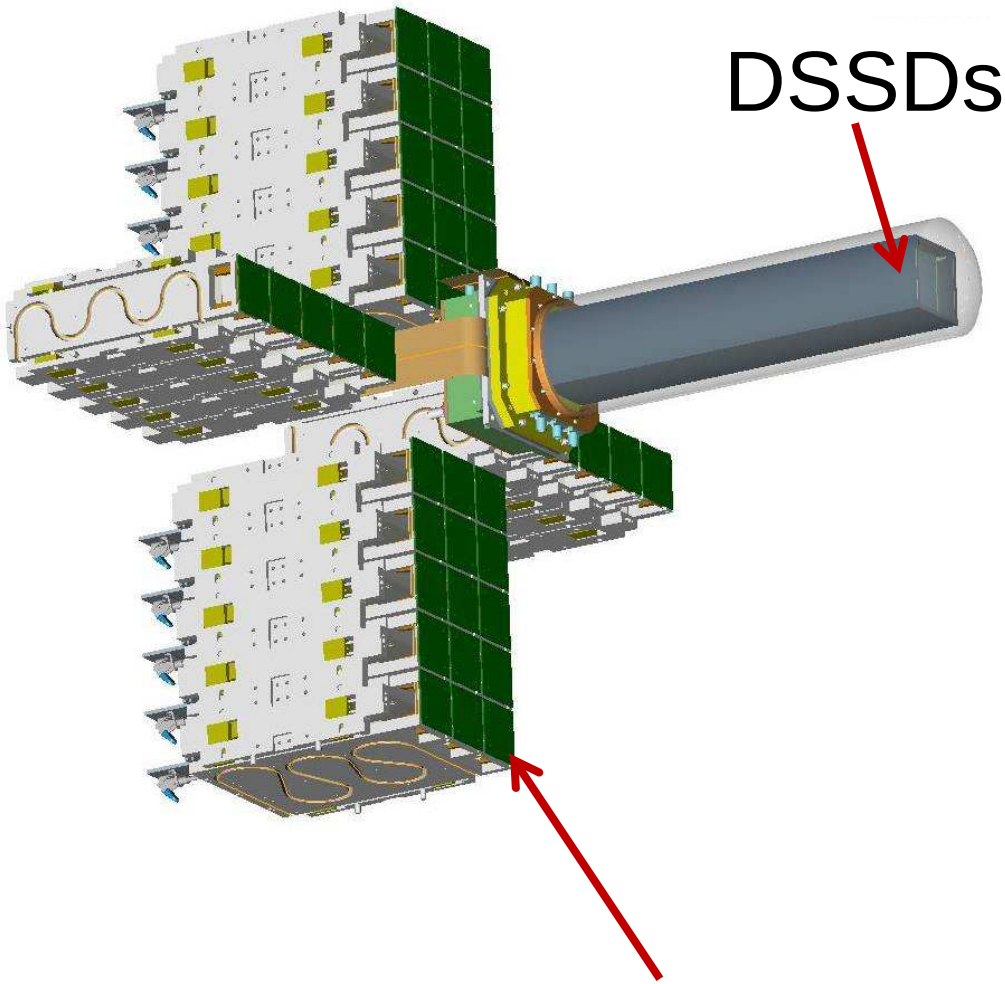


Si thickness = 1 mm, strip pitch = 625 μm, >5000 channels

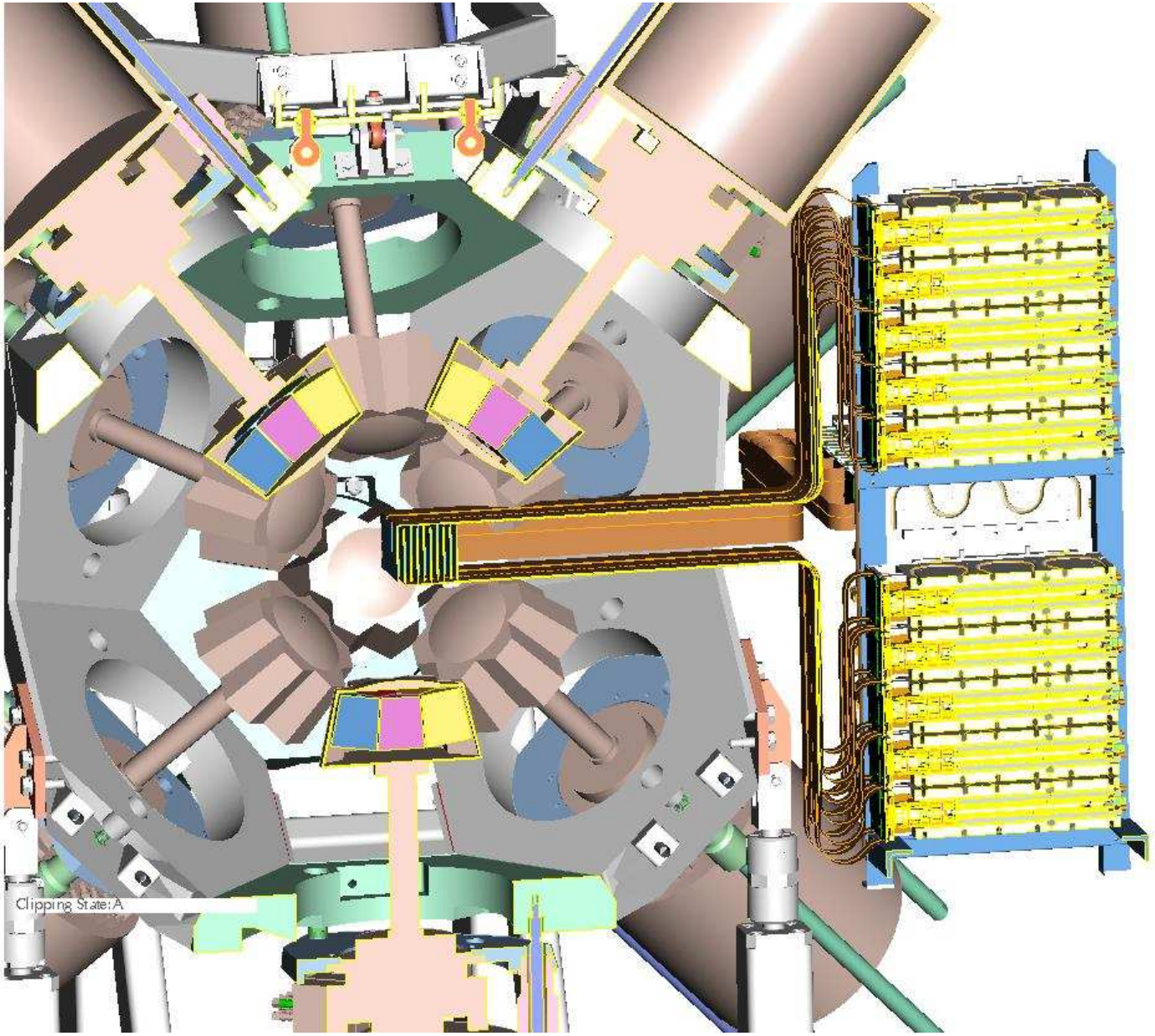
Compatibility with neutron array



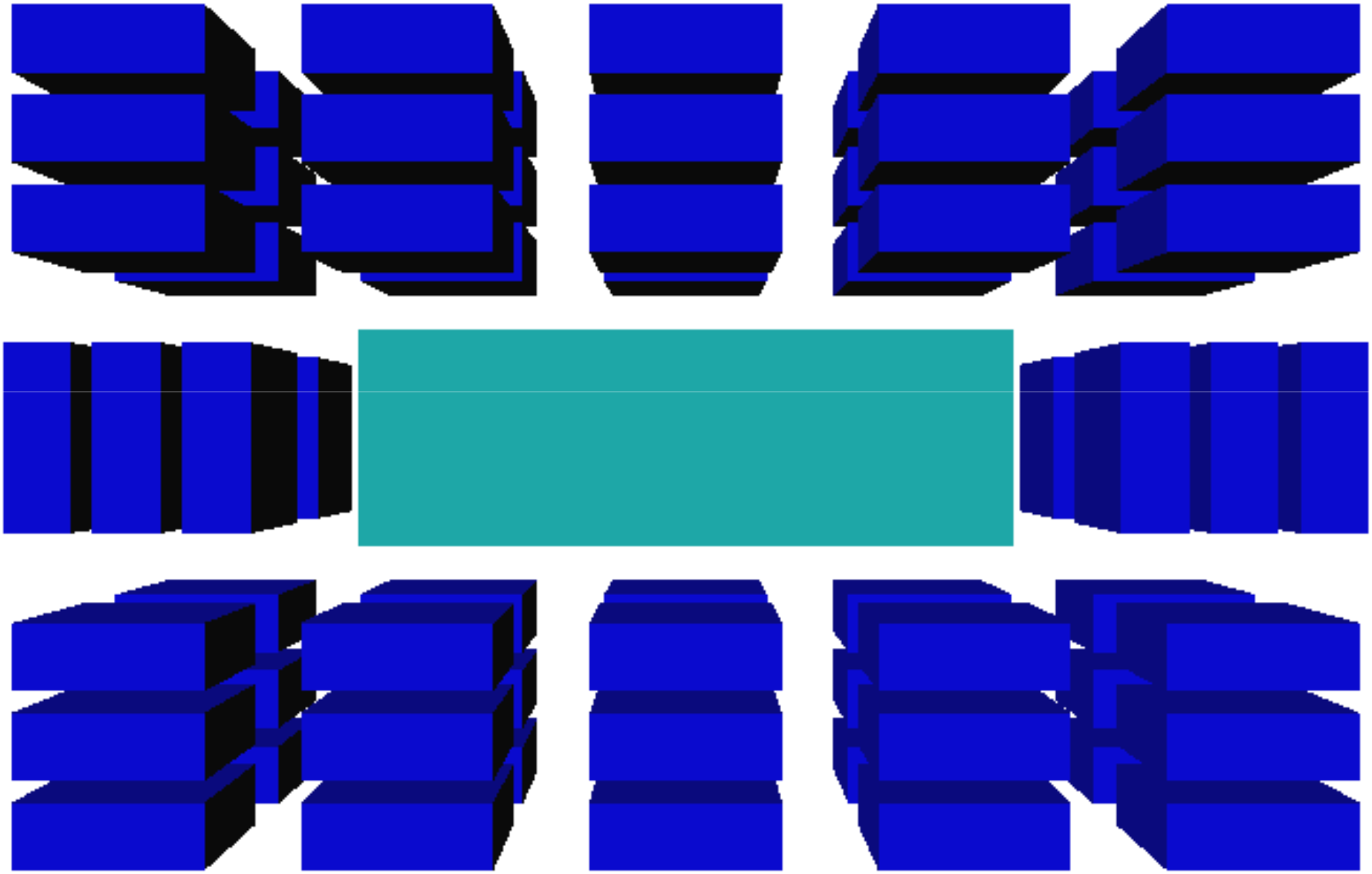
Compact configuration



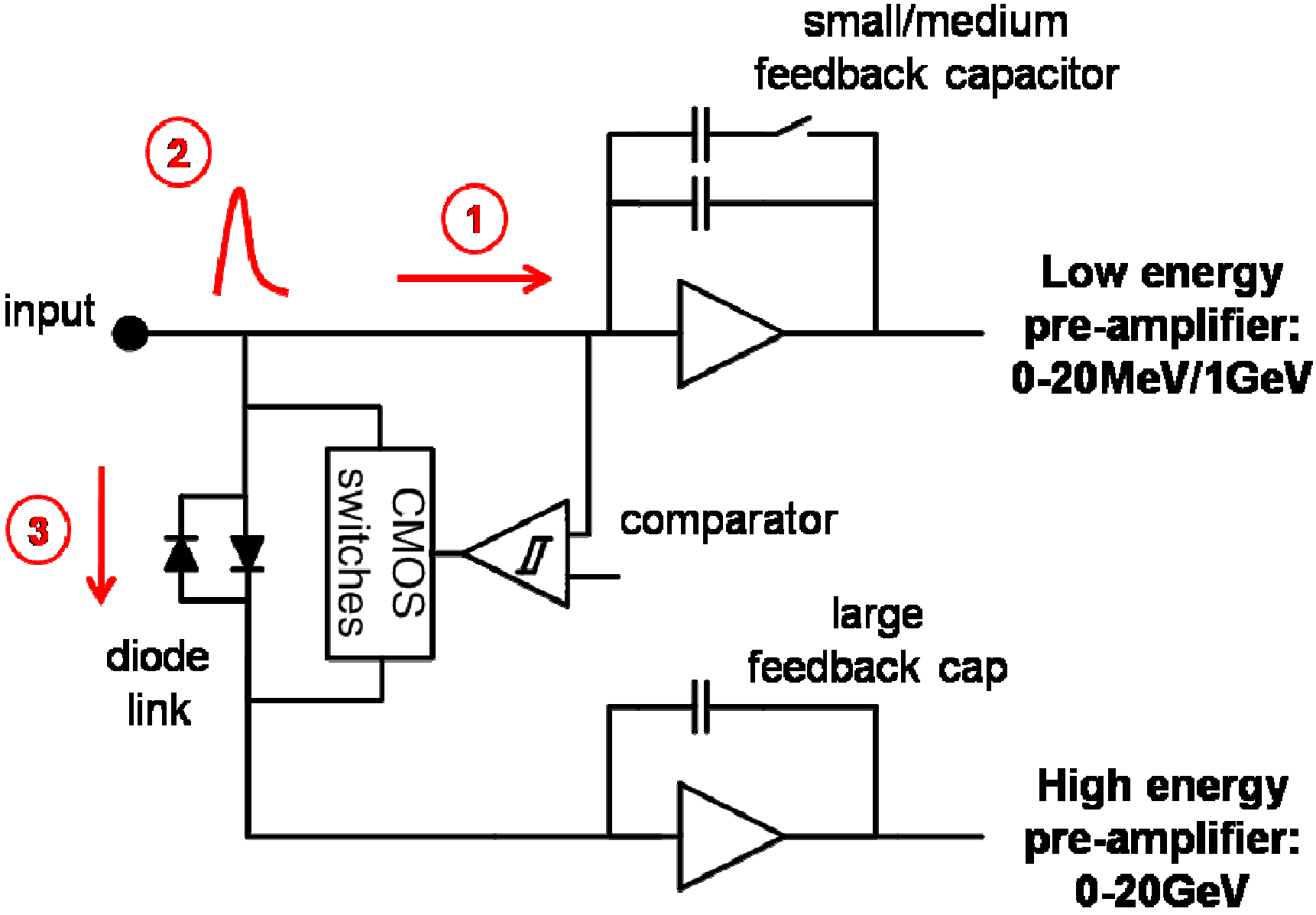
Compatibility with RISING



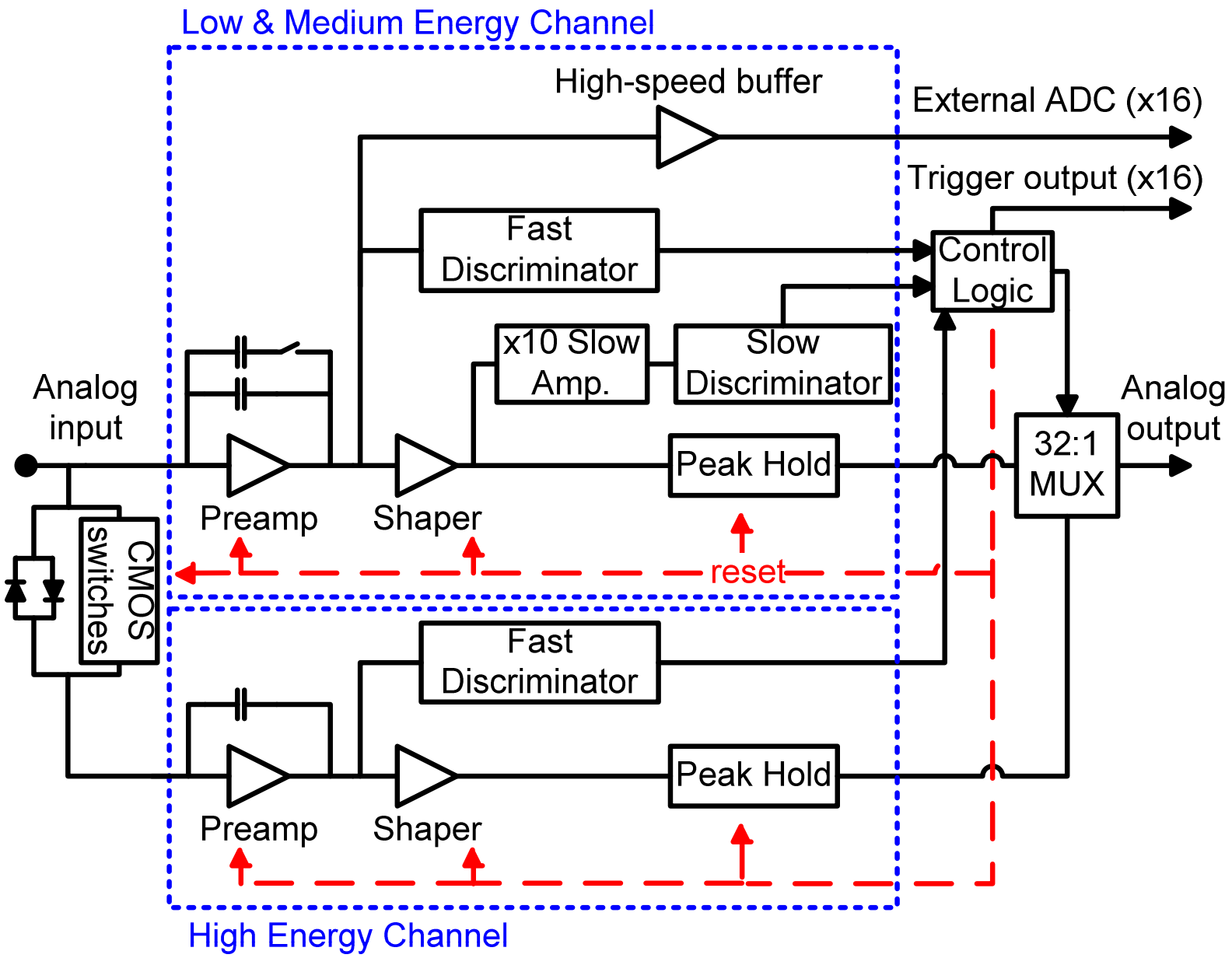
Compatibility with future Ge array



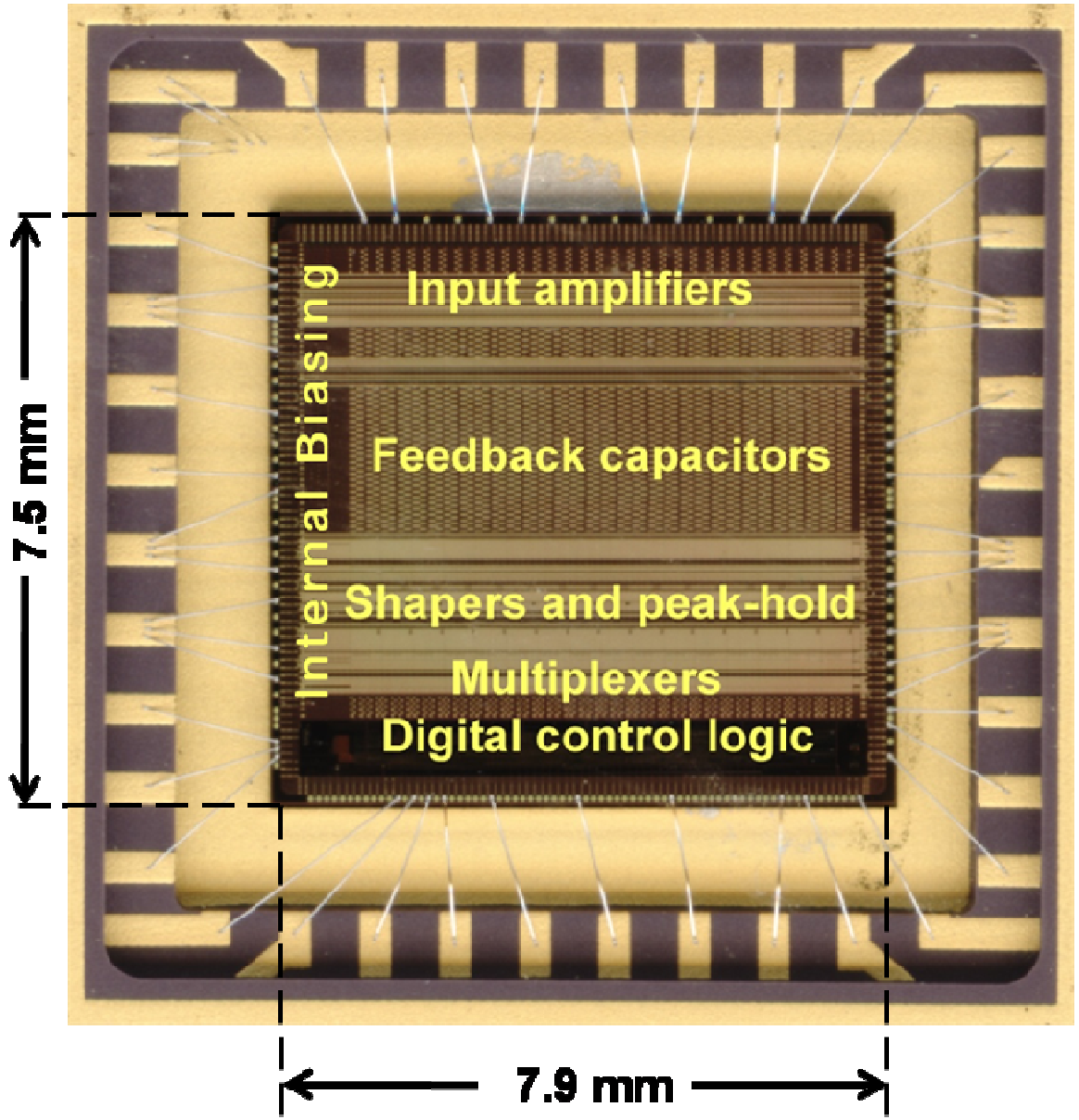
AIDA ASIC Design



AIDA ASIC Design



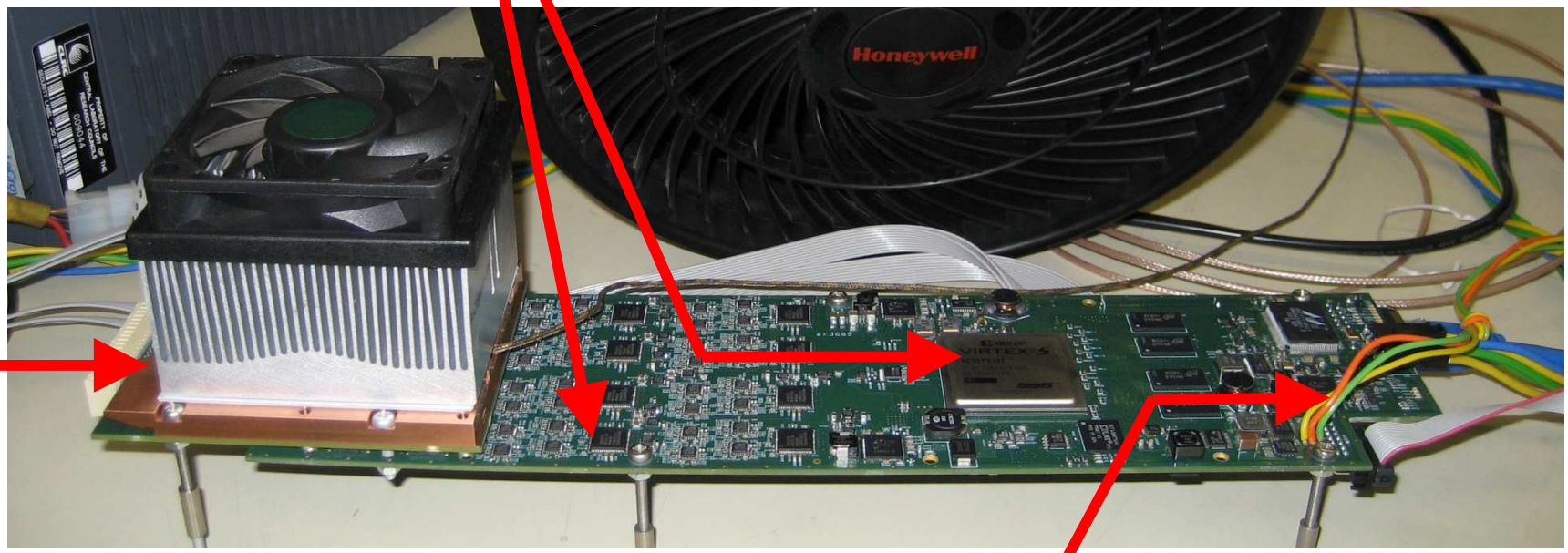
AIDA ASIC


Input amplifiers
Feedback capacitors
Shapers and peak-hold
Multiplexers
Digital control logic
Internal Biasing
7.5 mm
7.9 mm

AIDA ASIC & readout

Mezzanine card:
- 4x 16 channel ASICs
- Cu cover
  - EMI/RFI/light screen
  - cooling

FEE card:
- 4x 16-bit ADC MUX readout (not visible)
- 8x octal 50MSPS 14-bit ADCs
- Xilinx Virtex 5 FPGA
- PowerPC 40x CPU core – Linux - MIDAS



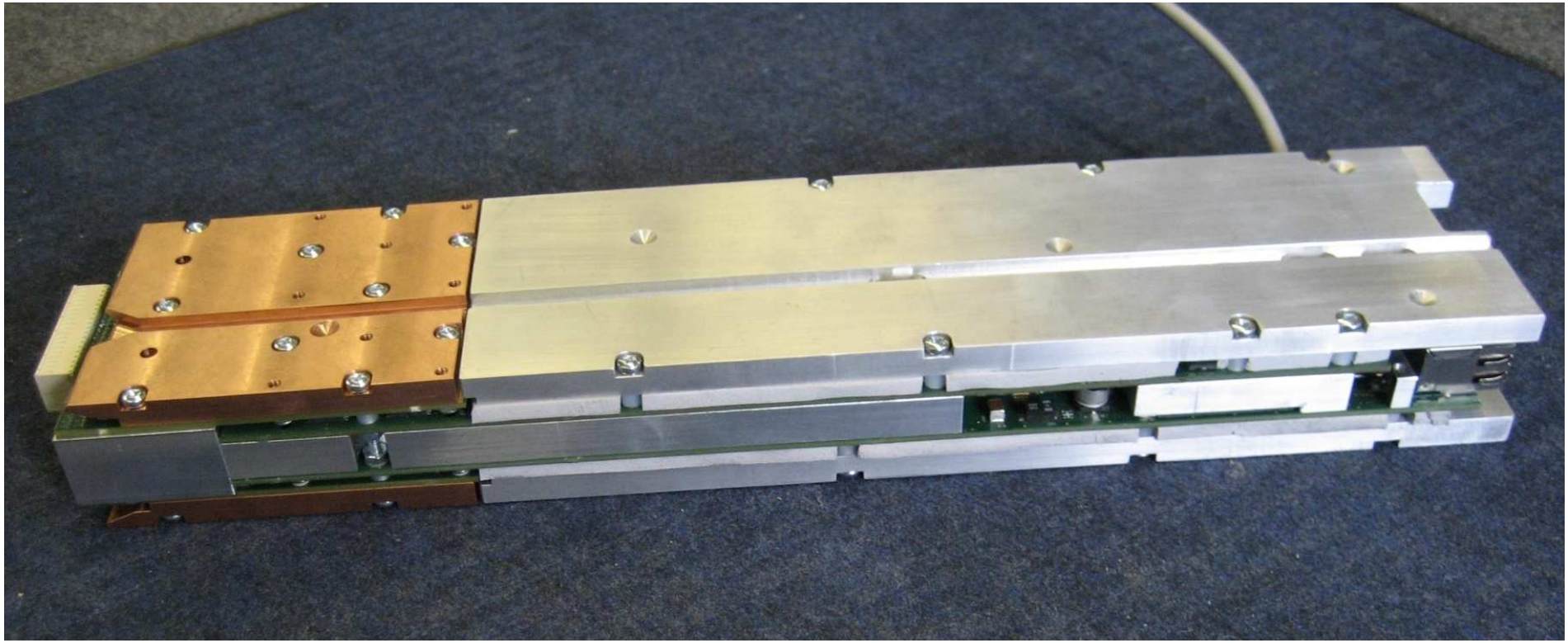
FEE card width: 8cm

Prototype – air cooling

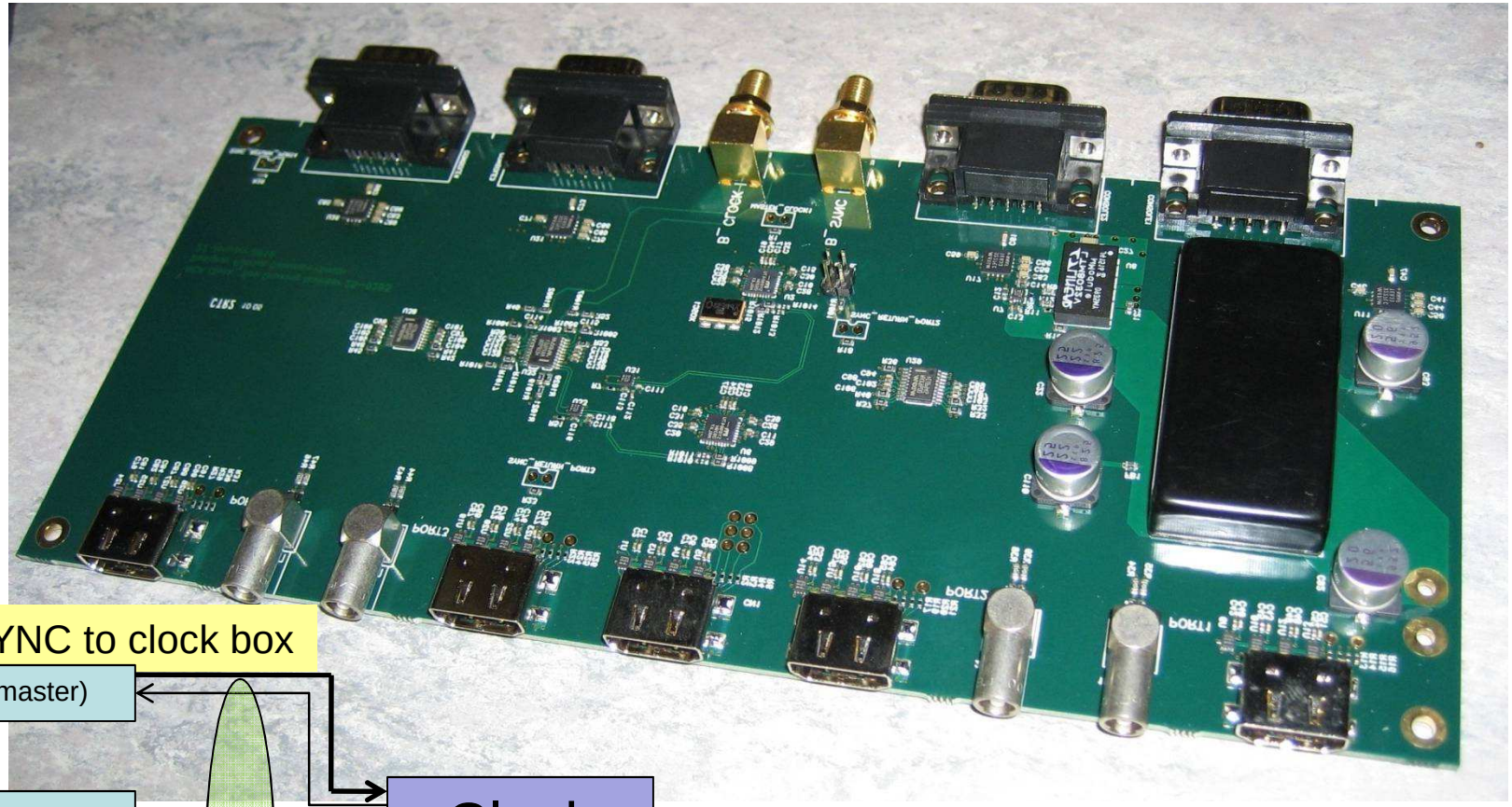
Production – recirculating coolant

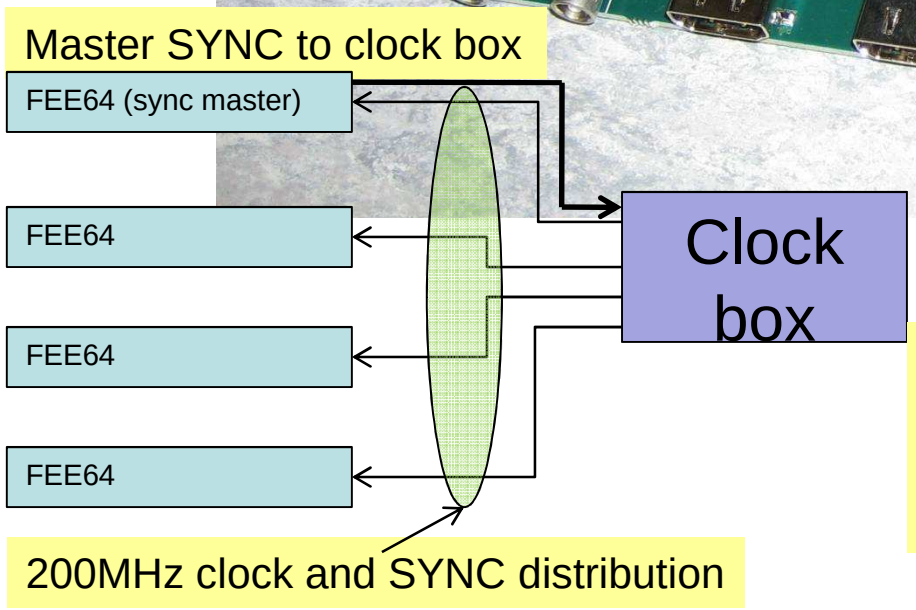
Gbit ethernet, clock, JTAG ports, power

Packaged AIDA FEE cards



AIDA clock box





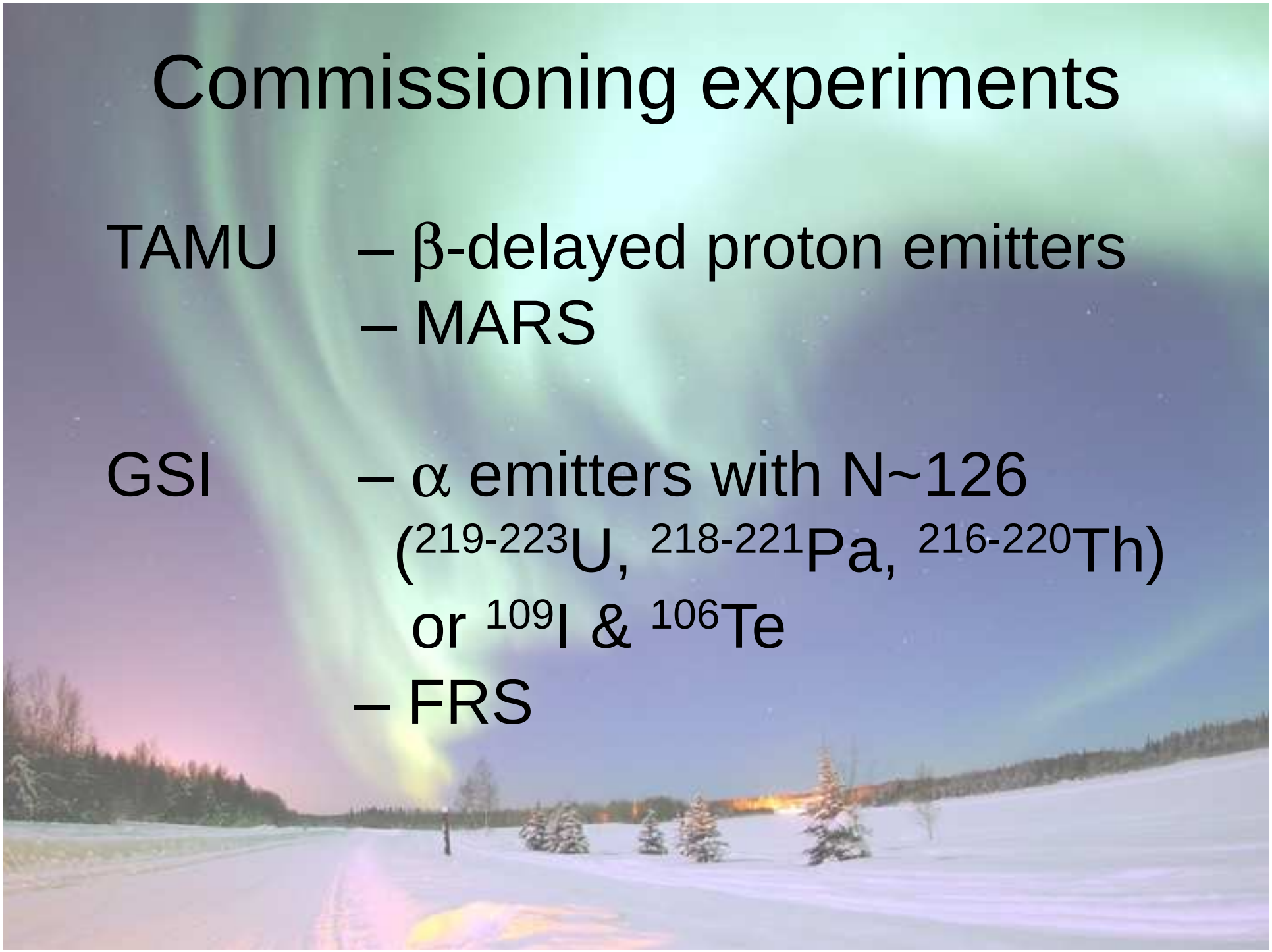
For operating >1 AIDA FEE64

Module may be cascaded

Commissioning experiments

TAMU – β-delayed proton emitters
– MARS

GSI – α emitters with N~126
($^{219\text{-}223}$U, $^{218\text{-}221}$Pa, $^{216\text{-}220}$Th)
or ^{109}I & ^{106}Te
– FRS



Status Summary

Mechanical assembly of prototype complete

Thermal tests of DSSD cooling ongoing

Bench tests of ASICs, FEE cards ongoing
pulsers $\rightarrow$ electron sources

Commissioning experiments soon (?)

First experimental proposals to GSI PAC

Further information: http://www.ph.ed.ac.uk/~td/AIDA

Collaborators

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