CLOCK / SYNC Distribution mCBM

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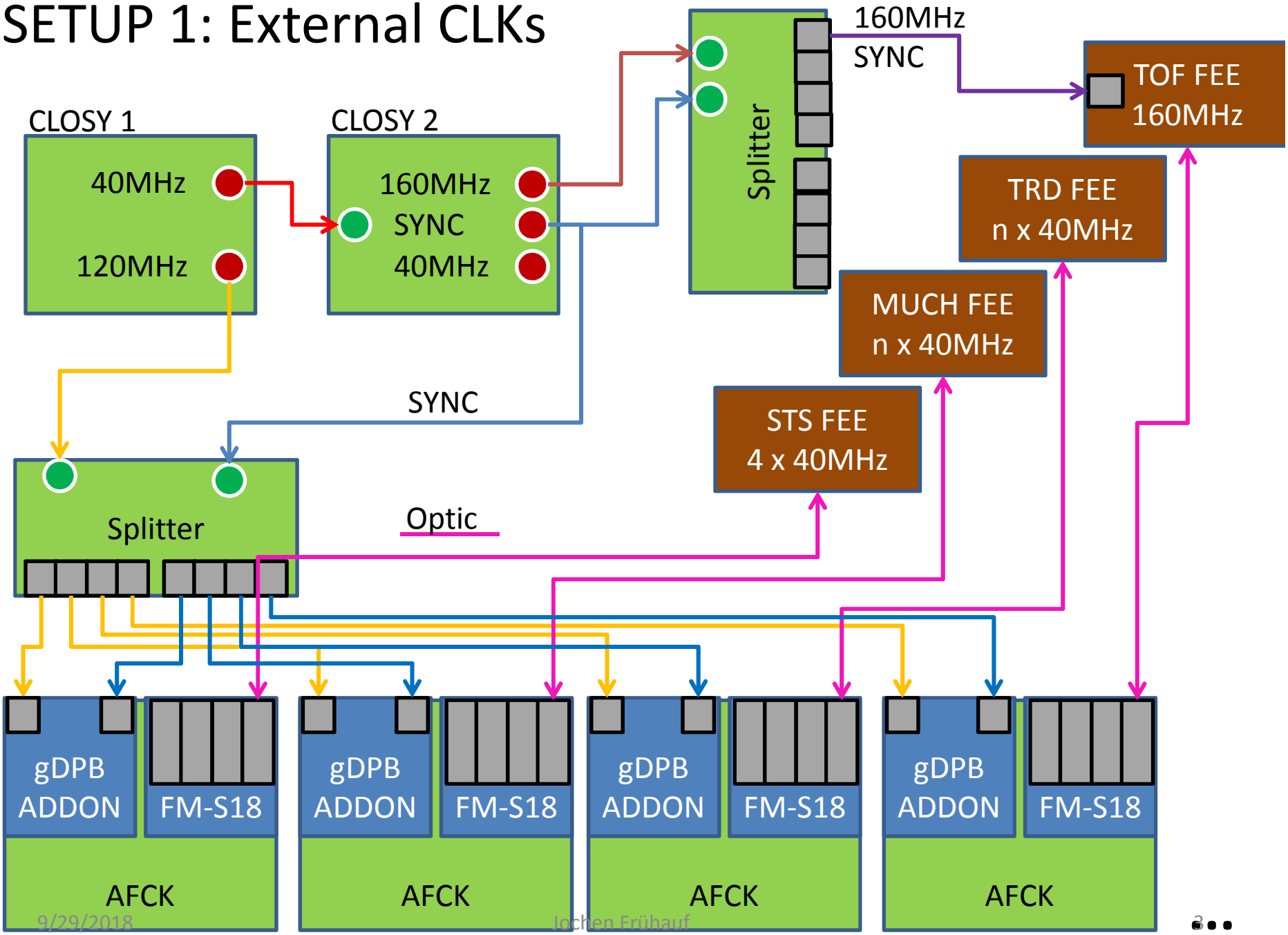
Needed Clocks

- 40MHz for AFCK Logic
- 120MHz for GBTx Logic
- 160MHz for TOF FEE
- n x 40MHz CLK for STS/MUCH and TRD
  - recovered from the optical link CLK of the GBTx

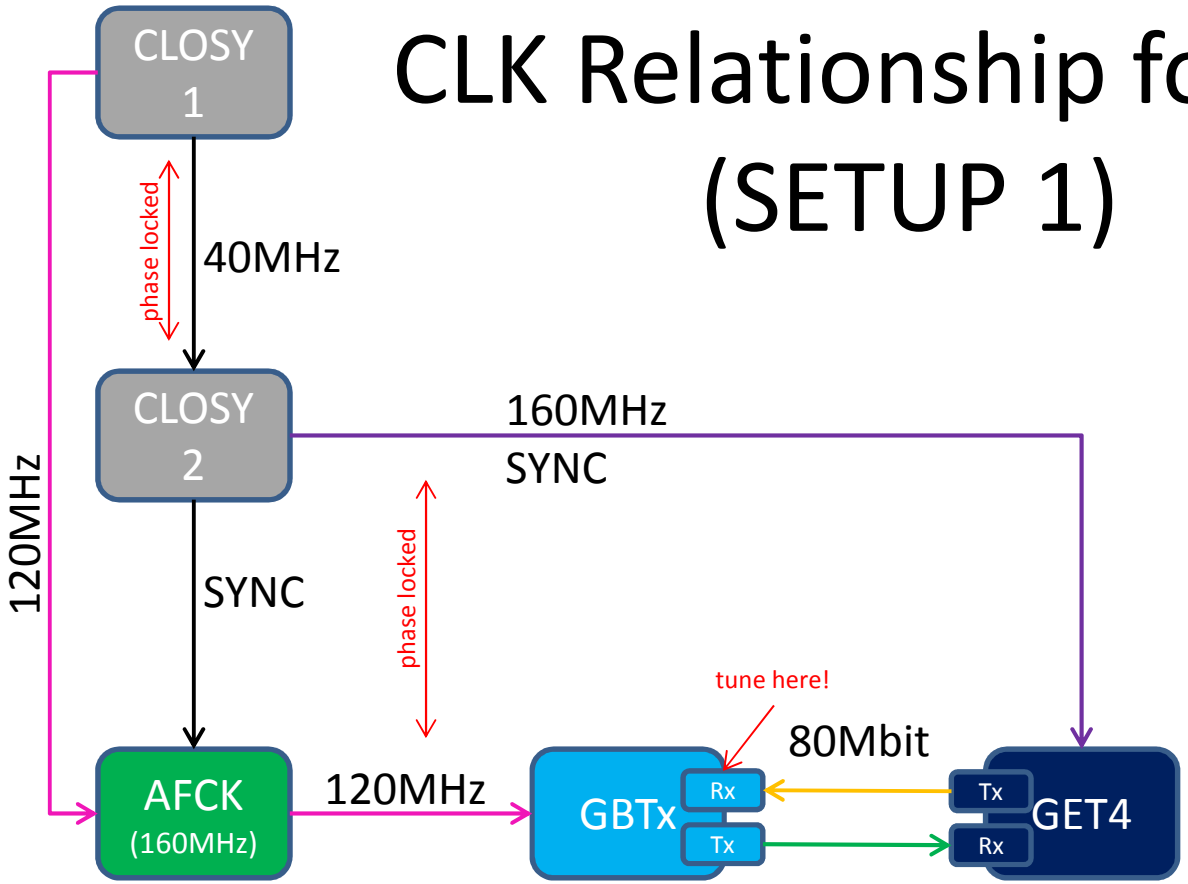
- SYNC Pulse for AFCK and ToF-FEE

120MHz for GBTx needs to be phase locked to the 40MHz/160MHz for ToF to guarantee a synchronous data taking between subsystems

SETUP 1: External CLKs



CLK Relationship for ToF (SETUP 1)

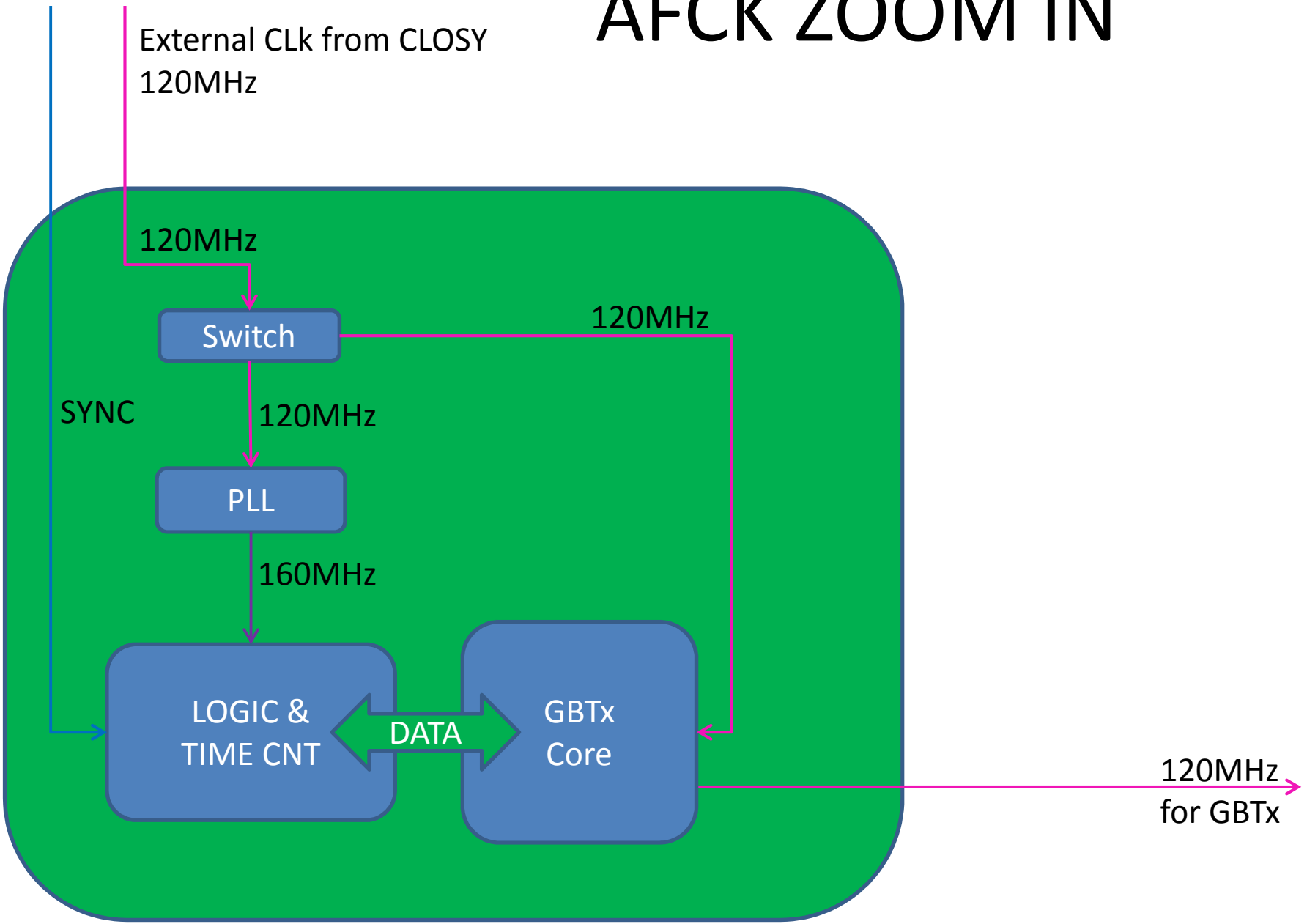


Only one point to tune!
All other relationships are given by cable delays and fix for a given setup

be carful:
120MHz and 160MHz are phase locked to each other but the phase can change after each power cycle of
- CLOSY
- GBTx Core Reset (FPGA)

CLOSY1: 120MHz & 40MHz phase locked
CLOSY2: 160MHz phase locked to 40MHz from CLOSY1
AFCK: 120MHz from CLOSY1 for GBTx and generate 160MHz for logic
GBTx: 120MHz from AFCK = Phase locked to CLOSY2 160MHz for GET4
GET4: 160MHz from CLOSY2 = Phase locked to 120MHz from CLOSY1 = Phase locked to 120MHz for GBTx
GET4 Rx use 4 times oversampling
GET4 Tx needs to be “phase controlled” on the GBTx side

AFCK ZOOM IN


External CLk from CLOSY
120MHz
120MHz
Switch
120MHz
SYNC
120MHz
PLL
160MHz
LOGIC &
TIME CNT
DATA
GBTx
Core
120MHz
for GBTx

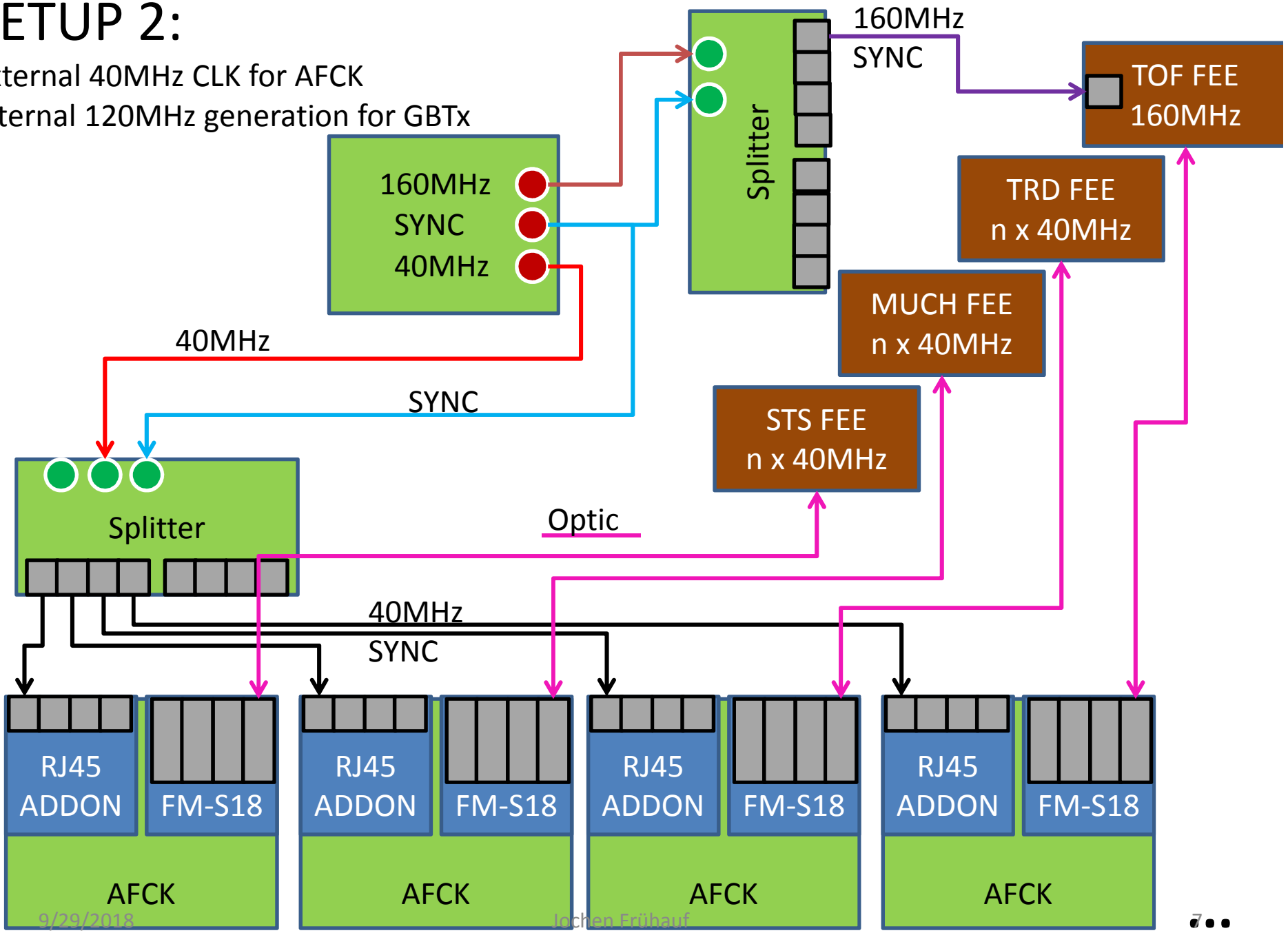
SETUP 1: External CLK generation

1. CLOSY1 Generate 120MHz and 40MHz
   - 120MHz for AFCK/GBTx
   - 40MHz for CLOSY 2
2. CLOSY2 generates phase locked to 40MHz from CLOSY1:
   - 160MHz for ToF FEE
   - SYNC for AFCK and ToF FEE
3. AFCK generate phase locked 40MHz for logic out of 120MHz from GBTx Core

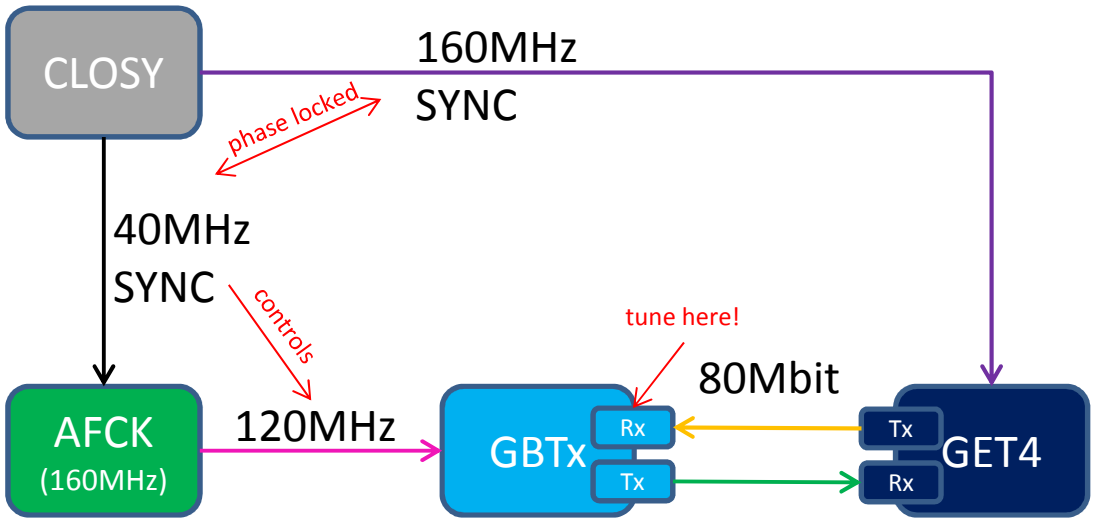
CLK for FEE (except ToF FEE) from GBTx

SETUP 2:

External 40MHz CLK for AFCK
Internal 120MHz generation for GBTx



CLK Relationship for ToF (SETUP 2)

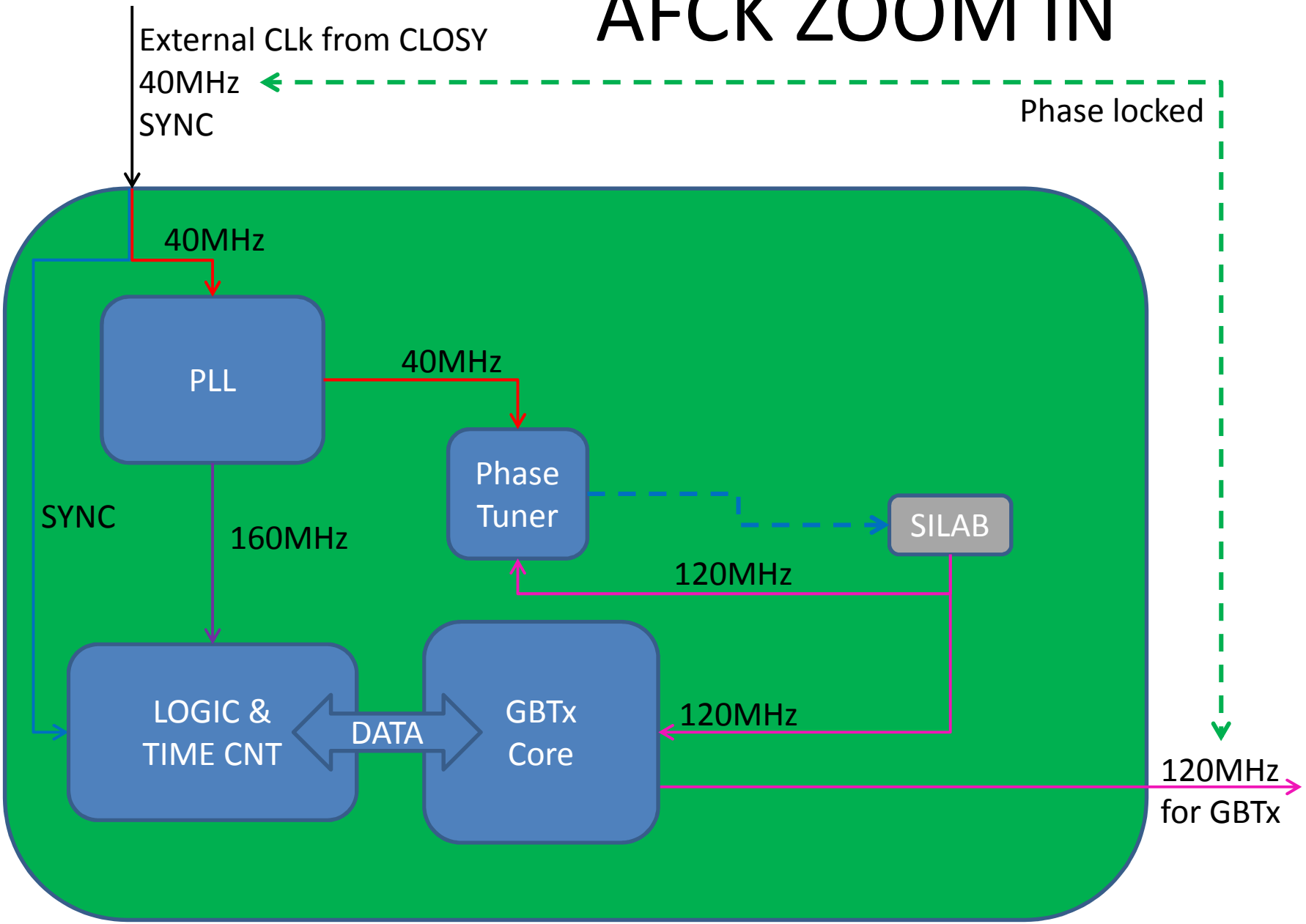


Only one point to tune!
All other relationships are given by cable delays and fix for a given setup

be carful:
120MHz and 160MHz are phase locked to each other but the phase can change after each power cycle of
- CLOSY
- AFCK
- GBTx Core Reset (FPGA)

CLOSY: 160MHz & 40MHz phase locked
AFCK: 40MHz from CLOSY to control 120MHz for GBTx and generate 160MHz for logic
GBTx: 120MHz from AFCK = Phase Controlled by 40MHz from CLOSY
GET4: 160MHz from CLOSY = Phase locked to 40MHz for AFCK = Phase locked to 120MHz for GBTx
GET4 Rx use 4 times oversampling
GET4 Tx needs to be “phase controlled” on the GBTx side

AFCK ZOOM IN


External CLk from CLOSY
40MHz
SYNC
Phase locked
40MHz
PLL
40MHz
Phase
Tuner
SILAB
SYNC
160MHz
120MHz
LOGIC &
TIME CNT
DATA
GBTx
Core
120MHz
120MHz
for GBTx

SETUP 2: Internal 120MHz generation

- synchronize Si570 on FM-S18 with PLL design as it's done in “White Rabbit 2”
- external 40MHz from CLOSY will be the reference CLK for this solution

  (suggested by Adrian Byszuk)

CLK for FEE (except ToF FEE) from GBTx