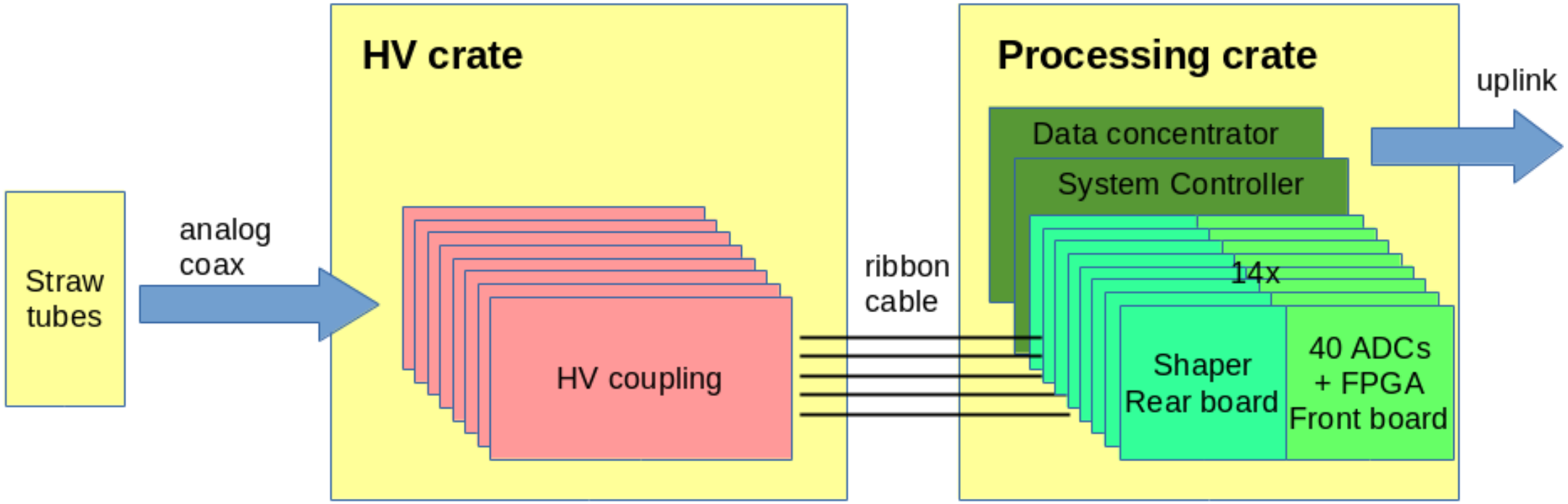
STATUS OF ADC BASED DAQ FOR PANDA STT

PANDA COLLABORATION MEETING

6. JUNE 2018 I A. ERVEN, L. JOKHOVETS

SYSTEM OVERVIEW



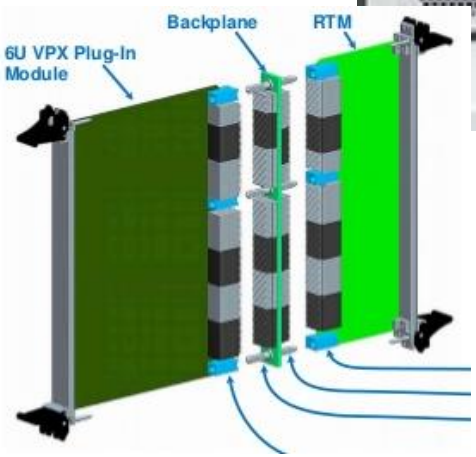
480 straw tubes

„Samtec cable“

CRATE

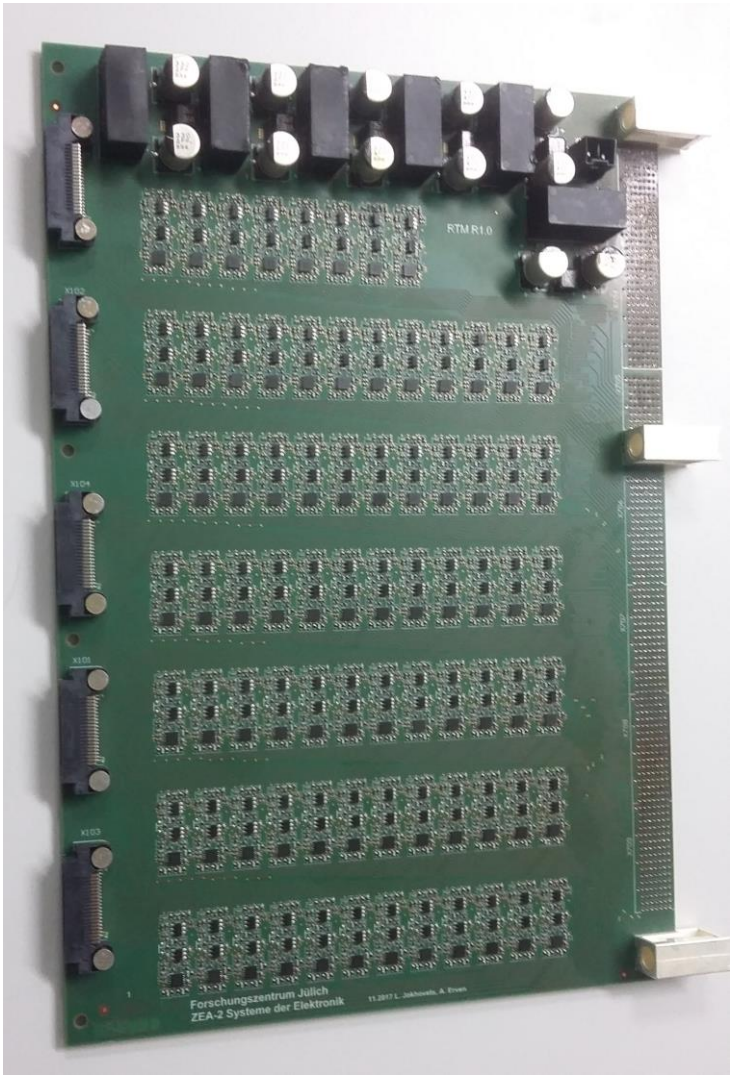
- Initial planning was based on ATCA standard, but changed to openVPX standard
- Advantages
  - Introduction of Rear Transition Module (RTM) allows separation of analog and digital part

    → independent development
  - Highspeed Board-to-Board and Controller-to-Board communication
  - Enough connections for RTM-communication
  - Compact boards for short signal lines to backplane and ADC
  - Backplane adapted to our needs and crates produced by ELMA (very smooth development)



REAR TRANSITION MODULE

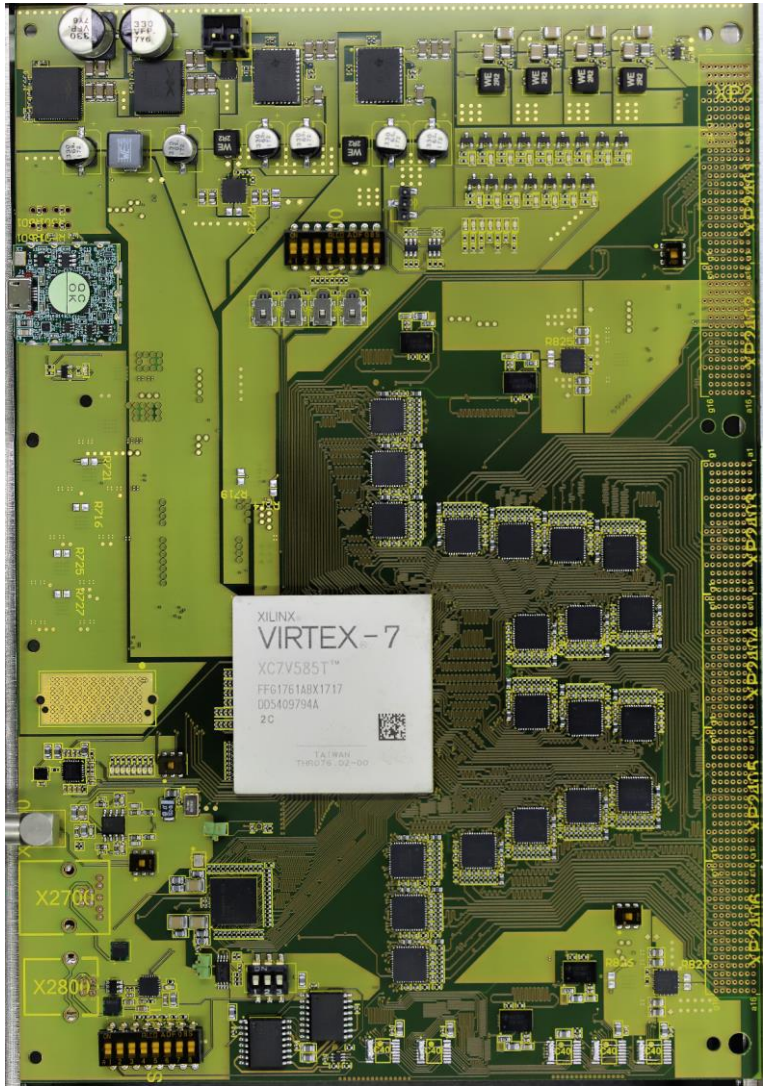
- Amplifier stages for 160 channels per board
- 5 input connectors for samtec cables (32 channels each)
- After receiving modules, error in layout was realized
- Found workaround for test, modules were usable with limitations
- Fix for further productions is done by external provider
- Slight revision of power supply needed
- Add contact area to ground plane for shielding



PROCESSING BOARD

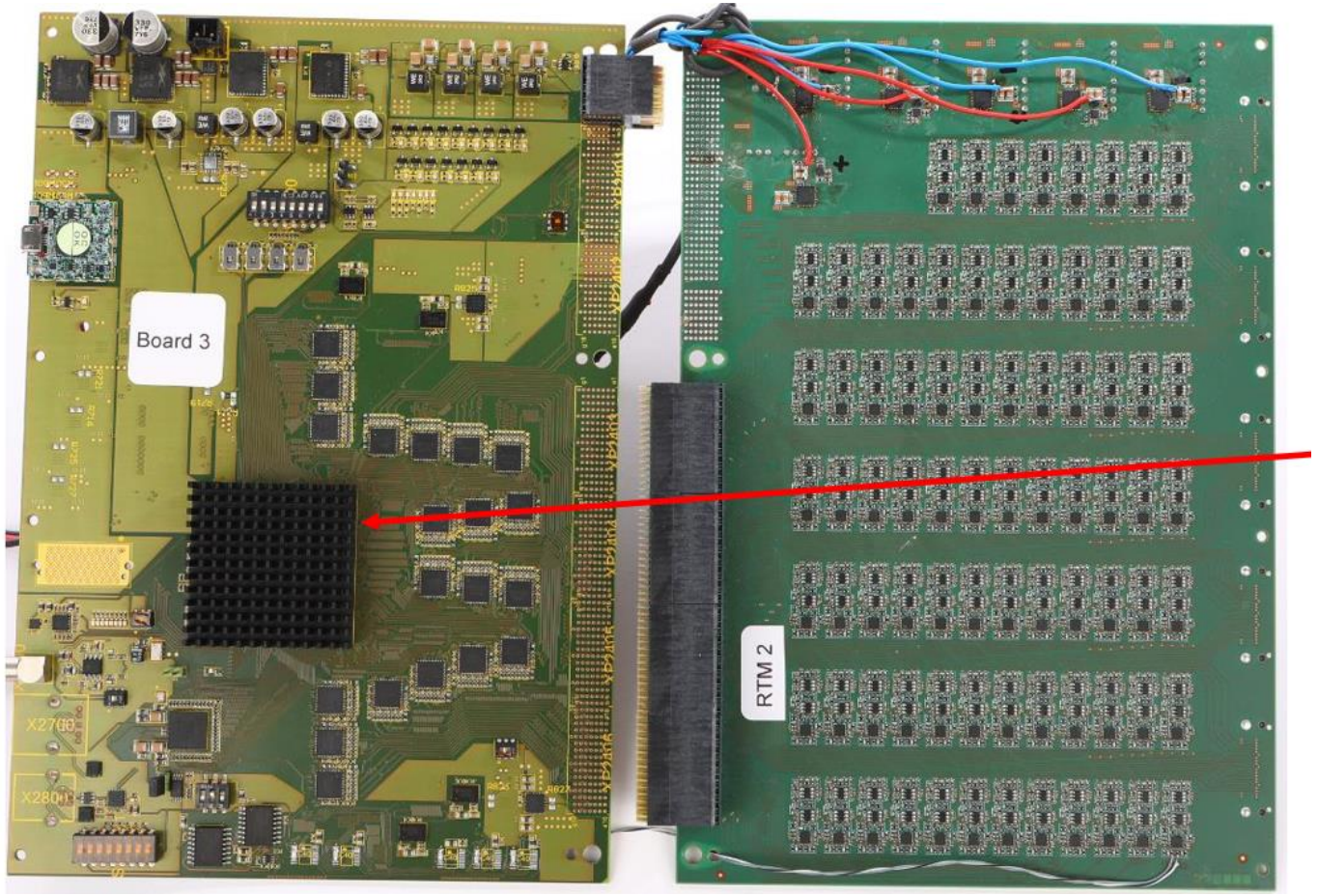
- Sampling for 160 channels, 40 4-channel ADC
- Signal processing in single FPGA
- Layout was done with high attention on length compensation of signal lines
- Modules were produced with high delay, but
- **Modules run very well**

  (high complexity, first revision)
- All 3 Modules produced run reliable during startup and beam time
- For further production, no extensive redesign is needed, just small modifications



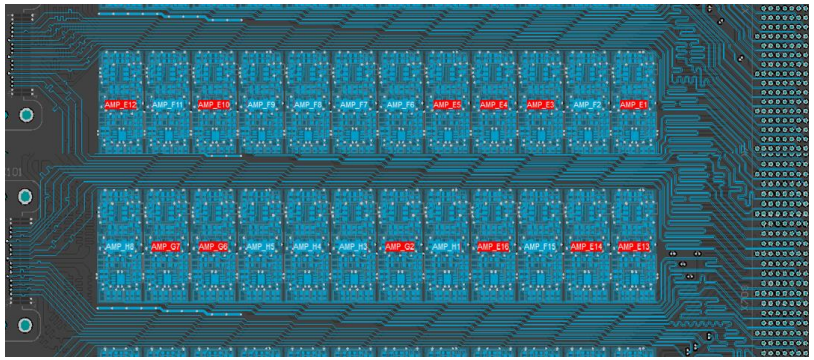
BOARD OVERVIEW

- Motivation: processing of all 160 channels as single one
- No calibration / delay setup for electronics needed



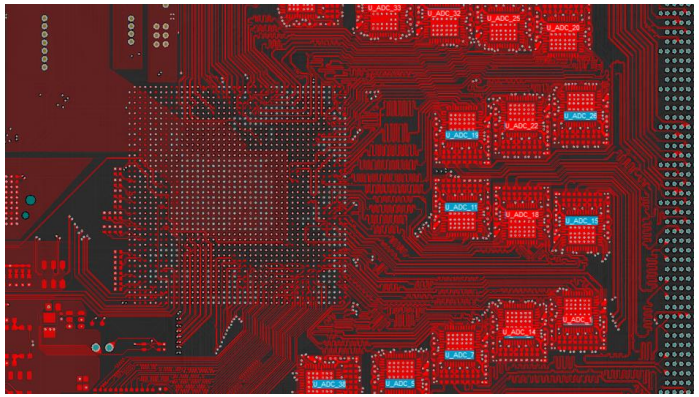
FULLY SYNCHRONOUS DESIGN

Length matching on Rear Transition Module



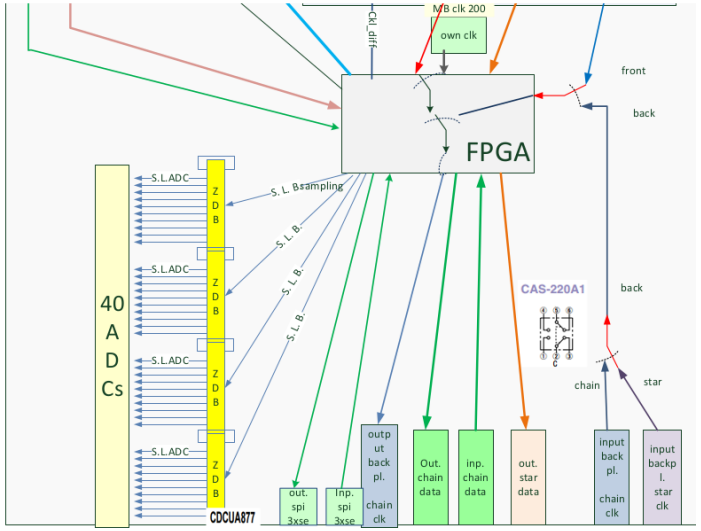
- Tolerance of 0.1mm
- All channels on board have the same signal propagation delay: no calibration for boards itself needed

Length matching on Front Module



- All digital 1GHz lines matched provided propagation difference only +45ps
- On FPGA signal capture do not require separate delay setup for each channel.

ADC clock distribution



- Use of zero delay clock buffers
- Length matched design
- Sampling clock skew < 15-20ps

MEASUREMENT SETUP

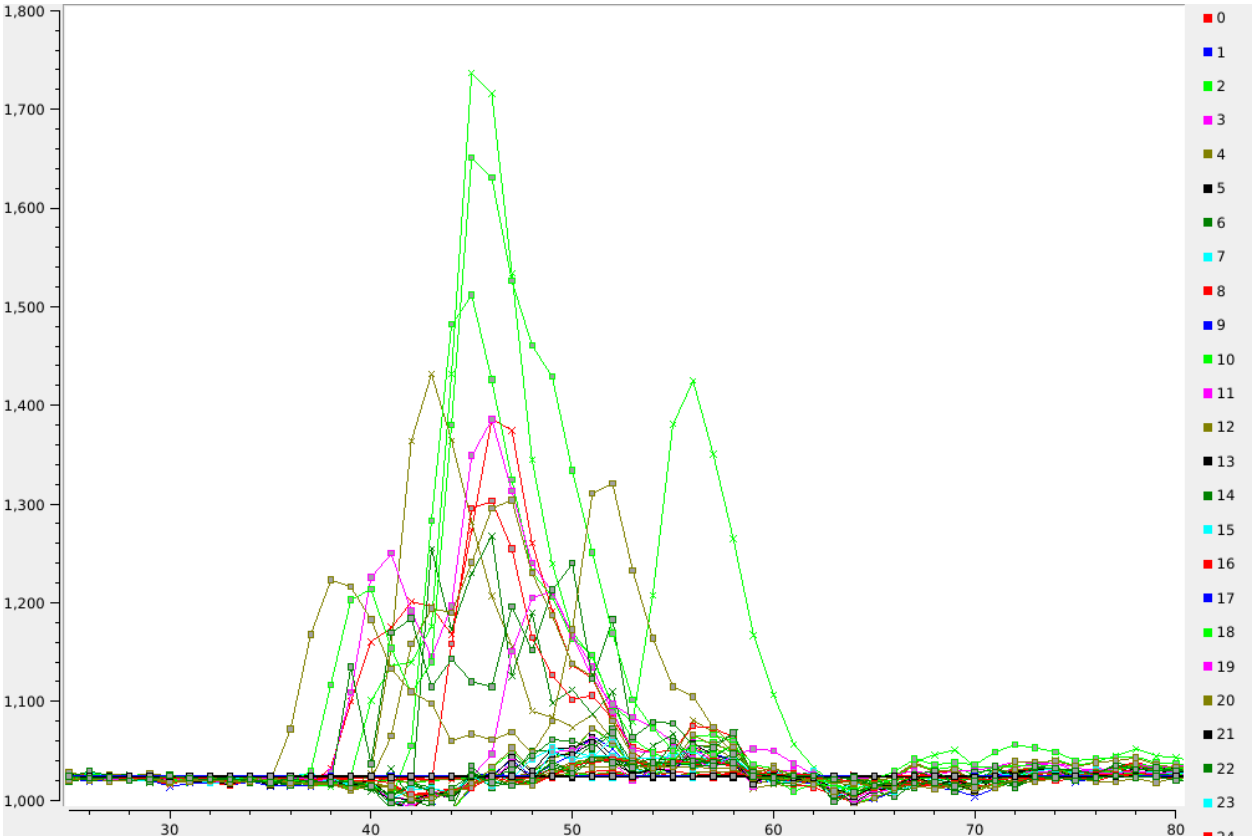
Beamtest Report
from Peter:

BEAMTEST

Due to delays, setup with limited number of channels was used

- One RTM / One Processing Board
- Layout error on RTM: 20 channels were not connected to Processing Board
- Generation of firmware for all channels very time consuming → used firmware with readout of 64 channels
- Shielding of cables HV <-> Processing Crate mandatory

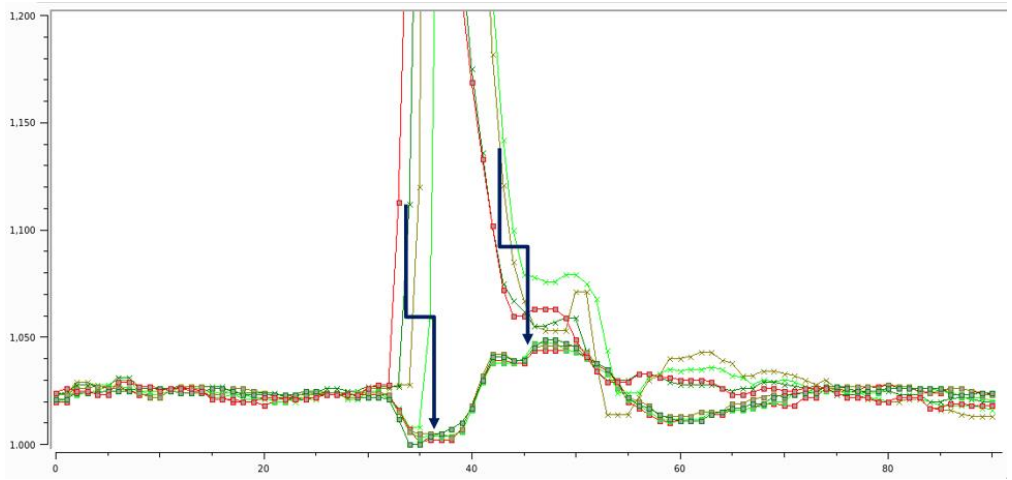
BEAMTEST



- Sampling of Straw Pulses @ 100MHz

SIGNAL

Crosstalk

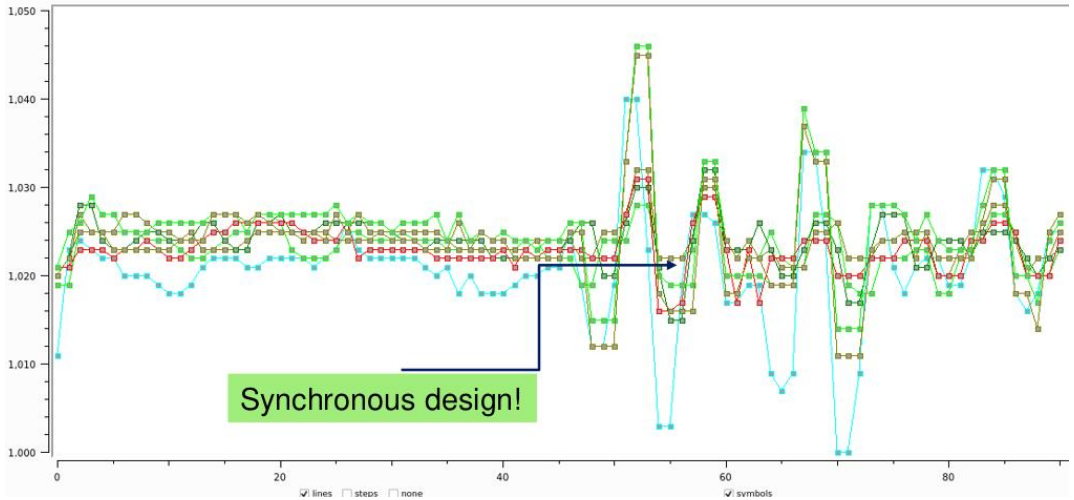


- Crosstalk is not observed at processing crate and samtec cable

  → further investigation needed

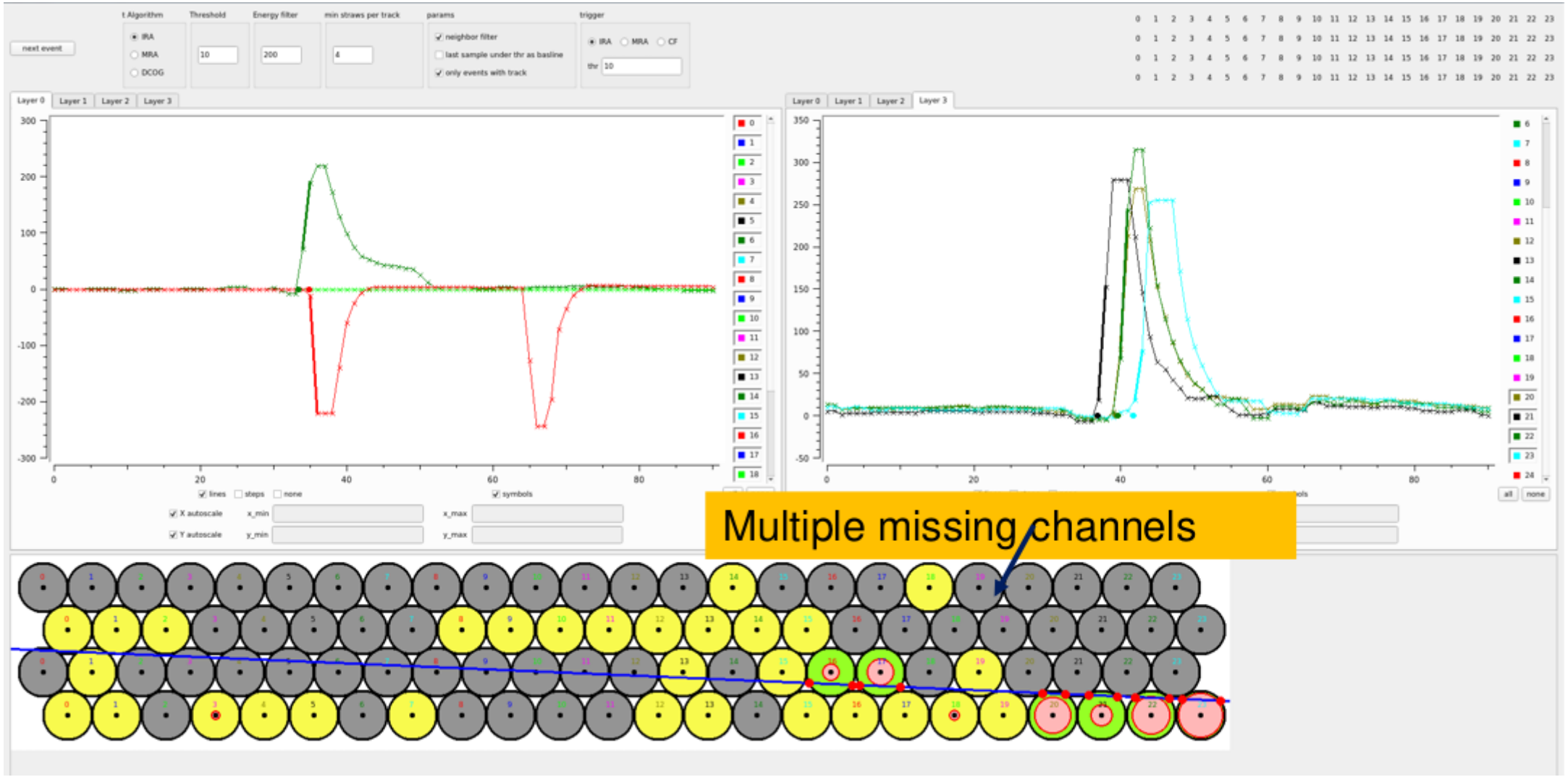
- The resolution in our design is not strong affected by crosstalk, moreover, we can detect and resolve it

Coherent Noise

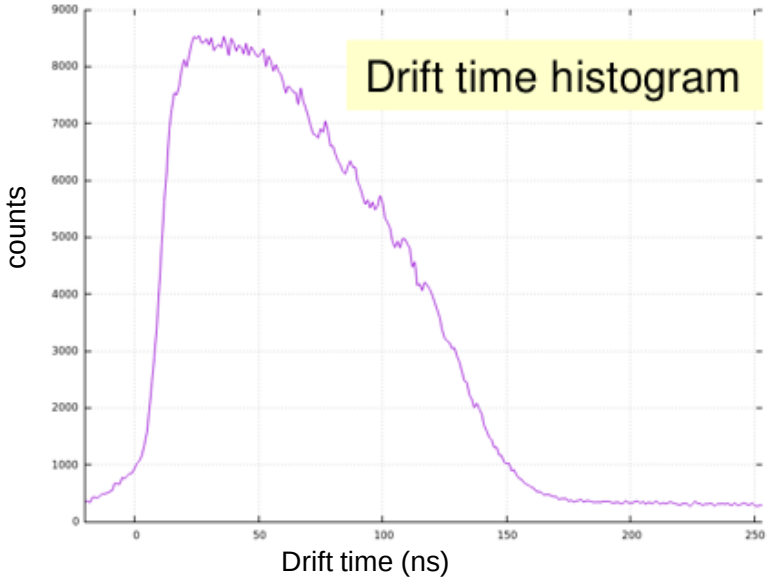


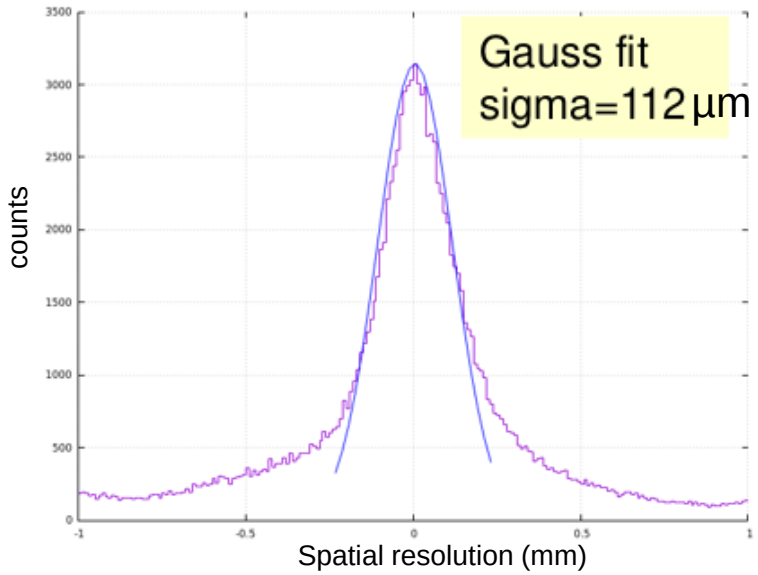
- Supposed to be introduced by Samtec cable

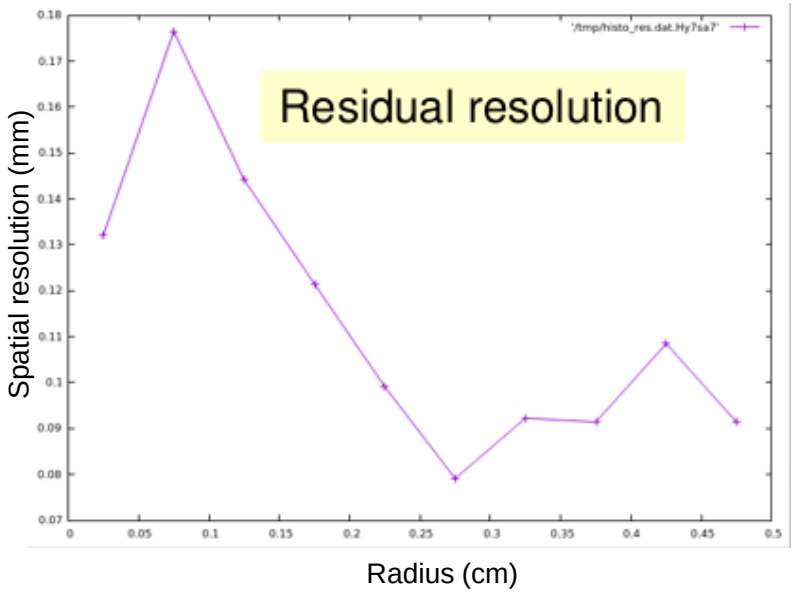
FIRST TRACKING USING NEW DAQ



PRELIMINARY RESULTS







- Sampling wtih 100MSPS
- High threshold of 20 because of noisy design
- ~ 6 straws per track
- Results comparable to results of previous beamtimes

SUMMARY

- Successful development of electronics for ADC based DAQ system:
  - Crate, Amplifier Board, Processing Board
- Functionality of system could be shown, it is able to provide reasonable tracking data
- Some debugging issues: they will be performed without HW-redesign and measurements with cosmics will be used for verification
- Modules are ready for production with minor changes

OUTLOOK

General tasks to do

- Firmware development
  - Processing (almost done), communication, integration of SODA
- Development of System Controller and Data Concentrator
  - Layout from Processing Board can be reused
- Second revision of both boards (minor changes), will be done by us, no risks and additional costs

Estimation for needed time ≈ 2 years