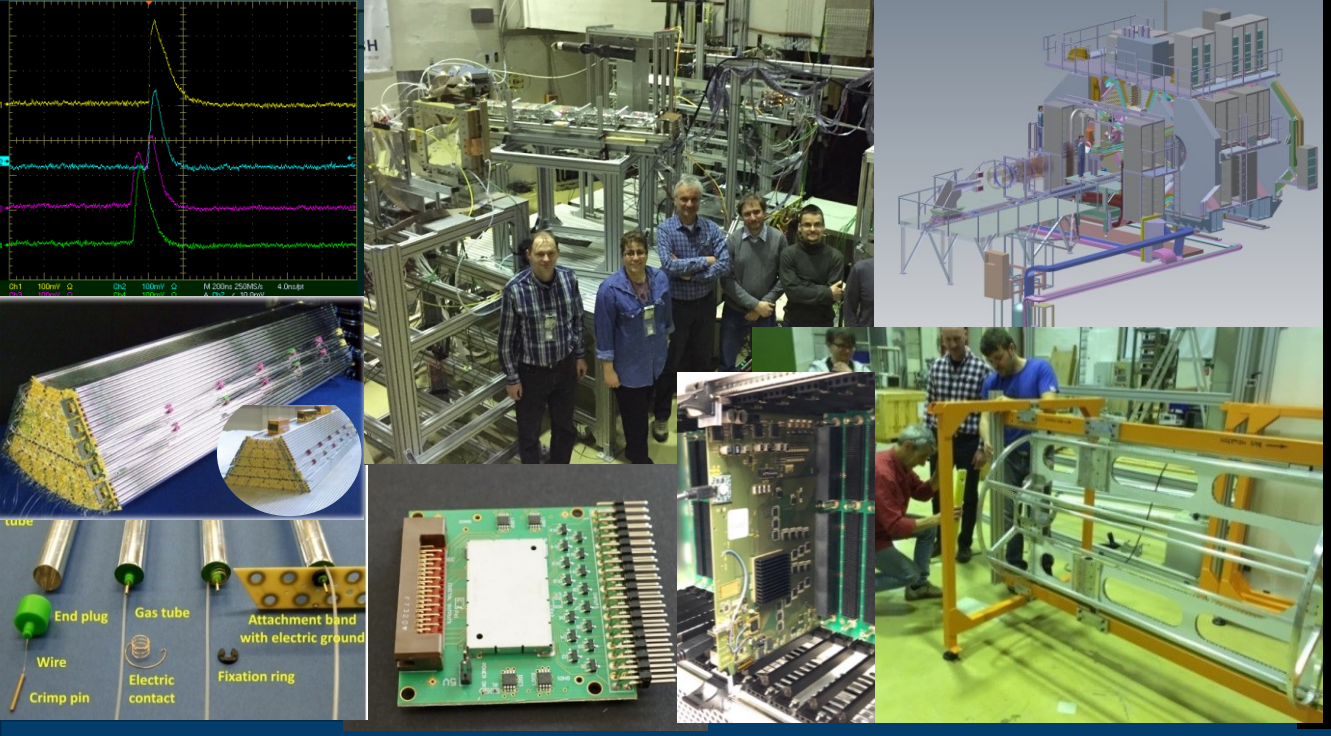


STT READOUT MEETING

25 MAY 2018 | PETER WINTZ

TOPICS TODAY

- Overview Decision Process
- General Readout Status
- System Completion & Resources

- Individual Status Reports (ADC)

- Discussion: Messages at next CM

DECISION PROCESS OVERVIEW

- Finances & resources planning for STT & FT systems at Day 1 (2023) ongoing
- STT/FT status reports at CMs and to PANDA officials (Mar/Apr/May/June)

- STT system
  - Complete system set up for day 1 start
  - Open WPs identified (mech. system, gas system, ..)
  - Cost consolidation done (e.g. readout systems, synergies, ..)

- Decision about final STT readout will be done by PANDA-CB
  - Clear readout status reports, open points & next plans needed
  - Input from us for the decision
  - High transparency of decision wanted, solid ground for acceptance
  - Implications for PANDA experiment (FE-layout, PID performance, ..)
- Decision required in June/July

STT COST TABLE

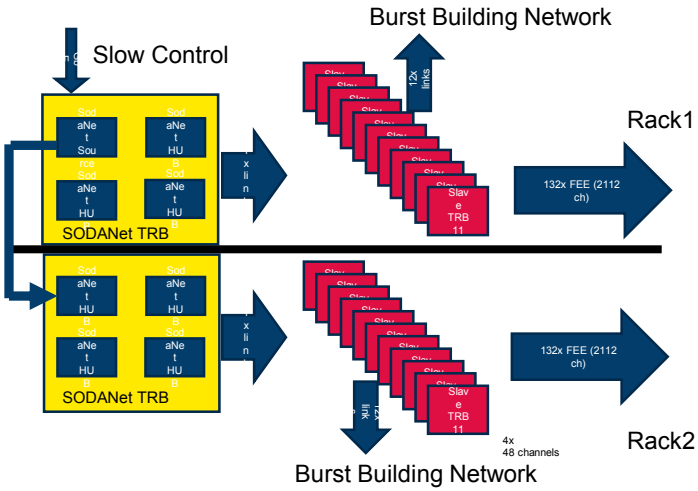
- Requested by PANDA officials and reported at CM 18/1
- Further iteration ongoing (open WP, ..)
- Readout system cost table set up within the two working groups in February
  - Mainly production & installation & maintenance costs, no re-design

STT Work Package / Costs (T EUR)				Update (2018)		Risk	Synergy Savings		Responsible Institutions		
				RO #1	RO #2		FT	Phase0	FZJ	Krakow	IFIN
3	Electronic readout										
	3.1	ASIC/TRB		**416**		100					
			ASICv1/FEBv1-v3 Design	37		40					
			PASTTRECv1/FEBv3 (4800 ch)	41		20					
			FE-layout/cooling/HV-boards	50		40					
			Readout Board/Crate: TRB3, LVDS Cable, data links	78							
			DataConcentrator	10							
			TRBx/DataConc for full lumi	100							
			ASIC/FPGA Maintenance/Lab	100			-75				
	3.2	ADC-based			**650**	100					
			Cables/HV-decoupling		180						
			Readout Board/Crate Amp/ADC/FPGA/DataConc		400	100					
			FPGA Maintenance/Lab		70						

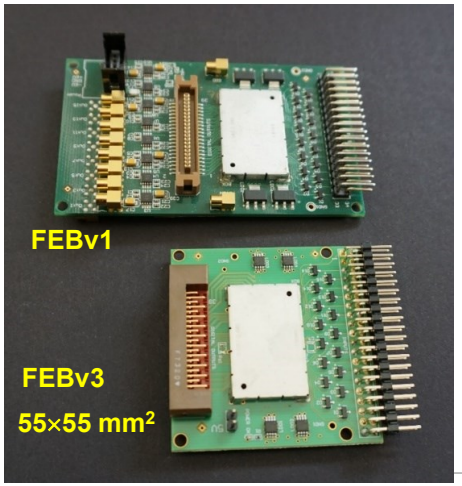
ASIC/TRB READOUT

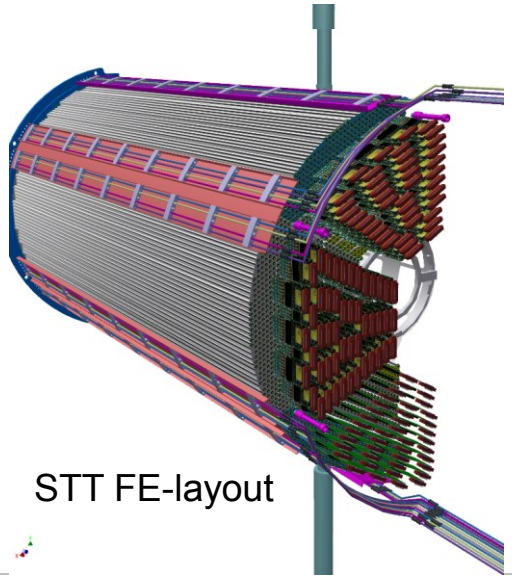
- STT-specific ASIC “PASTTRECv1“ (AGH & JU Krakow)
- FEBv3 for STT developed (small size, low power)
- TRB3 system with FPGA-ASIC control (SW)
- Data concentrator stage in progress (commercial HW)
- PID by time-over-threshold
- TRB3 integration into PANDA-DAQ (SODANet sync.)
- PANDA-DAQ (CN) set up: straws (TRB3) & EMC (ADC)

HARDWARE SETUP



Scheme by Greg. K.

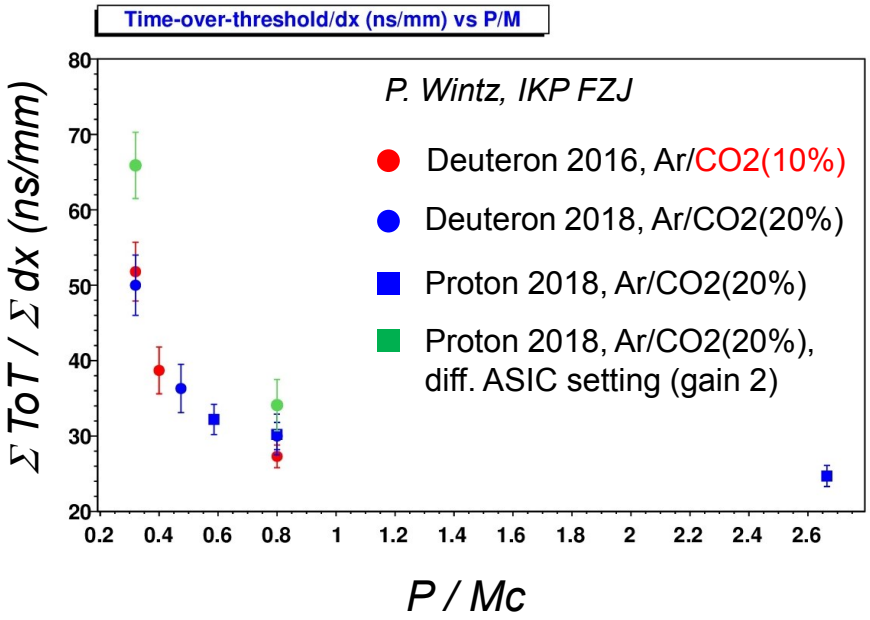


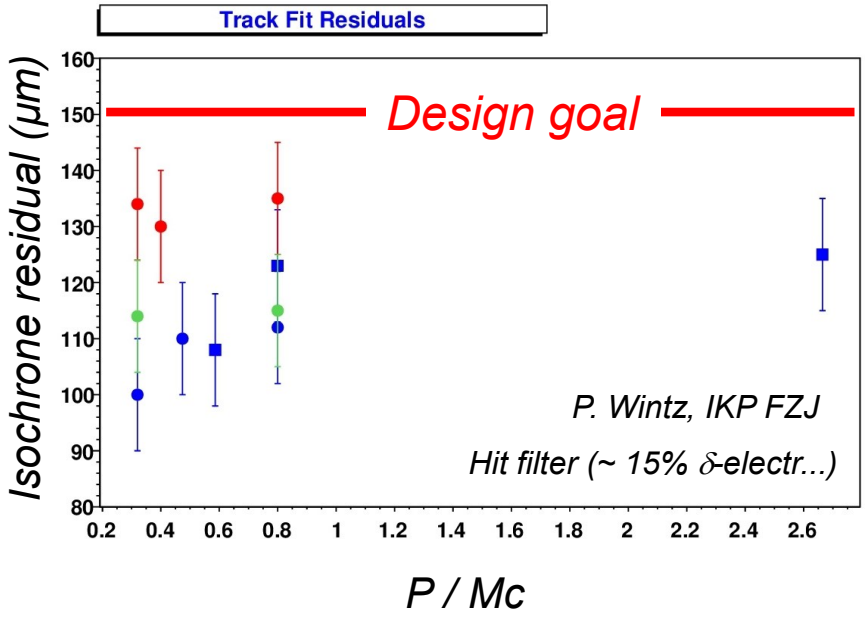


STT FE-layout

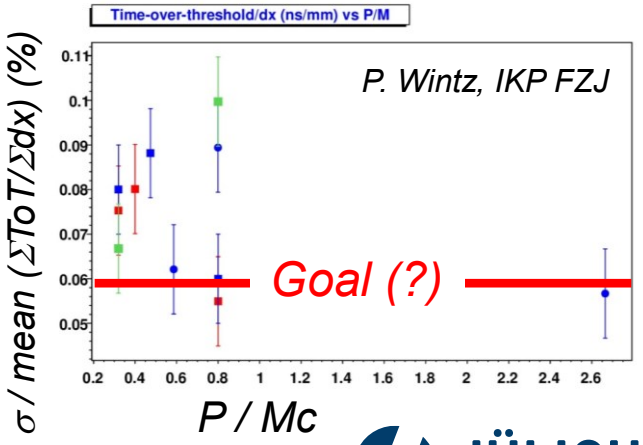
Straw (256ch, TRB3) & EMC (3x3 crystals, ADC) & PANDA-DAQ (3 CN) test setup in Krakow

TESTBEAM RESULTS ASIC/TRB



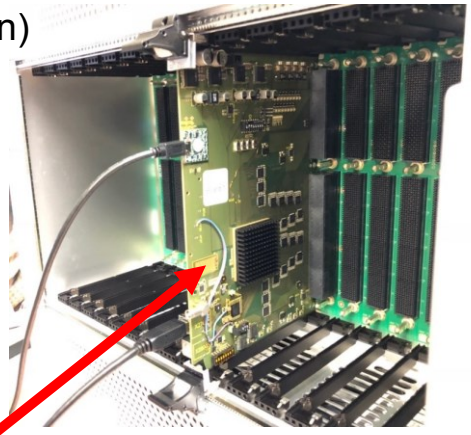


- ToT results (deuteron, proton beam & cosmics)
  - S ~ 3.3 (K/p @ 750 MeV/c, TDR: S ~ 5)
  - S ~ 5 (K/p @ 390 MeV/c, TDR: S ~ 8)
  - S ~ 9 (π/p @ 300 MeV/c, TDR: S ~ 13)
- All TDR separation power w/ 10% dE/dx resolution
- ~ 60-70% of TDR separation power reached by ToT
- But: low truncation yet, can treat results as lower limits



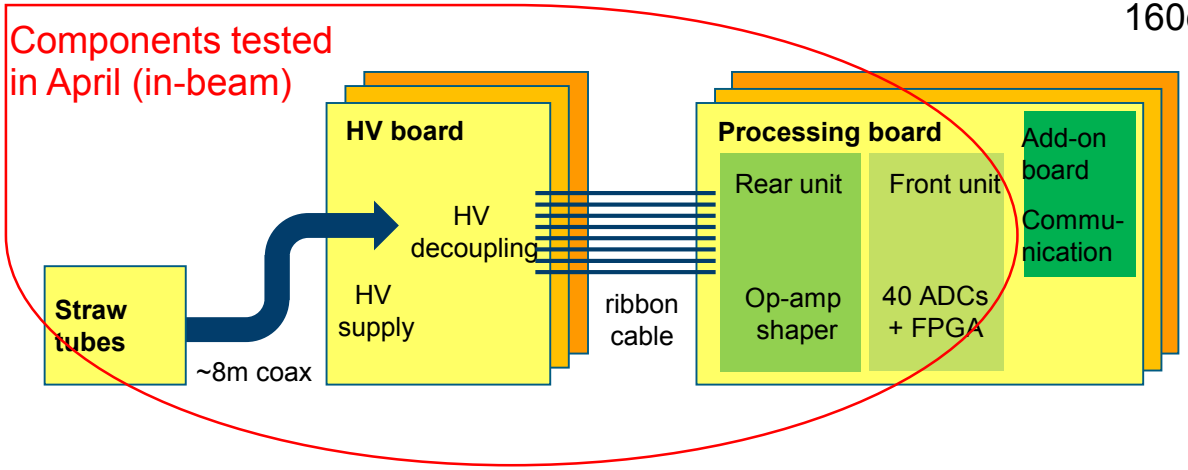
ADC-BASED READOUT

- STT-specific, non-standard scheme: “frontend electronics-free“
  - HV & signal on same coax line, straw access from backend (cut off option)
  - FE-layout: no cooling, low mat. budget, less space required
- RO board design by FZJ/ZEA-2, system scheme by IFJ PAN/IKP
  - Op-amps, waveform sampling ADC (40× 4 ch @ 160 MSPS, 12 bit)
  - WF-readout & signal processing by central FPGA (Xilinx Virtex7)
- Data concentrator stage as Add-on board (hit sorting)



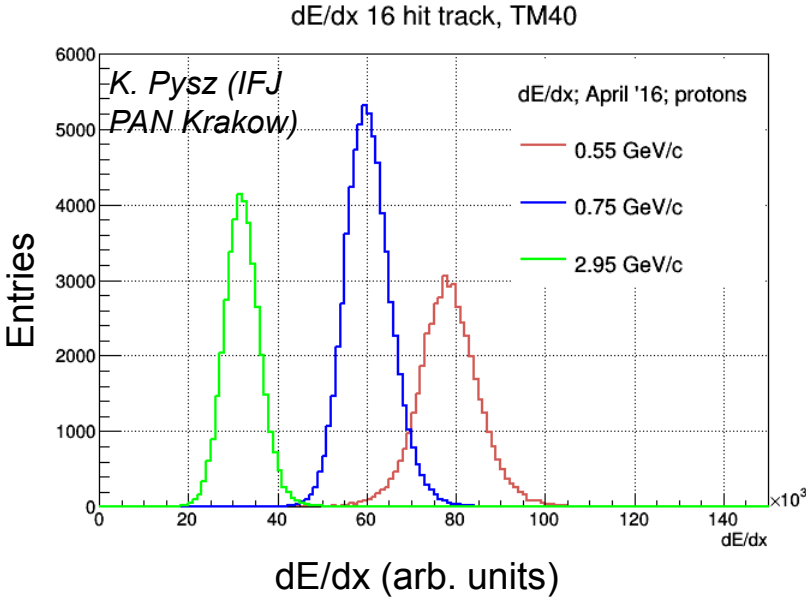
160ch readout board, double-sided, with 2x20 ADC, 1x central FPGA (crate front side)

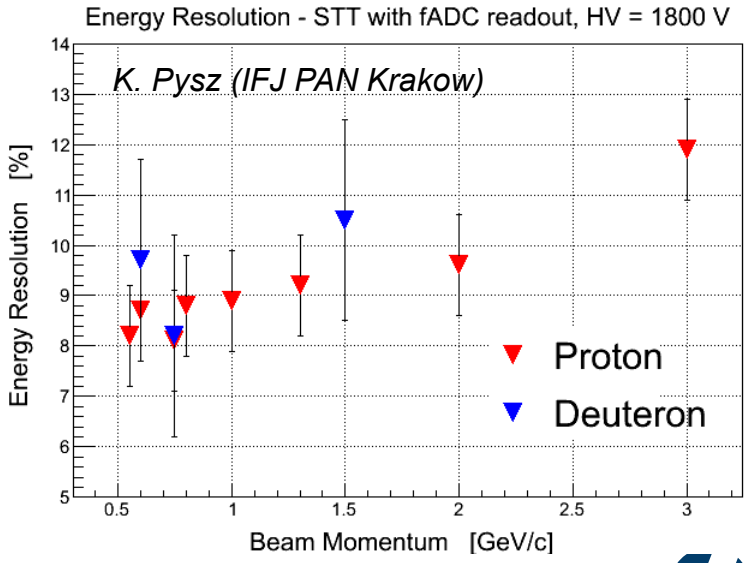
160ch amplifier board (crate rear side)



TESTBEAM RESULTS ADC-SYSTEM

- Results for FADC (240 MHz) prototype system (and direct straw cabling)
- Raw mode readout with full WF information, no real-time FPGA pulse analysis
  - Example: separation of 2.95/0.55 GeV/c protons: S ~ 8.5
  - Treat prelim. results of S as upper limit (?)
- New SADC (160 MHz, 12 bit), Op-Amp board brought into operation in April
  - ToDo: Op-amp dynamic range to be tested (5-50 keV/cm)
  - ToDo: real-time FPGA readout, data stream output (HW)





SYSTEM COMPLETION ESTIMATE

ASIC/TRB3 Readout

Remaining WP list	(min.) Resources (FTE/a)
• FE-mech. layout / cooling, HV distr., cable routing scheme	1
• Data concentrator stage (HW selected) & PANDA-DAQ integration	0.5
• Real-time FPGA programming (hit sorting, data concentr., tracking, ..)	0.5
• ASIC, FE-board & FPGA maintenance, design & test lab	1.5
• Tracking & PID SW algorithms (offline), test data analysis	0.5

- **Total: ~ 4 FTE/a** + (>) 2 PhD
- **~ -1 FTE synergy** with Forward Tracker (ASIC/FPGA/DAQ)
- TRBx for phase 3, additional cost incorporated in cost/resource table
- TRB3 & PANDA-DAQ (CN) test system set up, in-beam tests next (straws & EMC)
- STS@HADES setup, ~1800 channel ASIC/TRB3 system under exp. conditions

SYSTEM COMPLETION ESTIMATE

ADC-based Readout

Remaining WP list	(min.) Resources (FTE/a)
• Analog signal part, final cable routing / hv-supply, installation	1
• Final Amp/ADC board design & production	0.5
• Communic. board design & production, PANDA-DAQ integration	0.5
• WF processing and readout in real-time (FPGA)	0.5
• Pre-series system set up, testbeam measurements	1
• Real-time FPGA programming (hit sorting, data concentr., tracking, ..)	0.5
• System HW & FPGA maintenance, design & test lab	1
• Tracking & PID SW algorithms (offline), test data analysis	0.5

- **Total: ~ 5.5 FTE/a** + (>) 2 PhD

- ~ 1 more year (x 4.5 FTE) for completion & commissioning of pre-series system
- ~ 2 weeks testbeam time with dE/dx range 5-50 keV/cm

GENERAL REMARKS

- Spatial (isochrone) resolution better than design goal (σ = 150µm) expected for both readouts, same calibration & tracking methods
- PID capability demonstrated for both readouts by in-beam tests
- Better PID expected for ADC (pulse area $\leftrightarrow$ pulse width), but to be demonstrated in-beam over full dE/dx range (pulse shape distortion by amp/shaper expected)

- FTEs for work packages not (fully) assigned, EoIs of institutions existing (partly)
- **MoUs required to establish WP planning** towards STT installation

- Manpower situation critical, remains challenging (staff & students)
- Lab capacities critical (personnel)
- Experience loss instead of experience build-up, continuation of WP difficult
- Additional outsourcing of WPs might be required (e.g. cabling, solder work, ..)
- Temporary personnel to be set up (student courses, ..)

DISCUSSION