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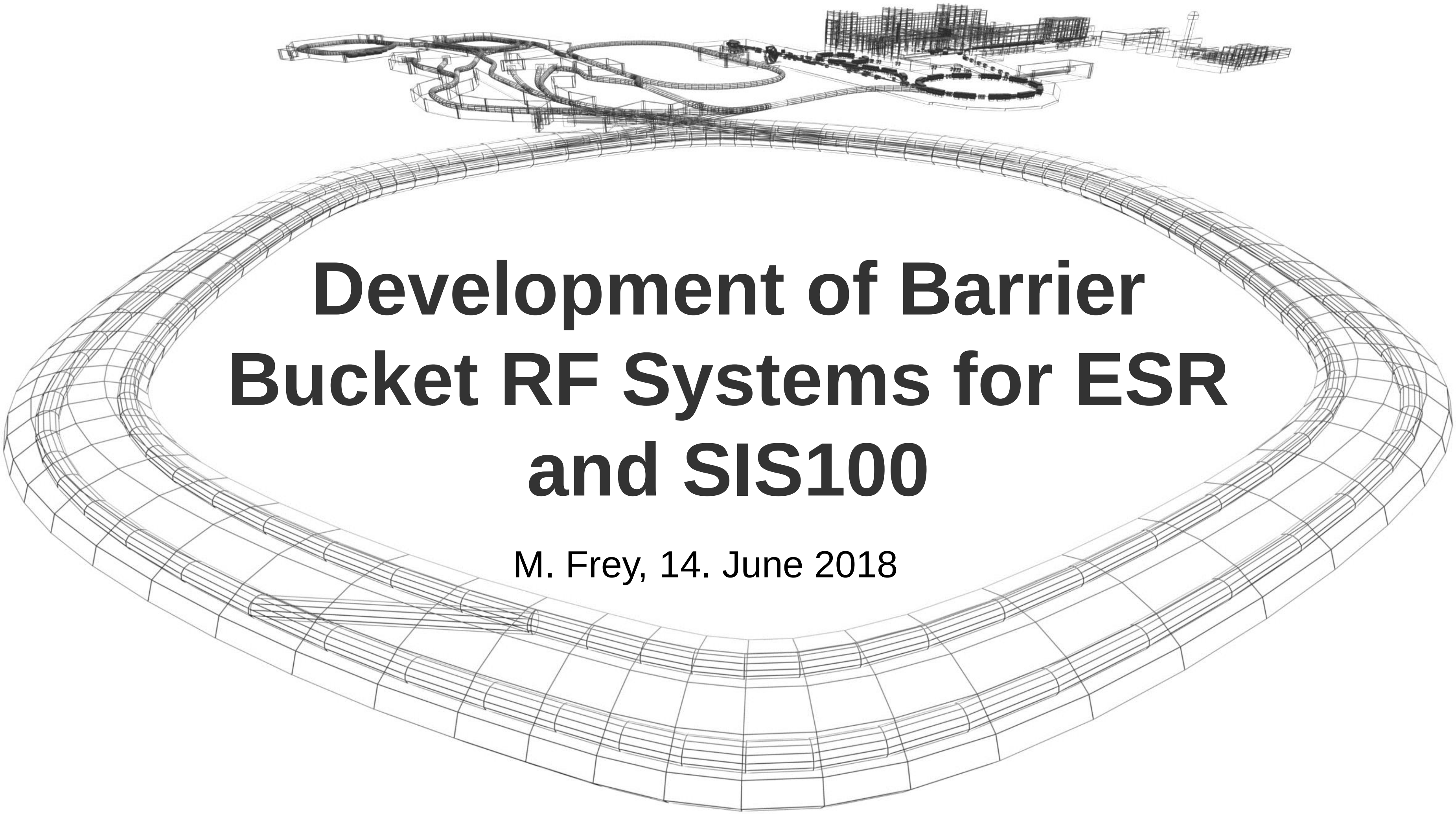


Development of Barrier Bucket RF Systems for ESR and SIS100

M. Frey, 14. June 2018

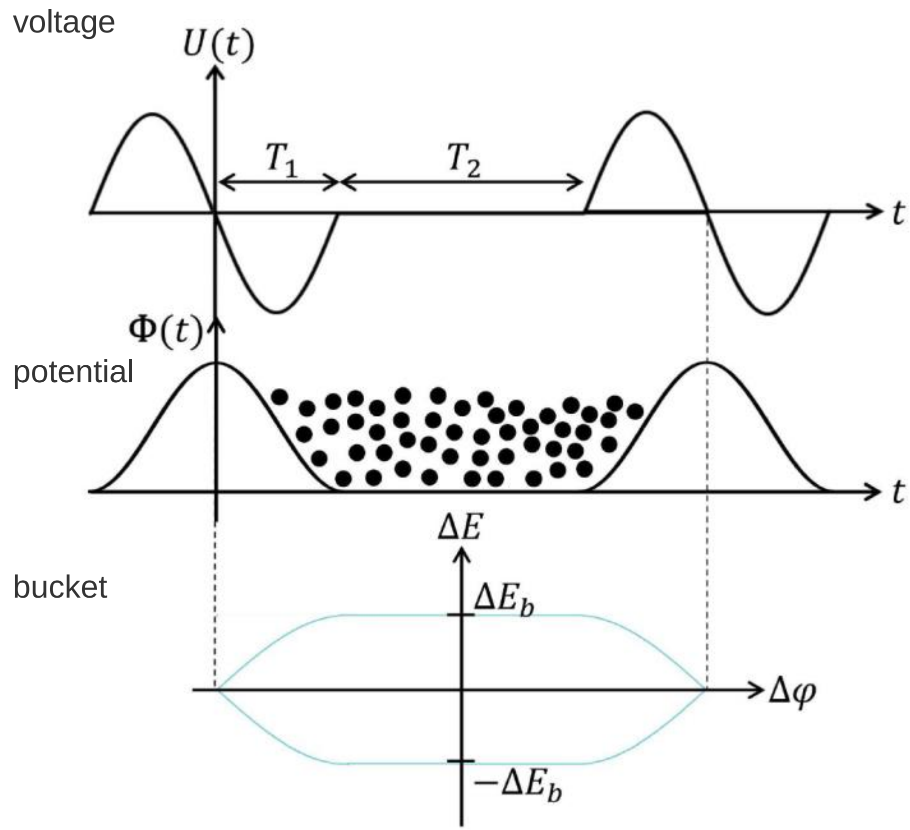
outline

- motivation/history at ESR
- ESR BB system
  - requirements
  - theory of operation
  - choice of ring core material
- ESR BB cavity design
  - prototype ring core impedance measurement+modeling
  - PSpice simulation of full cavity
- ESR BB cavity properties
- ESR BB pre-distortion
- ESR BB signal generation
- ESR BB full system results
- ESR BB outlook

- SIS100 BB system

motivation

- RF pulses create potential barriers
- barrier creation allows longitudinal beam manipulation, e.g. confinement of a bunch
- when barriers are moved, beams can be compressed -> intensity increases
- multiple injections between compression operations lead to further intensity increase („longitudinal stacking“)



bucket height

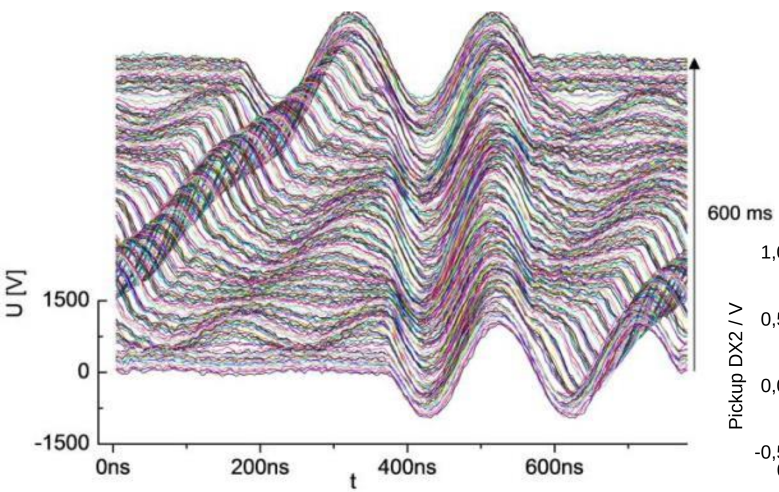
$$\Delta E_b = \left(\frac{2\beta^2 E_0}{|\eta|} \frac{\left| \int_0^{T_1} eU(t)dt \right|}{T_0} \right)^{\frac{1}{2}}$$

J. Harzheim, Temf, TU Darmstadt

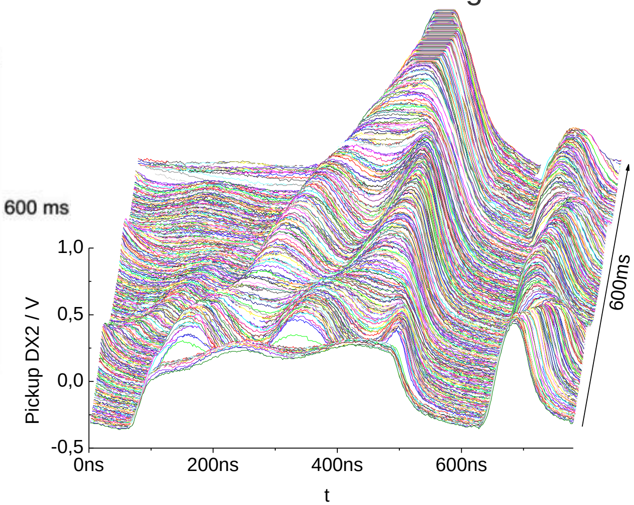
demonstration at ESR

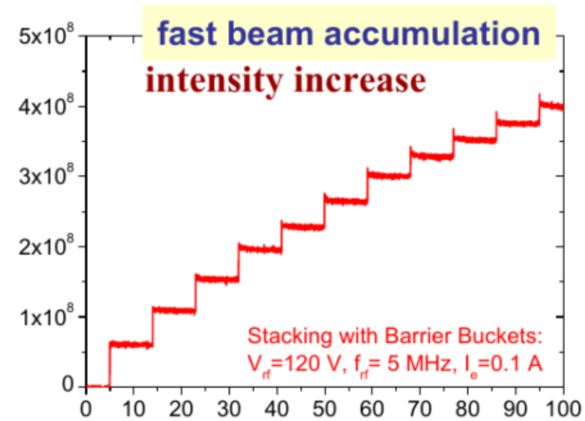
- ferrite acceleration cavities were used with single sine + offset pulses

gap voltage



beam signal





G. Schreiber, LRF department, GSI

C. Dimopoulou, BCO department, GSI

- hardly feasible due to extreme sensitivity concerning pulse parameters

development of a specialized BB cavity

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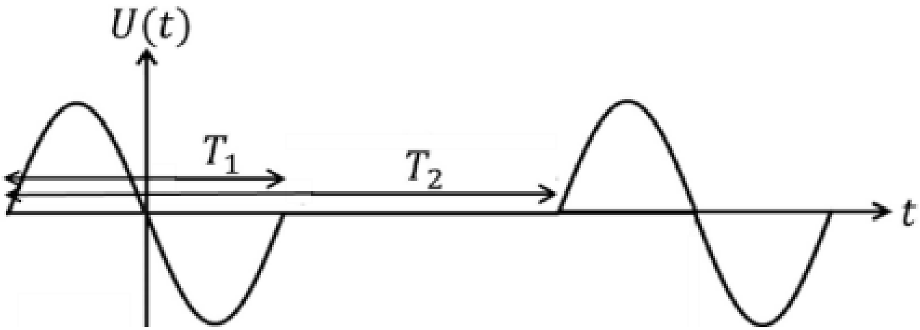
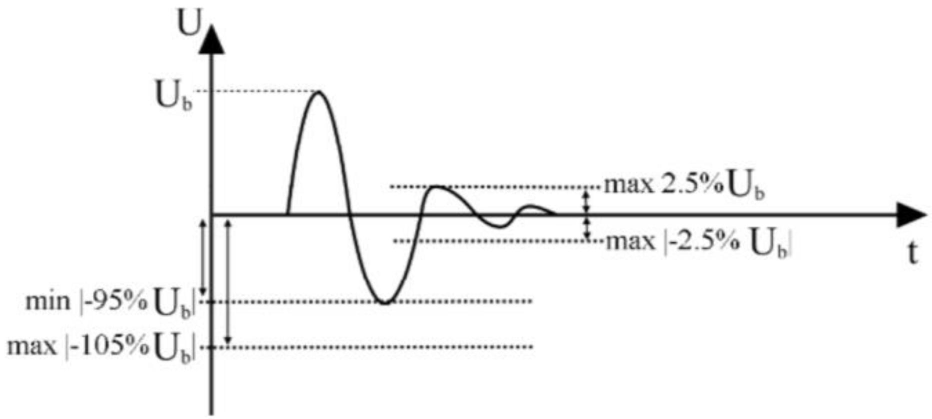
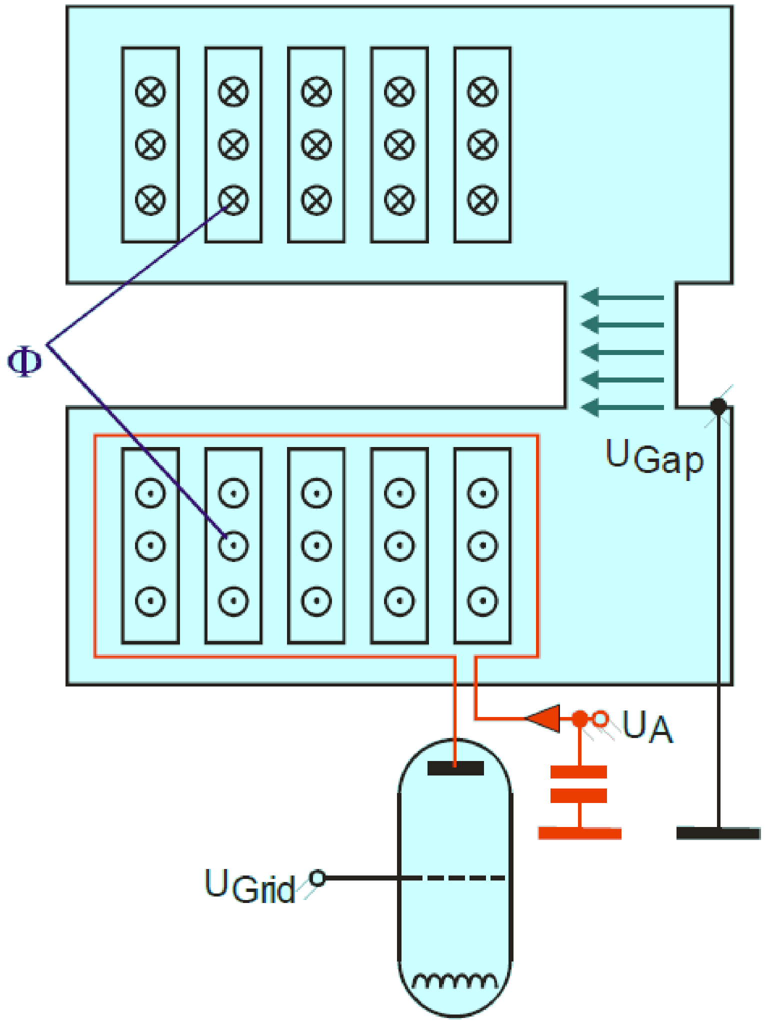
ESR requirements

- single sine pulses of T_1=200 ns (f_{BB}=5 MHz)
- pulse amplitude $\hat{U} = 1\,kV$
- flexible control of amplitude and repetition period T_2 at injection energy: 4-400 MeV (between f_{rep}=250 kHz and f_{rep}=2 MHz)
- symmetry and low ringing





ESR cavity design – theory of operation



H. Klingbeil, Temf, TU Darmstadt

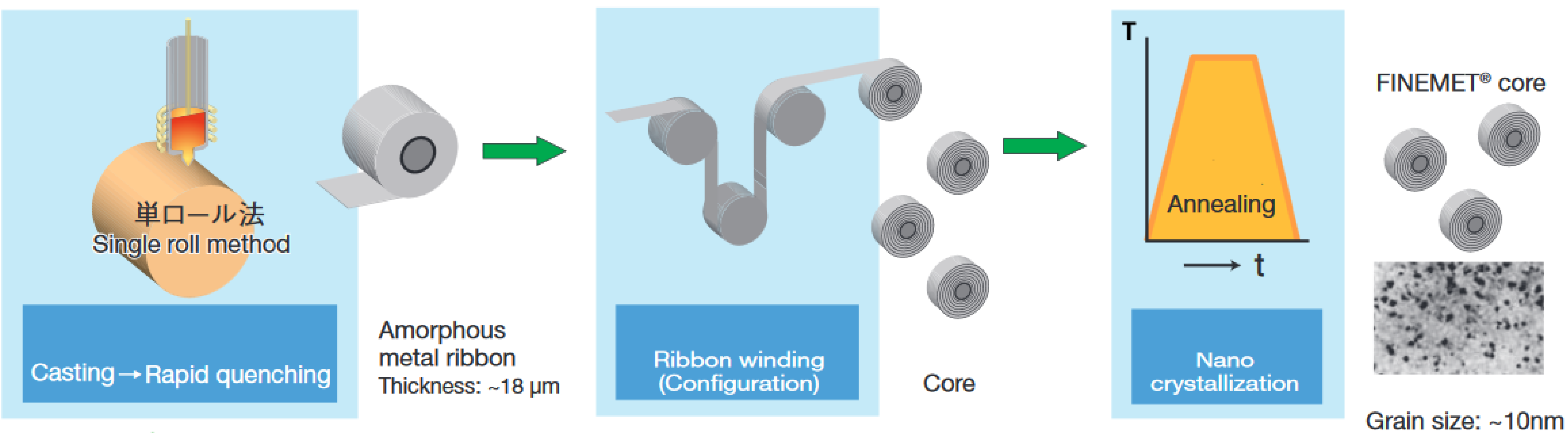
- cavities with ring cores are transformers: ring core = iron core, housing = secondary winding, gap capacity = load
- ring cores are a lossy inductance defined by geometry and complex $\underline{\mu}_r$

$$L_0 = l\frac{\mu_0}{2\pi}\ln\left(\frac{d_o}{d_i}\right) \qquad L = L_0\mu_r' \qquad R = \omega L_0\mu_r''$$

- ring core inductance L, resistance R and gap capacity C form RLC circuit
- loss effects in ring cores described by μ_r'' (~R) -> define oscillation damping -> bandwidth

ESR cavity design – ring core material

- ferrites: high Q-value -> narrowband cavities ☹
- iron-based nanocrystalline Magnetic Alloy (MA) ring cores: very low Q-value -> broadband cavities ☺



Hitachi Metals Ltd.

- cores are wound from thin ribbon: side surfaces are roughly textured because layers tend to misalign (important for cooling)

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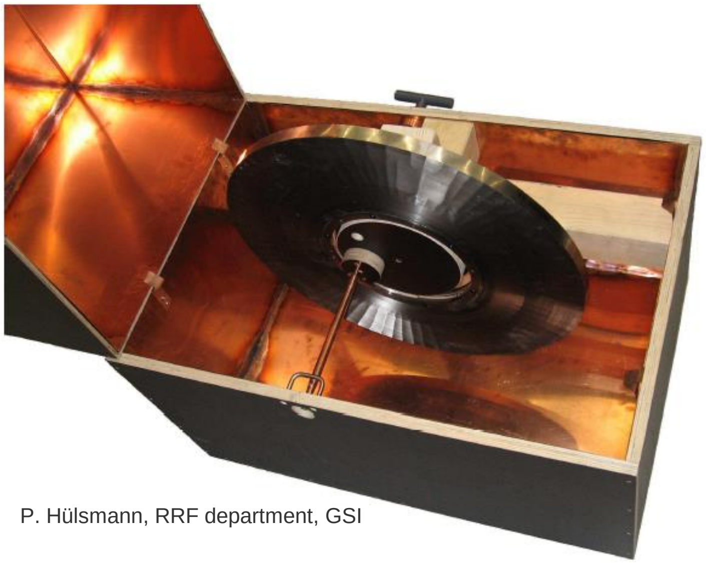
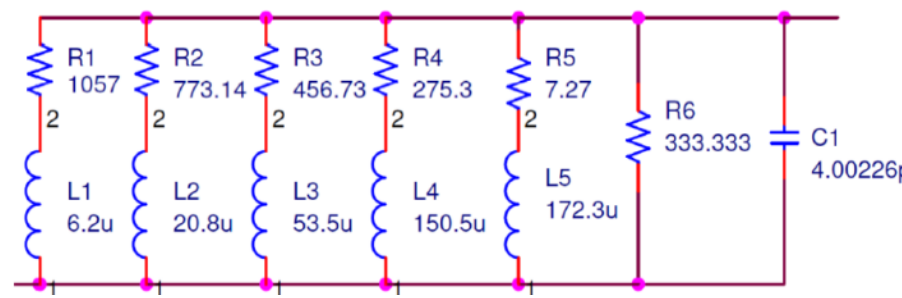
strategy: ring cores dominate cavity –> analyse prototype core to enable simulation of full cavity -> obtain amplifiers load impedance

ESR cavity design – impedance measurement and PSpice modeling



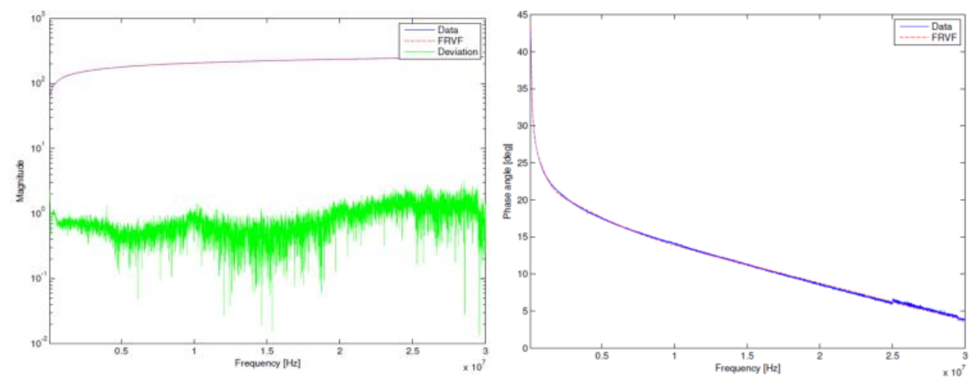
P. Hülsmann, RRF department, GSI

- identification of lumped-element equivalent circuit using „vector-fitting“ algorithm



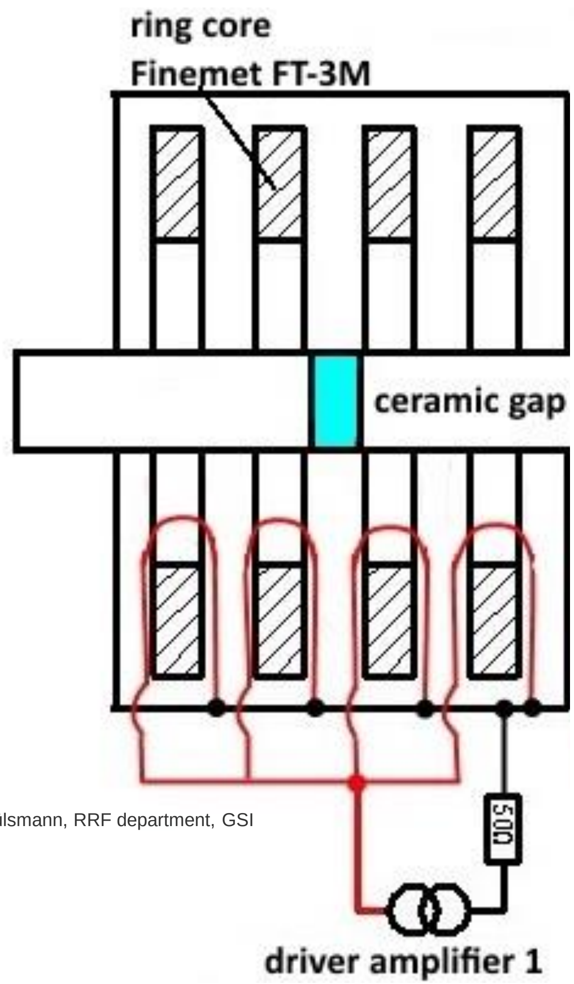
J. Harzheim, H. Klingbeil, Temf, TU Darmstadt

- impedance measurement of prototype core in test box
- subtraction of test box influence (estimated with CST simulation)



- 1 ring core at 5 MHz: $|Z| \approx 200\ \Omega$

ESR cavity idea



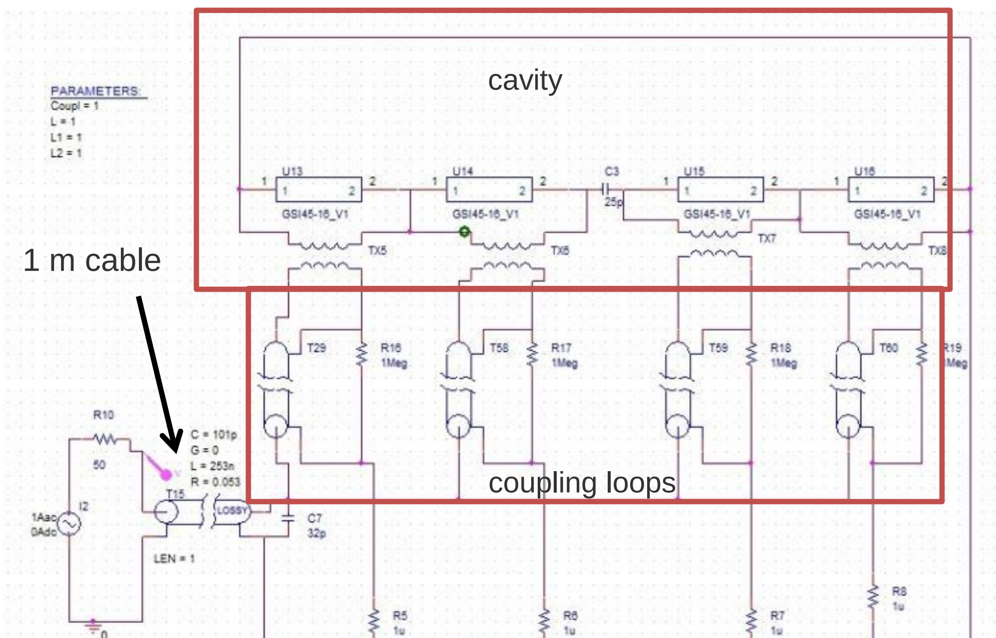
P. Hülsmann, RRF department, GSI

- 4 ring cores connected in parallel

  -> gap voltage
= 4 x voltage at load

- one cavity per pulse (2 in same housing)

ESR simulation of full cavity



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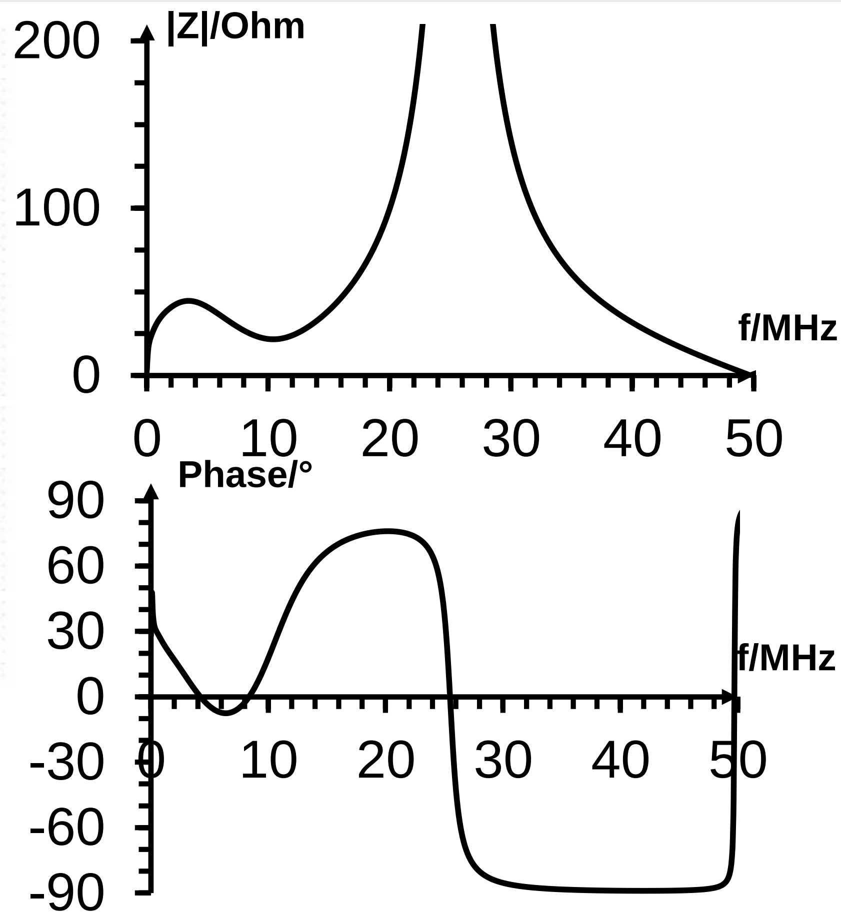
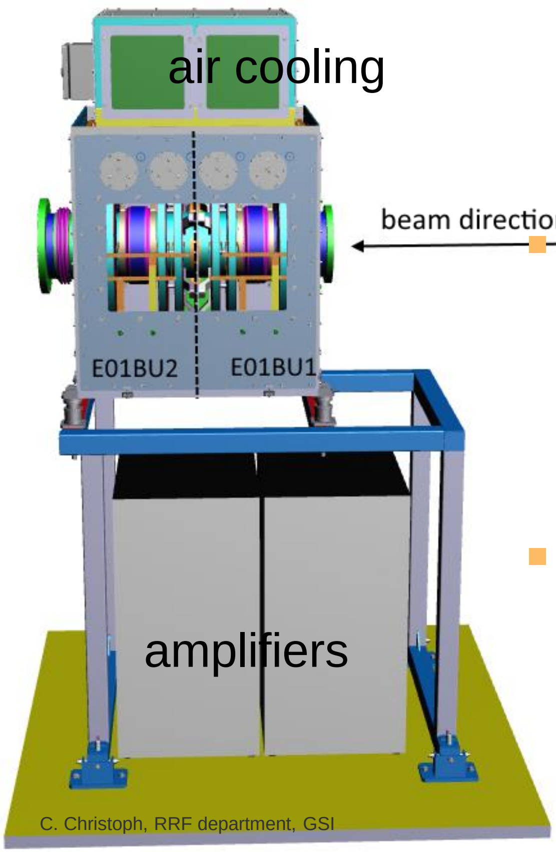


- sufficient matching between amplifier and cavity at 5 MHz
- at 5 MHz and |Z|=25 Ω, U=4x225 V =900 V possible with 1 kW

satisfying results → production approval

ESR cavity design – CAD and production

- based on extensive testing with ARD broadband test cavity



- very short beam pipe requested (for Schottky pick-up on same base-frame)
- large ESR beam pipe diameter -> little space for ring core material
- power range of amplifiers 1 kW -> air cooling necessary

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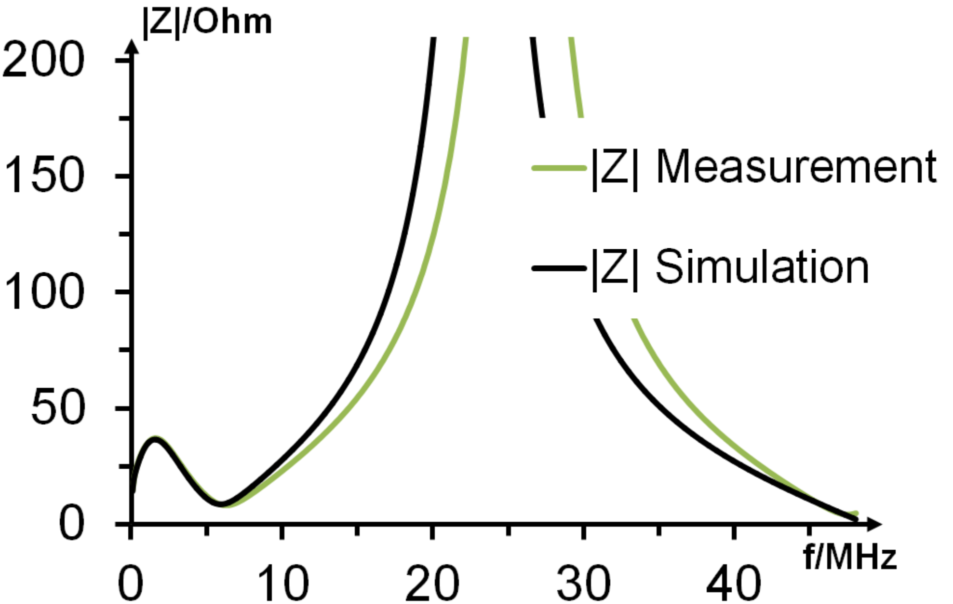
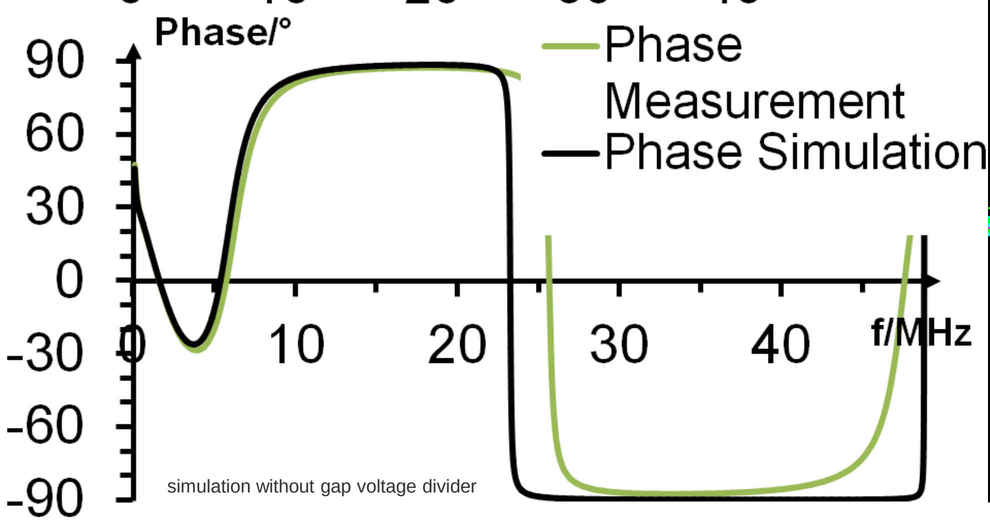
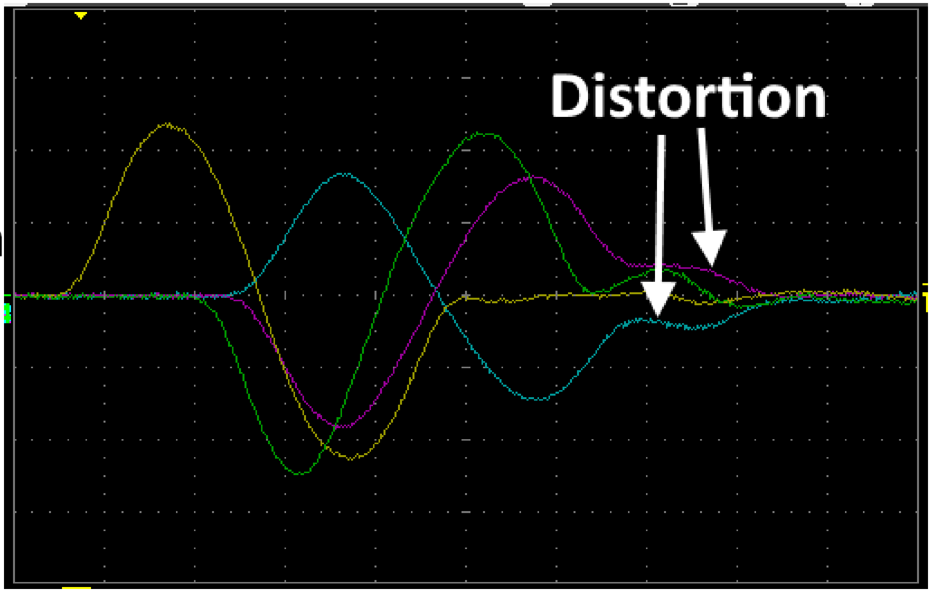
ESR cavity properties





measurement result:

- frequency response results in distortion of input voltage
- pre-distortion of signals is necessary

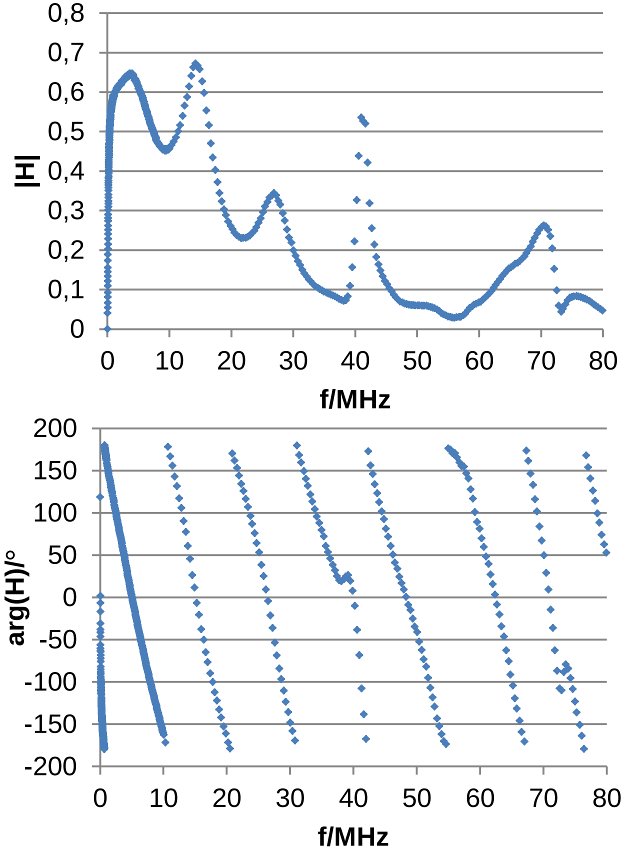


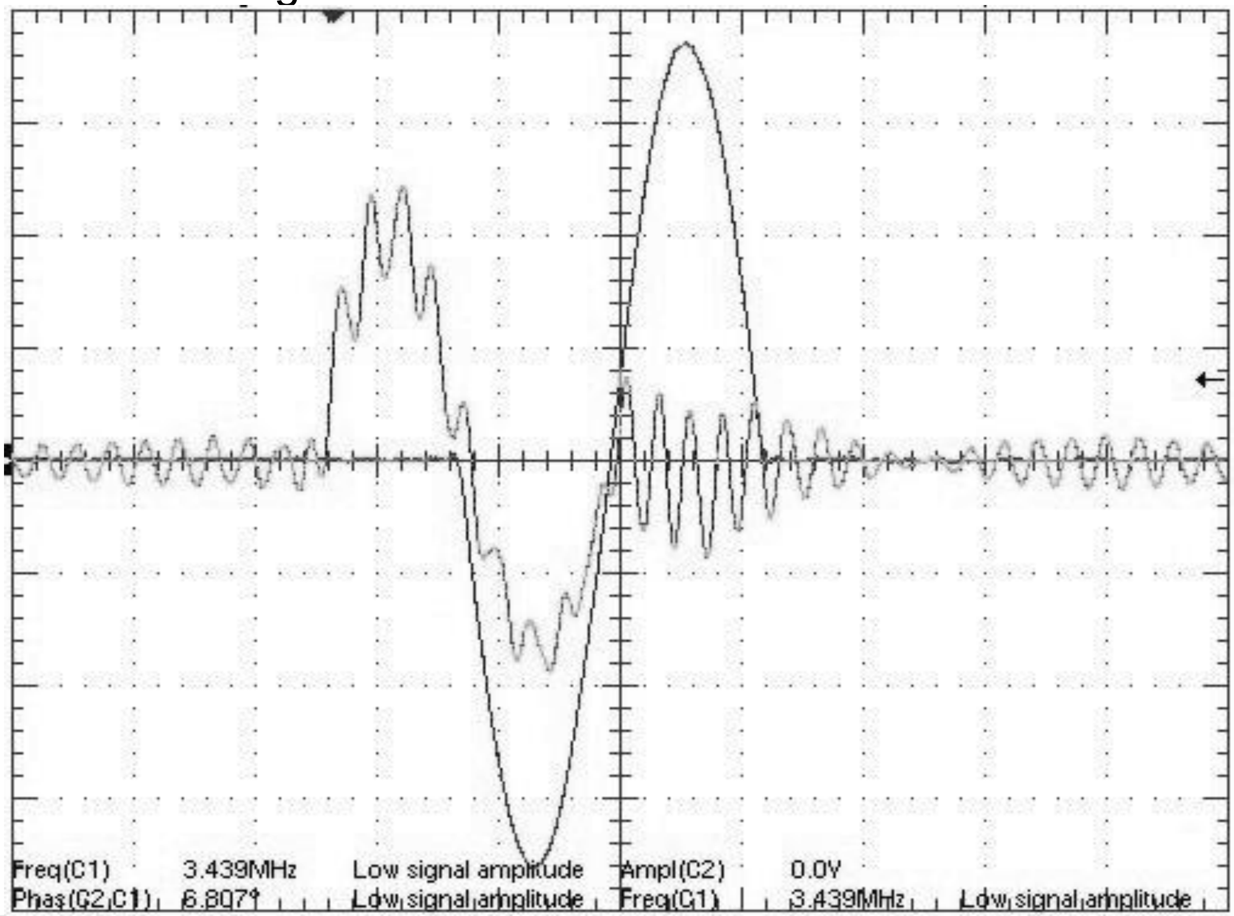
LLRF - pre-distortion of signals

1. measure transfer function H

2. calculate Fourier-coefficients of pre-distorted signal

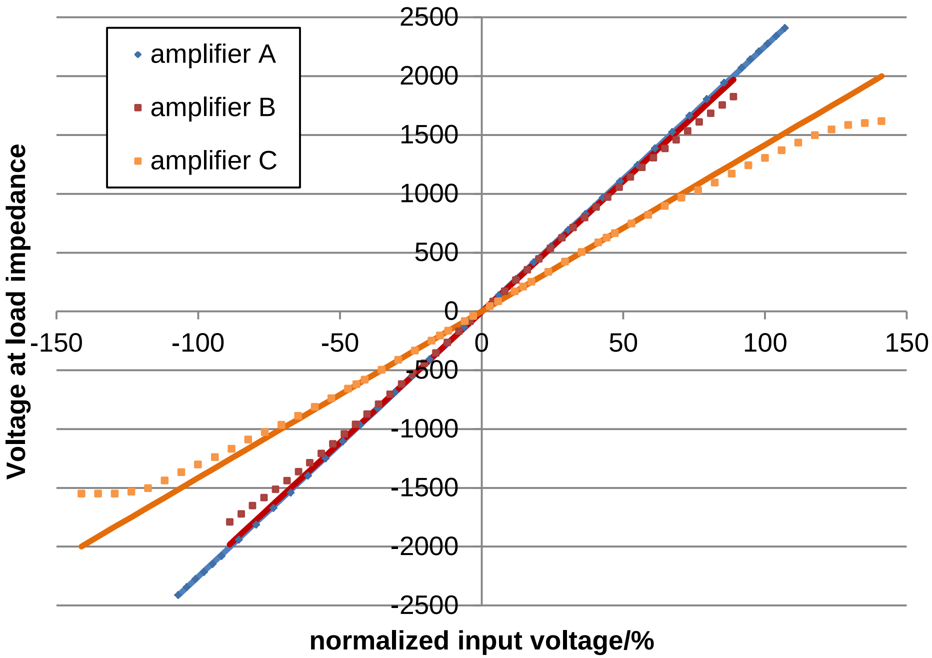
3. transformation to time-domain + application

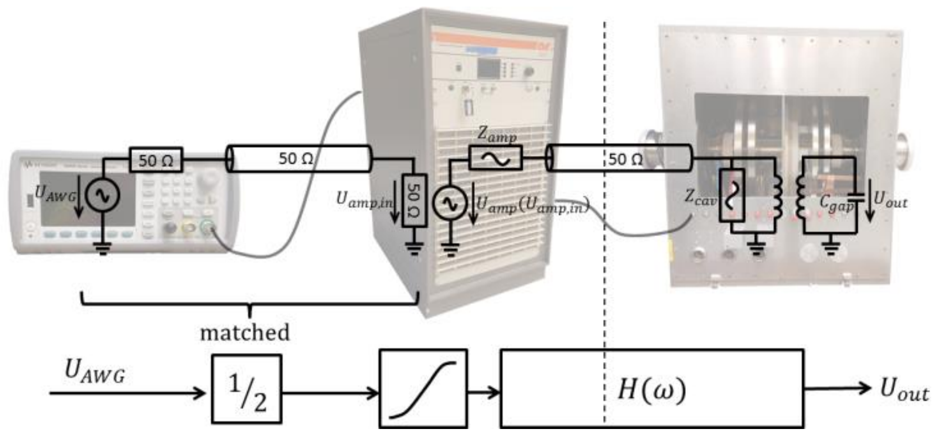




LLRF - non-linear predistortion

- problem with linear pre-distortion: amplifier characteristic





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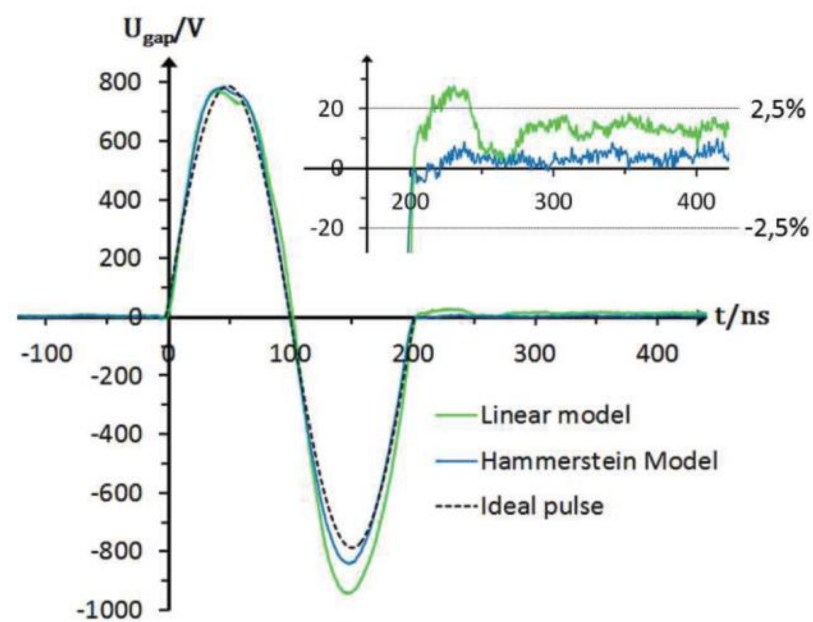

- no datasheet value depicts this characteristic -> amplifier selection by testing

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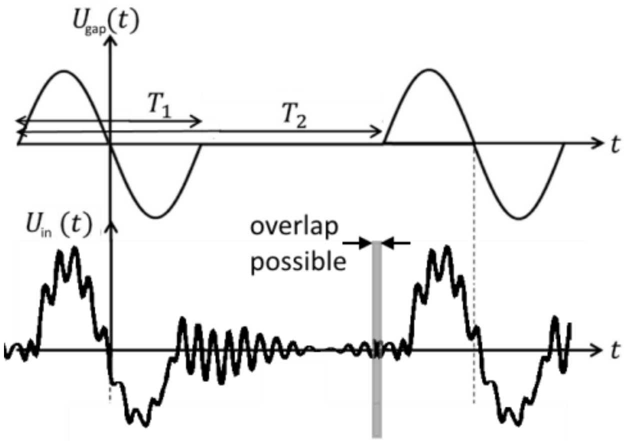
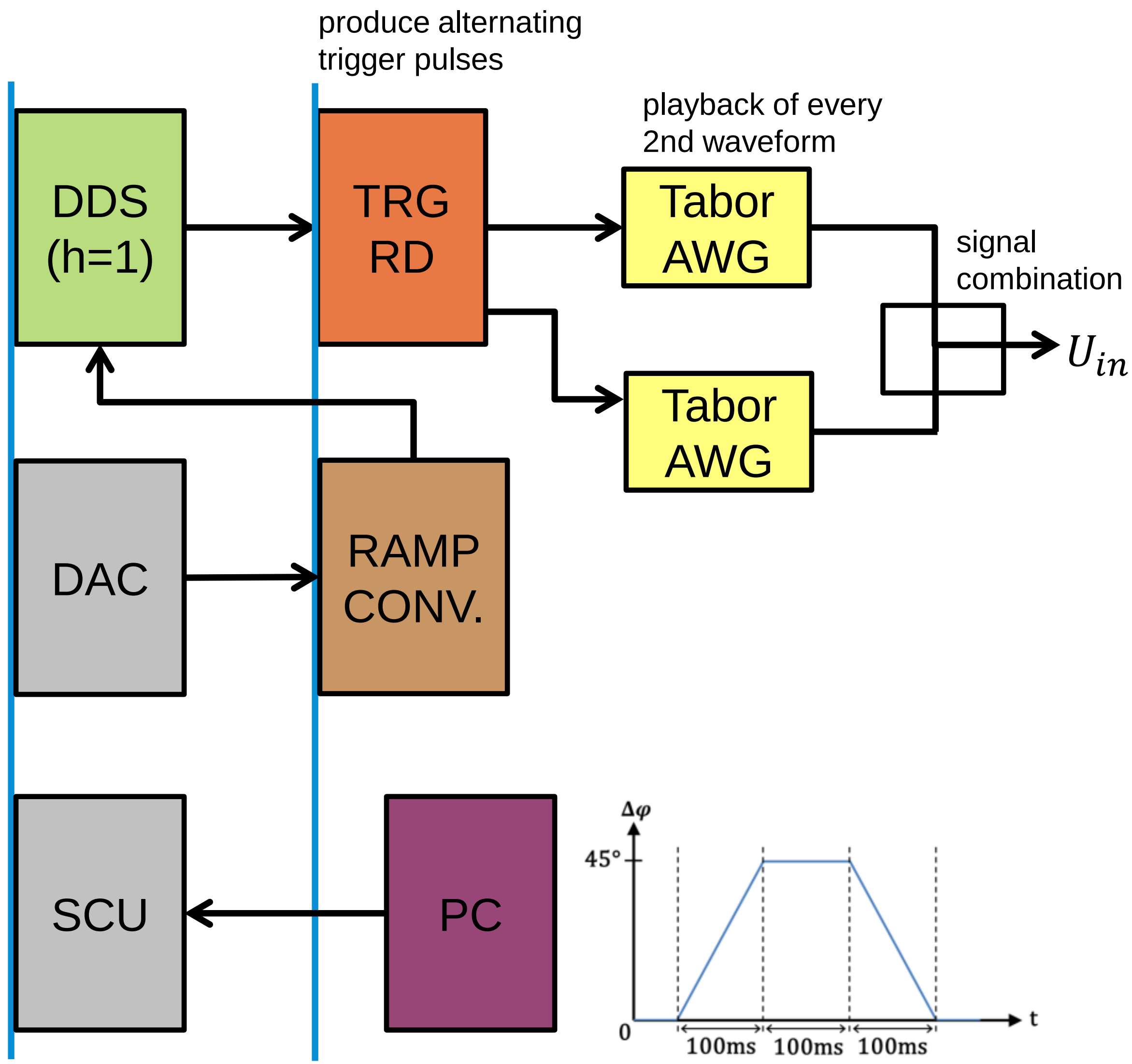
LLRF – re-triggering

- when barriers are moved, consecutive pre-distorted waveforms may overlap

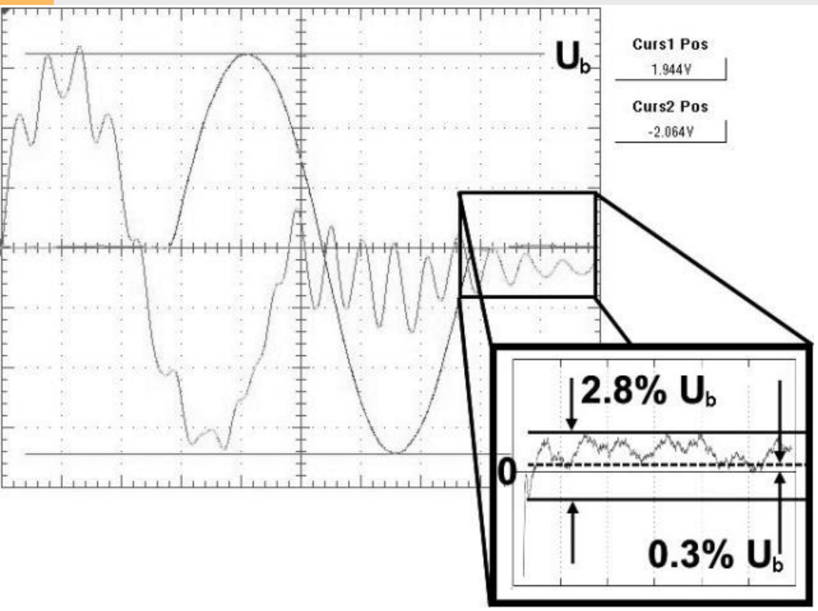


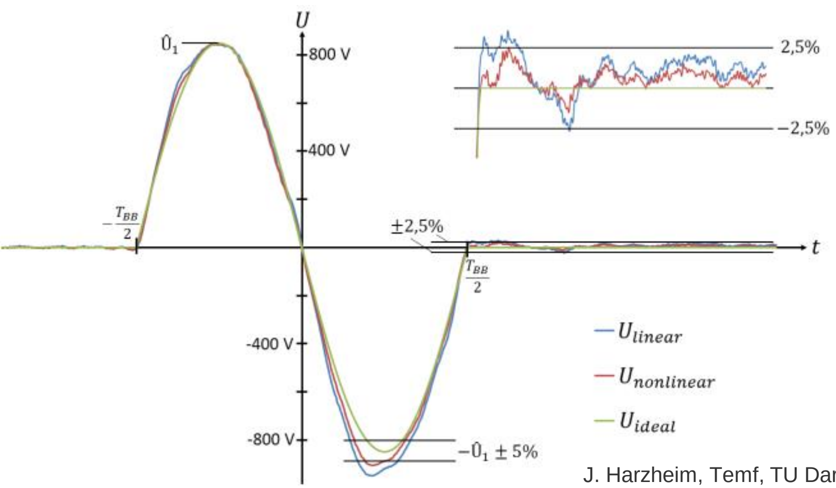
- signal generation must detect new trigger while output still active
- -> 2 alternating signal generators



K. Groß, H. Klingbeil, Temf, TU Darmstadt

ESR BB system – full system results I





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linear pre-distortion:

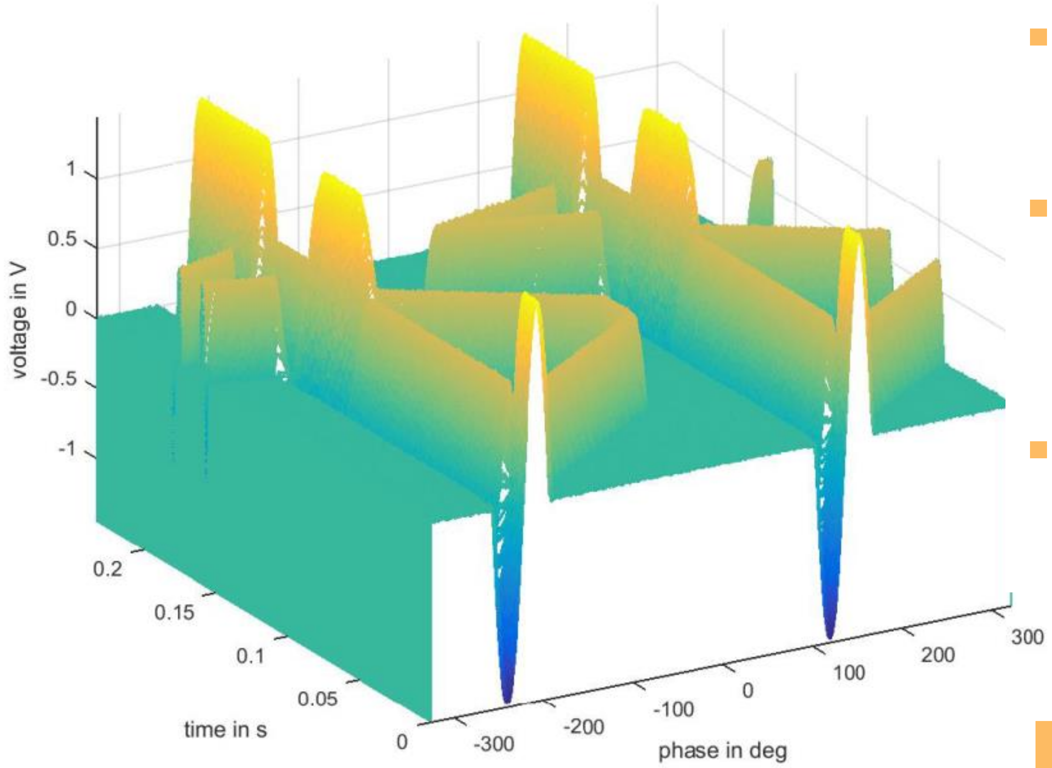
- U_b=520 V
- good quality

non-linear pre-distortion:

- U_b=800 V
- improvement in ringing after pulse
- symmetry insufficient (internal amplifier limitation?)

ESR BB system – full system results II

- phase shifting of moving barriers demonstrated with full system (manual data supply from PC to SCU)



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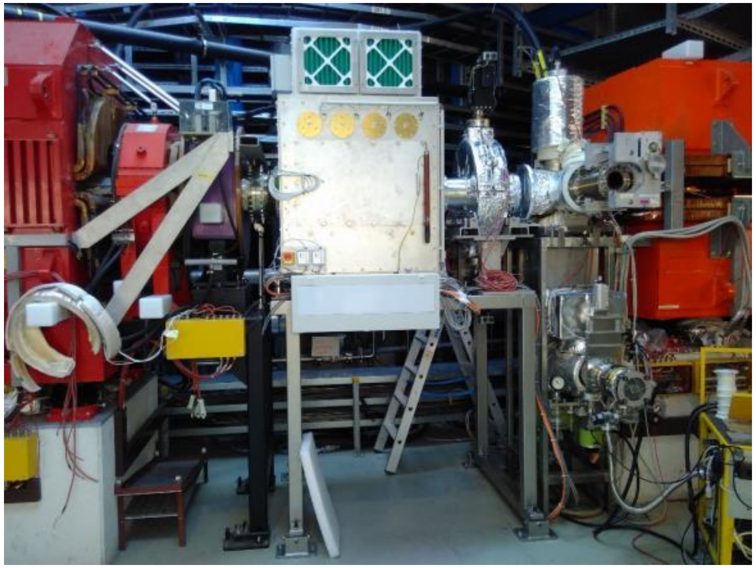
- two revolution periods are shown
- here barriers are created at equal phase angle (amplitude doubles)
- one barrier is shifted by 180° in both directions

full system works as intended!
-> installation appproval

ESR BB system – status + outlook

status:

- function of full system demonstrated
- pulse amplitude U_b=520 V with high quality achieved (1 kW amplifier)
- installation in ESR finished



to do:

- software development for unit controller (task: e.g. calculation of pre-distorted waveforms, control of signal generators)
- adaption of control system connection (e.g. phase ramp in FESA-class for ramped-devices?)

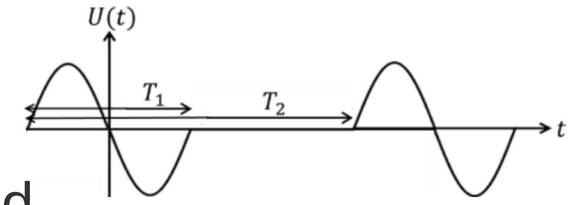
outline

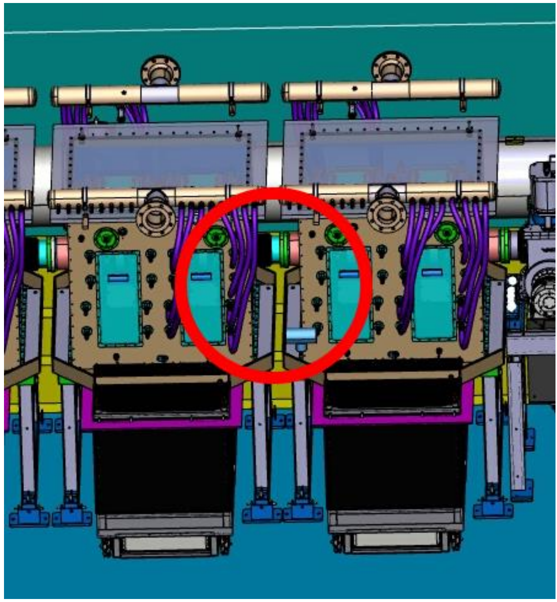
procurement starts 2019

- ESR BB system
- SIS100 BB system: pre-development phase
  - requirements
- SIS100 BB cavity design
  - oil cooling
- SIS100 BB power amplifier design
- SIS100 BB simulation results
  - frequency domain
  - time domain
- SIS100 BB outlook

SIS100 requirements

- creation of 2 barriers in two empty buckets -> single sine pulses of T_1=666 ns (f_{BB}=1.5 MHz)
- flexible control of amplitude and repetition period T_2 between f_{rep}=110 kHz and f_{rep}=270 kHz
- pulse amplitude $\hat{U}$ =15 kV
- maximum beam impedance 1000 Ω (cavity+amplifier)
- cavity length <1.3 m, but only 1.0 m for housing (due to feasibility of flange mounting)
- usability of identical cavities and amplifiers for SIS100 Longitudinal Feedback workpackage





SIS100 BB cavity design

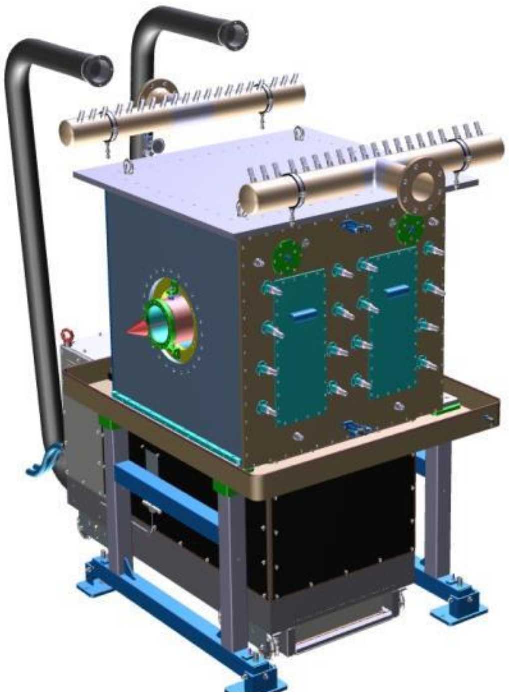
design goals:

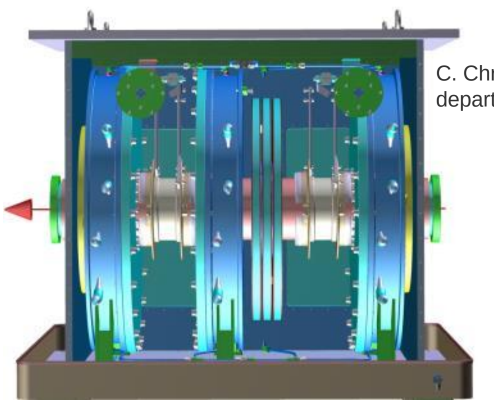
- broadband behaviour (-> MA cores)
- voltage gradient 15 kV/m (MA cores)
- matching with tetrode amplifier at tetrode´s working point
- cavity´s resonance frequency at or below barrier-bucket frequency f_{BB}

=> very similar to SIS18 h=2 cavity requirements!

working hypothesis:

- use h=2 cavity with less MA cores in order to increase resonant frequency



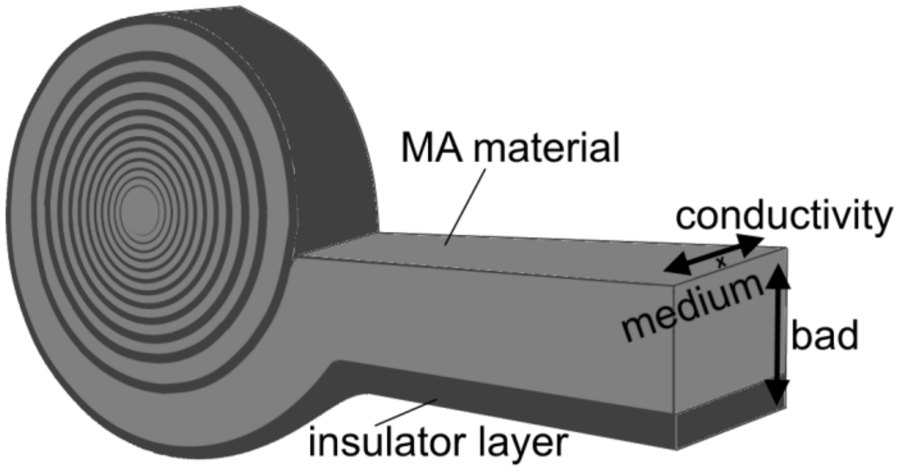


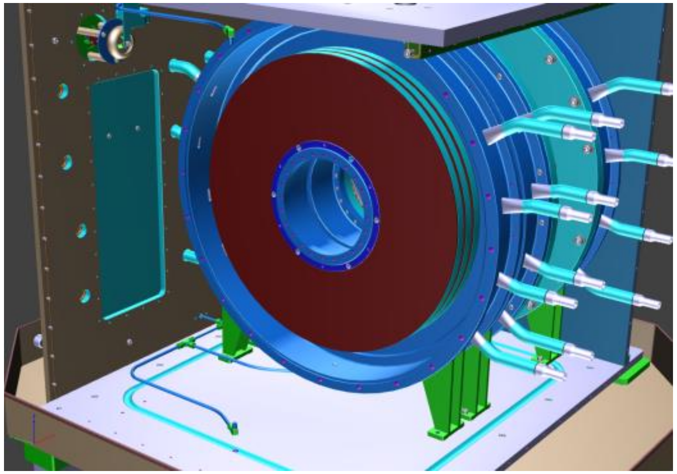
C. Christoph, RRF department, GSI

SIS100 BB – oil cooling

- due to magnetic loss effects, ring cores heat up during operation
- heat conductivity in FT-3M is anisotropic

P. Hülsmann, RRF department, GSI





- heat can only be removed through side surface, which is not flat
- insufficient heat transfer to cooling disks or air makes direct liquid cooling (oil) necessary

outline

- ESR BB system
- SIS100 BB system: pre-development phase
  - requirements
- SIS100 BB cavity design
  - oil cooling
- SIS100 BB power amplifier design
- SIS100 BB simulation results
  - frequency domain
  - time domain
- SIS100 BB outlook

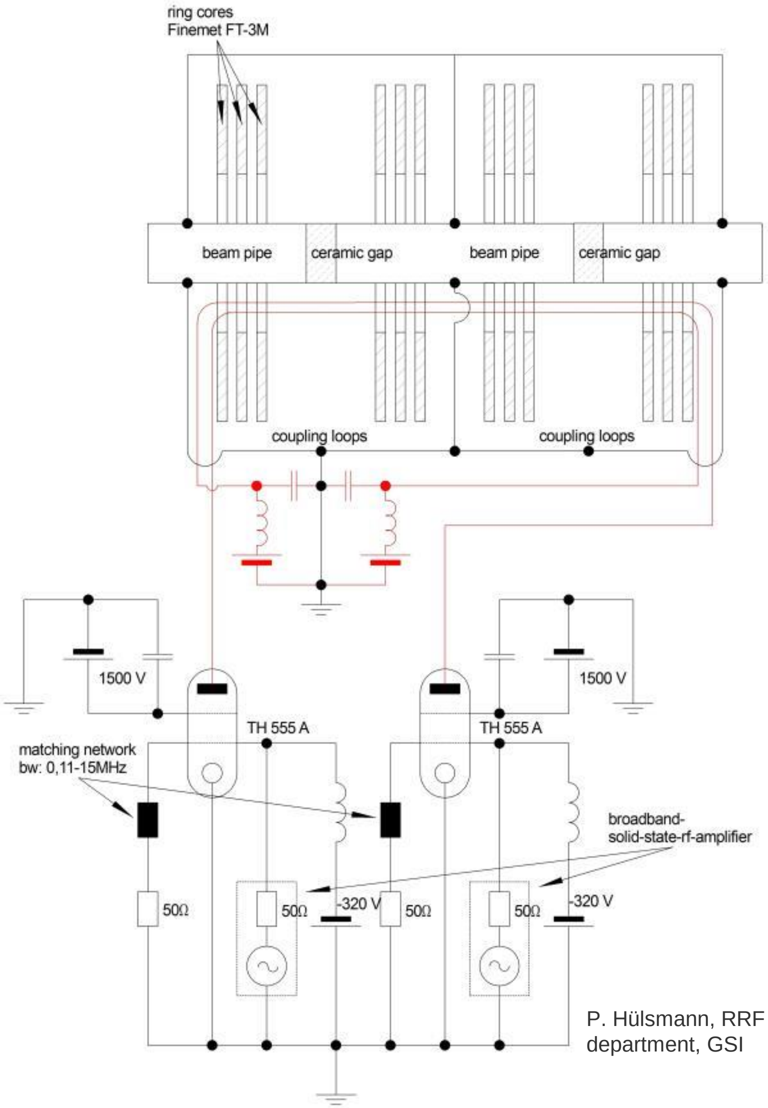
strategy:
- PSpice simulation of planned SIS100 BB cavity system
- comparison with measurements from mock-up of SIS100 BB cavity (with h=2 components)

SIS100 BB power amplifier design

- required signal quality
  -> class A amplifier (to avoid distortion in push-pull configuration)

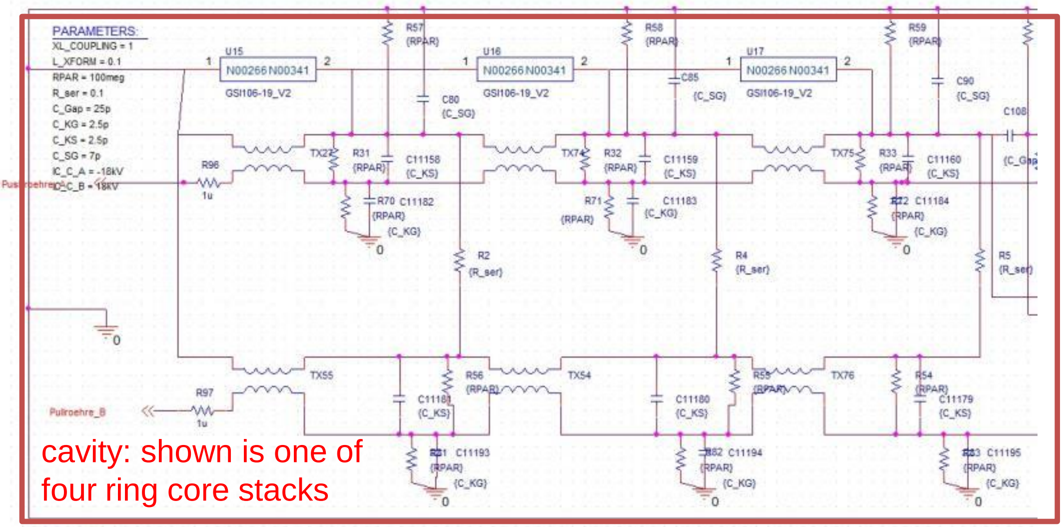
- tetrode capable of the expected anode dissipation power at working point above 15 kV -> Thales TH555

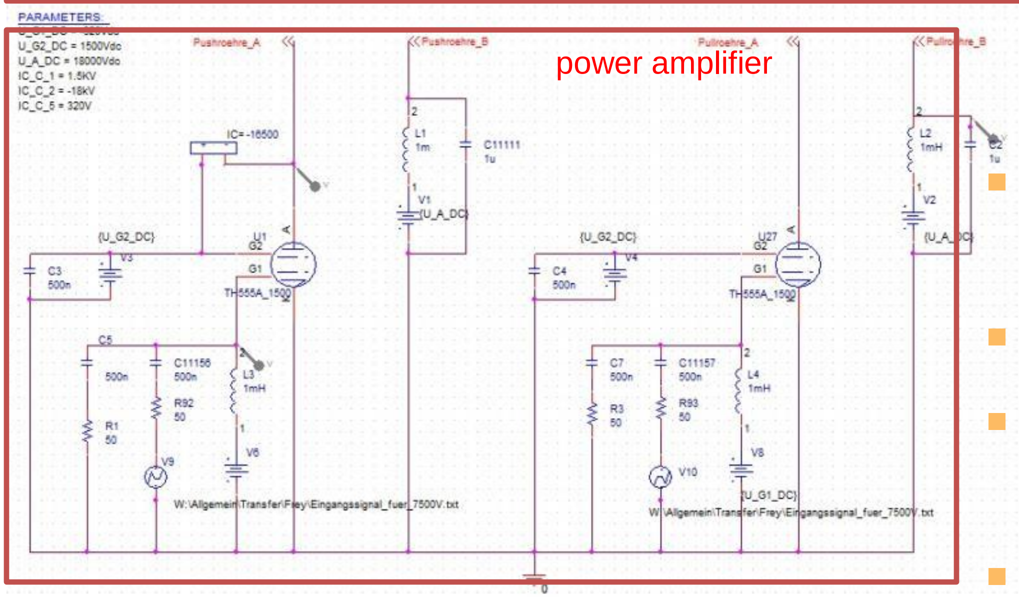
- compensation of anode currents by opposing winding directions of coupling loops

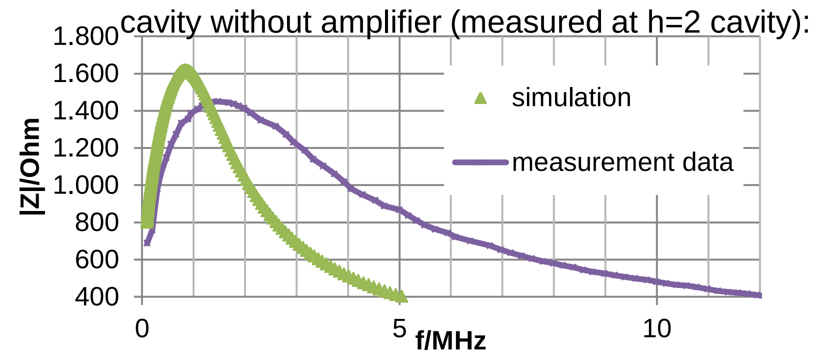


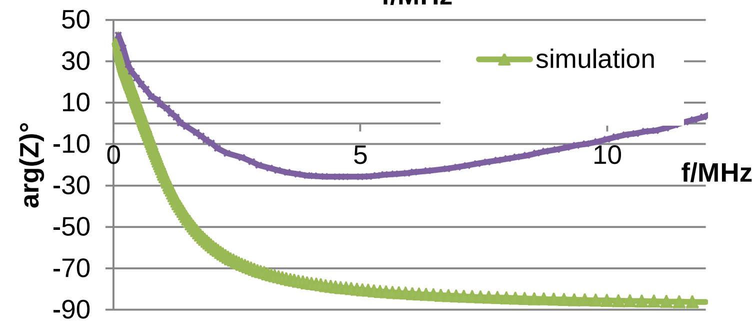
P. Hülsmann, RRF department, GSI

SIS100 BB simulation results – frequency domain



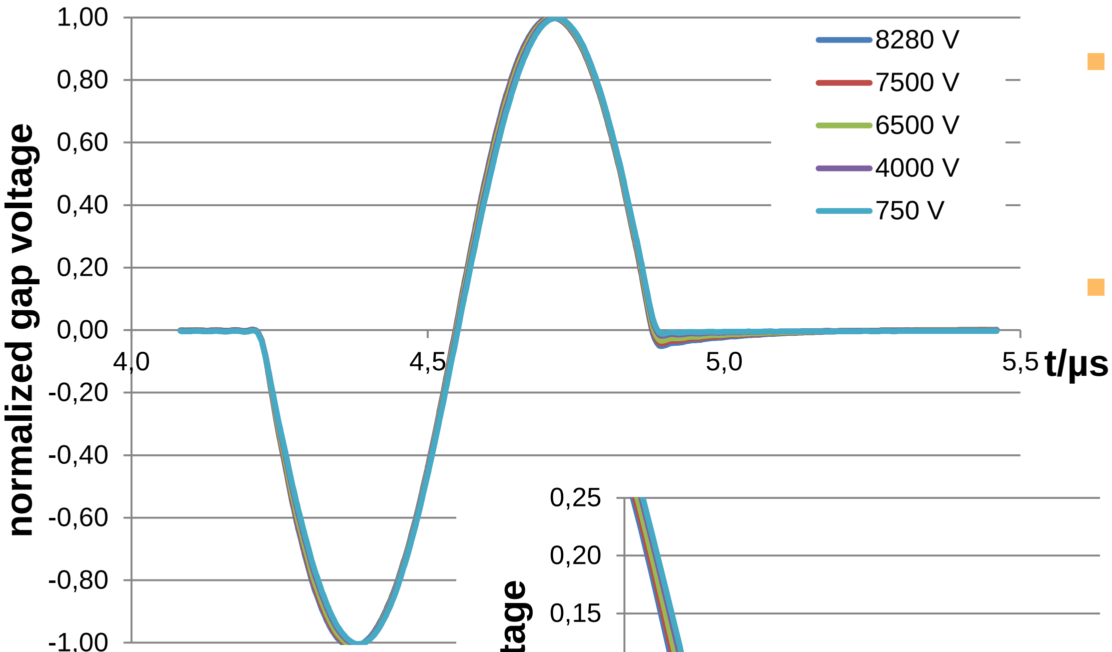






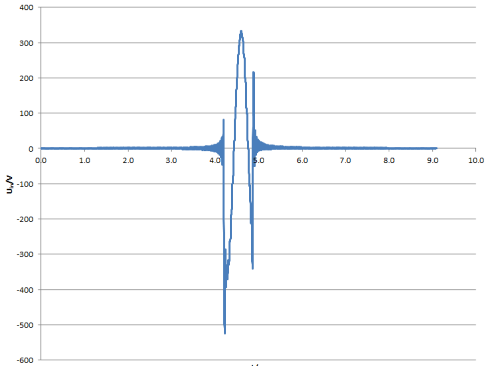
- tetrode model includes non-linearity
- deviations now understood
- sufficient matching between cavity and tetrode ($R_i \approx 1500\Omega$)
- resonant frequency $f_r \approx 1.5$ MHz

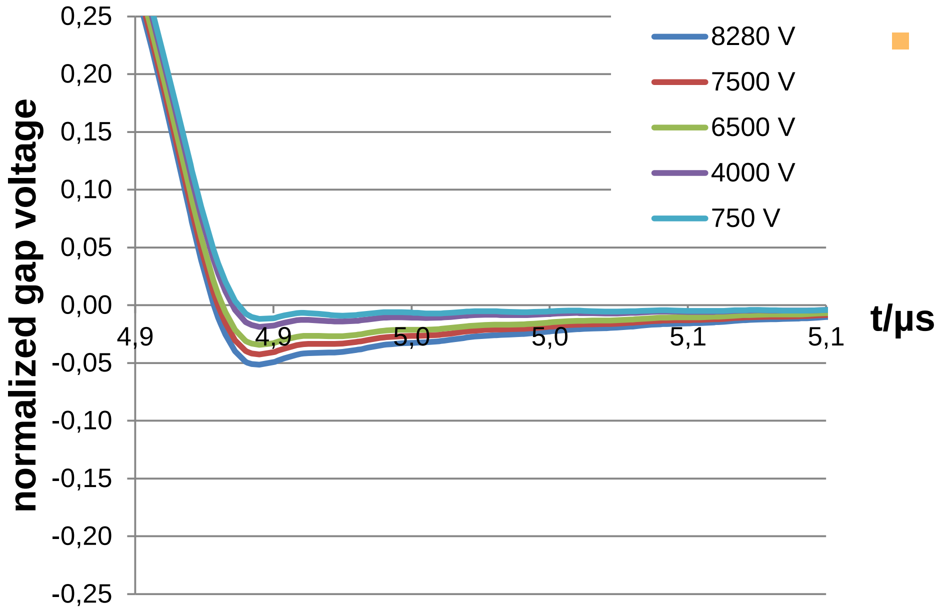
SIS100 BB simulation results – time domain



- desired pulse amplitude of 15 kV is achieved (7.5 kV across each gap)
- ringing at the pulse´s end is below 5% even with linear pre-distortion

input voltage in time domain
(linear pre-distortion, 0.02-30 MHz):



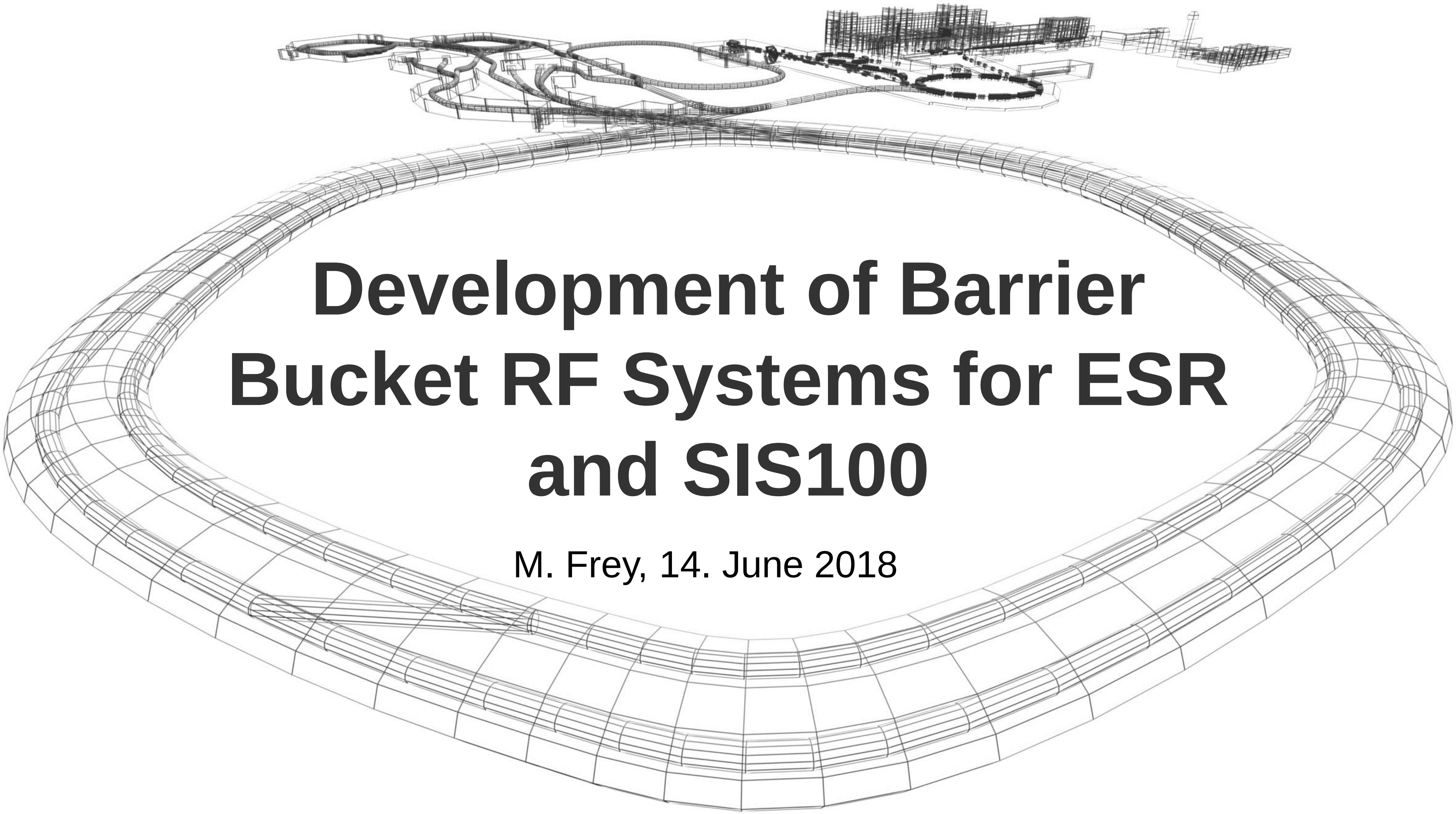


- desired bandwidth for input signal transmitting components: from 20 kHz to 30 MHz

SIS100 BB status and outlook

- Technical Concept document finished
- considerable effort was made to reduce technical risks by investigating (mostly at ARD broadband test cavity):
  - frequency dependent ring core properties
  - cavity bandwidth
  - ring core cooling
  - frequency- and time-domain simulations of full cavity/amplifier system
  - impedance reduction by cavity detuning
  - beam loading (effect of DC-fraction)
  - signal generation (LLRF system)
- Technical Concept proved feasible through all tests (15 kV, <5% ringing expected with non-linear pre-distortion)
- Detailed Specification 95% finished
- start of procurement is planned for June 2019

Thanks to all contributors

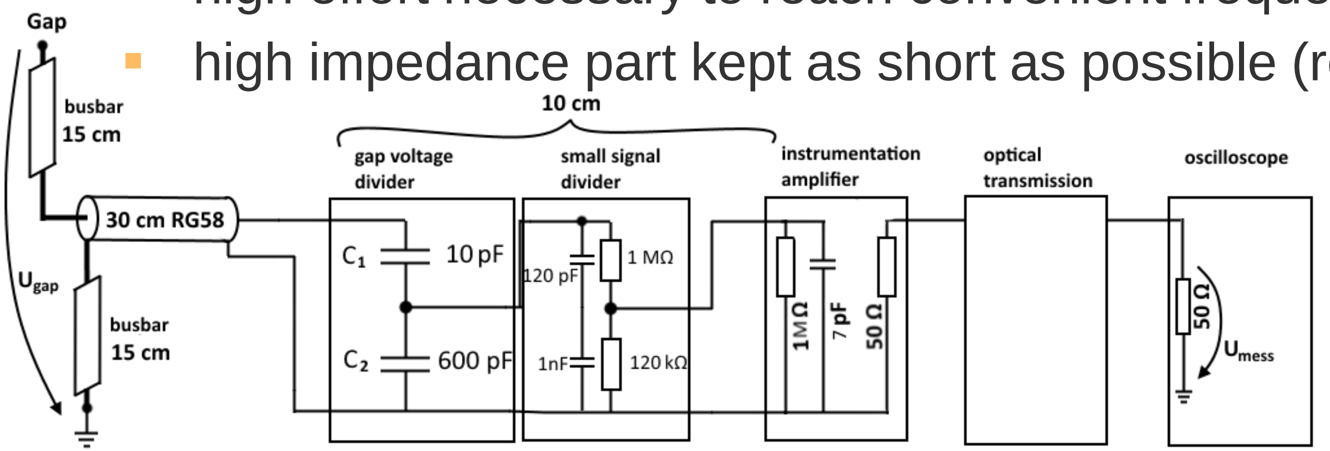


Development of Barrier Bucket RF Systems for ESR and SIS100

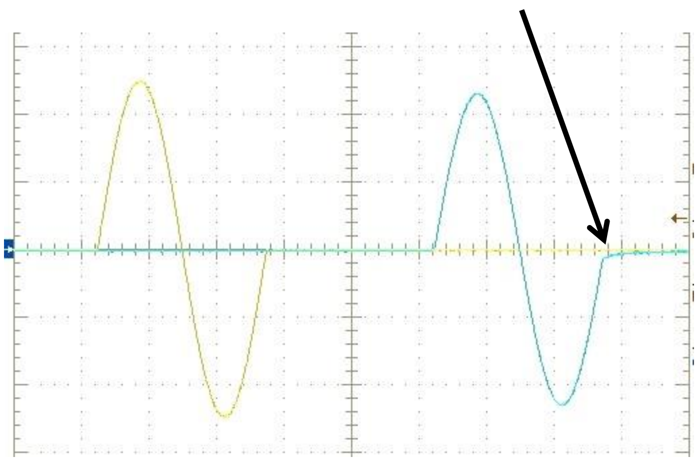
M. Frey, 14. June 2018

Appendix - gap voltage measurement

- distortion in measurement chain directly alters gap voltage signal
- high effort necessary to reach convenient frequency-response
- high impedance part kept as short as possible (reduce reflections)



130 m ½“ Cellflex: 5% distortion



2000 m optical fiber: 2% distortion (but synchronisation with SIS18 not possible yet)