

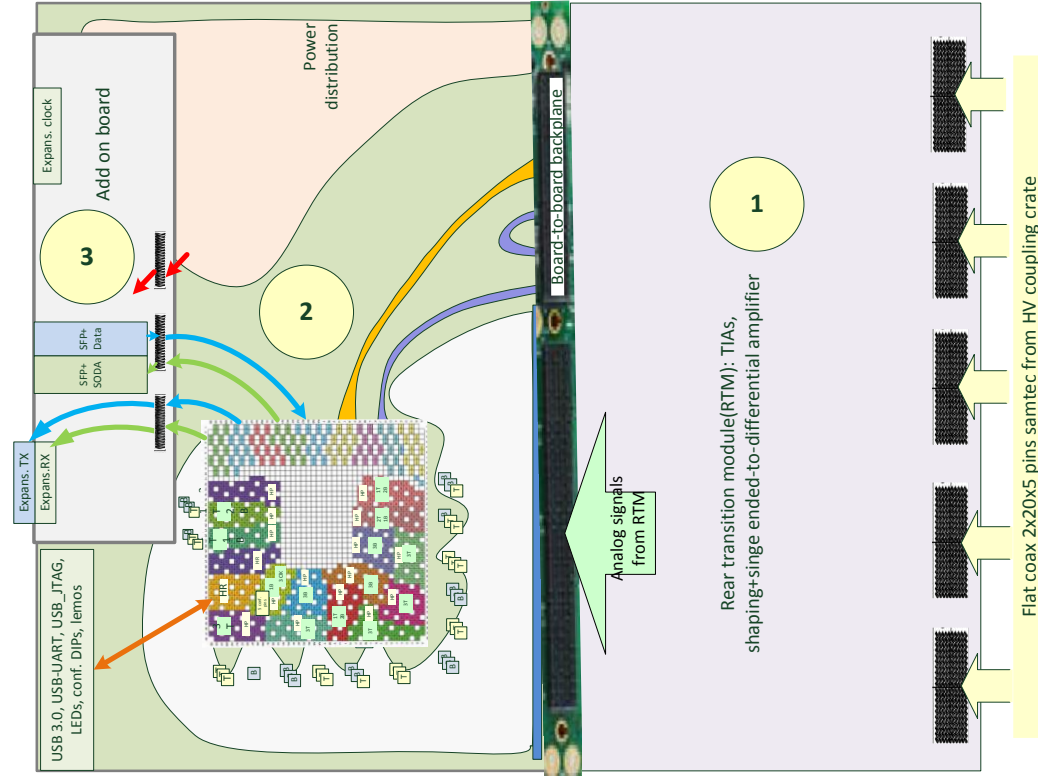
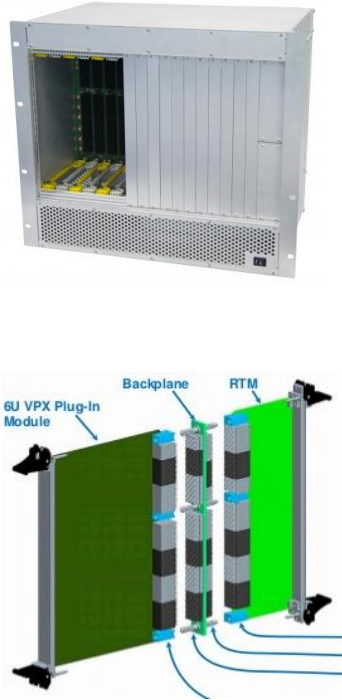
# Status of ADC based DAQ-System

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STT Readout Meeting

7 February 2018

# Crate and Board view



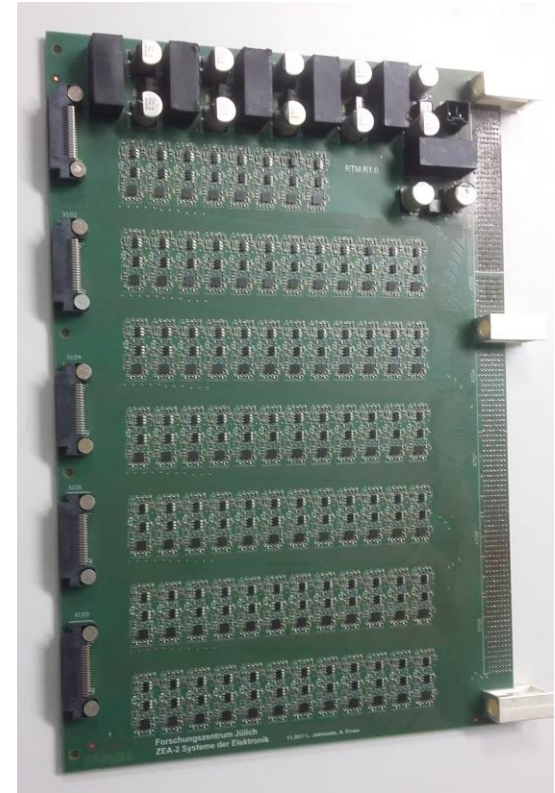
# Status Crate

- OpenVPX-based crate  
from ELMA
- Modification of backplane  
for our needs
- Received



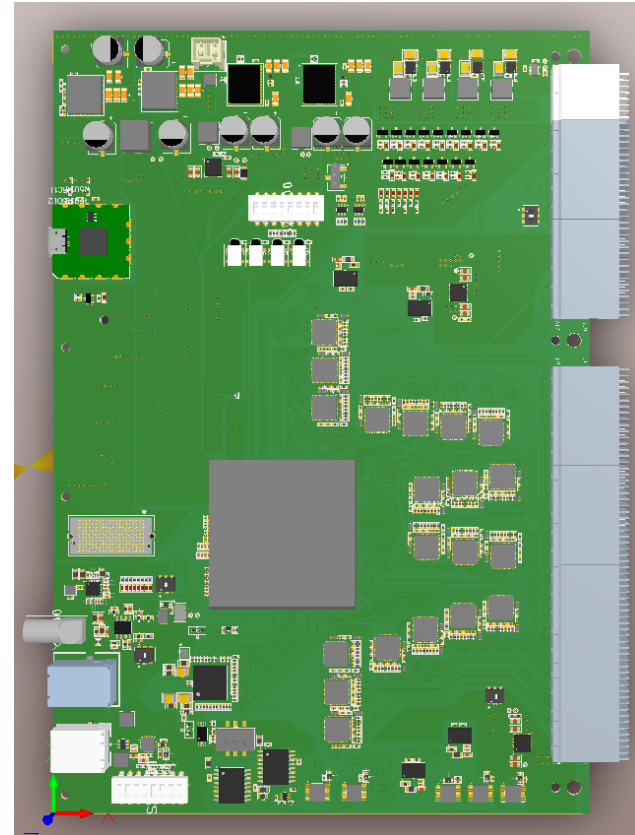
# Rear Transition Module

- Received produced hardware from external provider
- Modification of hardware was required  
(problems with backplane connectors)
- Power supply and amplifier stages under test in lab



# Front Module

- Layout of board done (remember, very complex board with 160 differential input pairs and 320 differential pairs for ADC $\leftrightarrow$ FPGA with length compensation)
- PCB in production, delivery expected at 13.2.
- Board assembly will start immediately at ZEA-2, beginning with power supply



- Several unexpected challenges, we worked hard on it, but we could not avoid delays
- Unrealistic to get a running hardware (tested in the lab, build up at COSY and tested with cosmics) within 12th March

→ decided to skip the tests in March and to be ready at the second week of beam time in April

## Configuration for beam test in 2018

- Time sorted and dedicated raw mode
- Running without controller
- Workstation will be used for controlling measurement and taking data
- Each module (160 channels) will have an uplink over USB 3.0 to workstation
- Data rates: max 300MB/s over USB3-link
- Modules are synchronized over backplane connection