CURRENT READOUT STATUS

- ASIC/TRB System
- ADC-based System

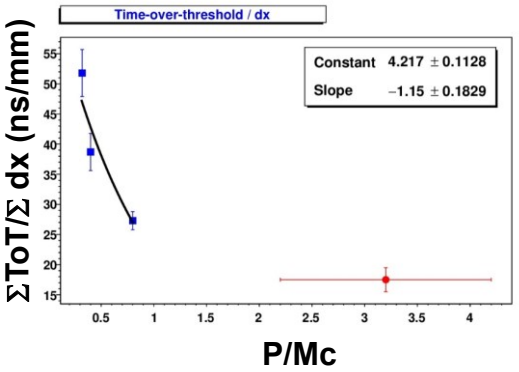
READOUT STATUS

- ASIC/TRB

  - HW achievements
    - PID by standard TDC system (TRB), time readout: LE-time + TE-time
    - specific frontend chip developed: PASTTREC, SW controlled (FPGA)
    - compact FE-boards, low power (~ 30-40 mW/ch)
    - Stable operation, several straw test systems (Krakow, Julich, ..)
    - Data links sufficient for PANDA phase-1
    - Data concentrator stage in progress, commercial HW identified, scheme developed
    - Complete readout system scheme (phase-1)

READOUT STATUS

- ASIC/TRB



  - Results
    - Deuteron beam & cosmics, 144ch test system
    - dE/dx separation (PID) by time/threshold demonstrated
    - Full dE/dx dynamic range covered (~ 5-50 keV/cm)
      - PID separation power by ToT (deuteron data, prelim., lower limits)
        - S ~ 5* (K/p @ 390 MeV/c, TDR: S ~ 8, w/ 10% dE/dx resol., best case)
        - S ~ 9** (π/p @ 300 MeV/c, TDR: S ~ 13)

*1.5 & 0.75 GeV/c deuterons
**0.6 GeV/c deut. & cosmics

    - Spatial (isochrone) resolution: σ = 130 – 140 µm (deuteron & 1 week cosmics)
  - Analysis SW status
    - Calibration procedures developed (time-over-threshold, BL/thresh. adjusting)
    - PID separation observable (e.g. Σ ToT/Σ dx, truncation, ..)

READOUT STATUS

- ASIC/TRB

  - In progress
    - PANDA-DAQ integration, data concentrator stage added (HW)
    - Straw & EMC test system set up with DAQ in Krakow
    - FE-layout, cooling & cabling scheme

  - Open
    - TRB3 not sufficient for full lumi (phase-2)
    - Next generation TRB system expected (likely already for phase-1)
      - Better FPGA capabilities (DC-stage)

READOUT STATUS

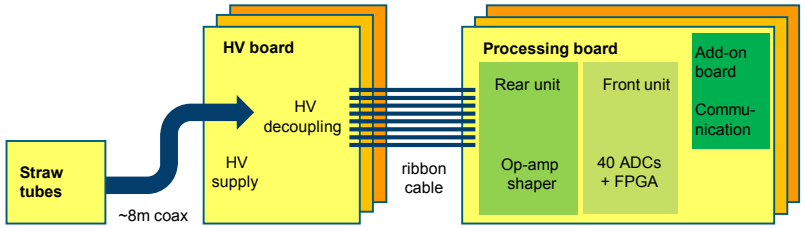
- ASIC/TRB

  - Phase-0 straw stations at HADES with ASIC/TRB readout system
    - ~ 1600 channels
    - Set up by end 2018

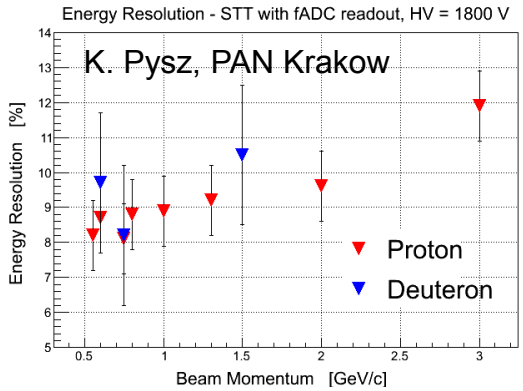
  - Spin-offs, RO system adopted & exported
    - MUSE@PSI experiment:
      - PASTTREC-FEB and TRB, 4000 channels, 500 ASICs in order
      - (also PANDA straw designs & techniques)
    - MDC@HADES:
      - PASTTREC readout tests done
      - likely: replacement of ASD8-HW by PASTTREC-FEB

READOUT STATUS

- ADC-based system (“FEE-free“)



  - Achievements
    - STT-specific HW scheme finalised (“inaccessible central tracker“)
      - All RO HW backend and accessible (amps, HV capacitors)
      - Individual straw channel accessible from outside (cut single lines w/ broken ch)
      - Minimal FE-space required, no cooling: bEMC closer to target
    - Custom-specific RO board design
    - Full waveform information
      - LE time (const. frac.), pile-up, max. amp, TE-time, ..
    - dE/dx resolutions demonstrated (240 MHz FADC)
      - larger dynamical range: pulse width → pulse area
    - Spatial resolution expected (slightly) better (LE-fit)



READOUT STATUS

- ADC-based system (“FEE-free“)
  - To be done
    - “completely new system“: full system test
    - reliability, proof of all components
    - FPGA processing capabilities: high rates & eff. peak search ..
      - demonstrate deadtime-free readout (SW)
      - particle bursts, heavy ionising, ..
    - resolutions, dE/dx separation to be demonstrated
    - calibration method, BL / noise level for individual channel, ..

READOUT DECISION CRITERIA

- Tech. specifications
- Performance (phase-1 → phase-2*)
- Costs
  - incl. spares (~ 5-years running)
  - production costs (incl. MP), no design costs
- WP definition
  - technical aspects, tasks, ..
  - MP needs (production, installation, operation, maintenance)
- WP association & responsibility
- AIM: no WP left open after RO decision

* phase-2 = full luminosity, phase-1 ~10%