Contribution ID: **38** Type: **not specified**

# Progress in the simulation of Resistive Plate Chambers with multi-strip read-out

*Wednesday, 10 February 2010 15:10 (20 minutes)*

RPCs in Multi-strip fashion are widely regarded as very convenient designs for covering large areas under low track multiplicities. It will be shown, from the perspective of Multi-gap structures and high accuracy timing, how the strip impedance, weighting field profile and cross-talk are very important limiting factors of this kind of designs. Comparison of avalanche simulations with published data will be presented, aiming at emphasizing and illustrating the above-mentioned effects. Recent results from optimized Multi-strip structures will be presented to show how these potentially 'limiting factors' can be minimized or even virtually suppressed by convenient choices.

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**Session Classification:** R & D in narrow-gap RPCs (II)