Contribution ID: **63** Type: **not specified**

Development of High Resolution Readout Electronics for MRPC

Friday, 12 February 2010 12:30 (20 minutes)

High resolution readout electronics is under development for MRPC detectors. It consists of a fast front-end ASIC and an ultra high resolution TDC based on FPGA. The front-end ASIC, CAD (Current Amplifier and Discriminator), works in fully current mode. Signal pulses are amplified by a current mirror with local negative feedback to reduce the input impedance and then are sent to a current comparator. Current mode design can achieve higher bandwidth with less power consumption compared to voltage mode approaches. The chip is designed in a 0.35μm CMOS technology but this architecture is well suited for deep submicron technologies with lower supply voltage.
In order to obtain time resolution of ~10ps in a FPGA TDC, a delay chain is used to interpolate time phases inside a clock. But it usually suffers from bad control of the delay time for each delay unit. The so-called wave union method is used to improve the linearity and the resolution.
The detailed the design and test results will be present in this paper.

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Session Classification: Gas systems and ageing (II) and digital systems