Status of GSI FEE Projects for PANDA

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Outline

Serial Adapter ASIC

Motivation

- Currently two different serial interfaces are foreseen to be used inside the barrel:
  - I^2C for High voltage DACs
  - APFEL serial configuration interface
- Both interfaces use single ended lines
  $\Rightarrow$ need ground connection $\Rightarrow$ Risk of ground loops
- Both interfaces are not compatible $\Rightarrow$ Requires additional cabling inside the magnet.

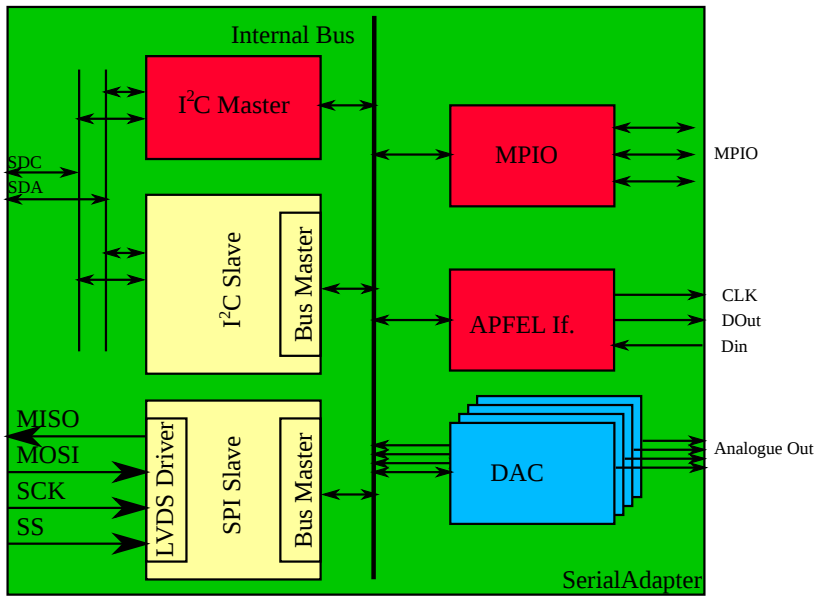
Wish for an adaptor circuit with additional analogue features raised up.

$\Rightarrow$ Integration of 10 bit DACs for HV adjustment.

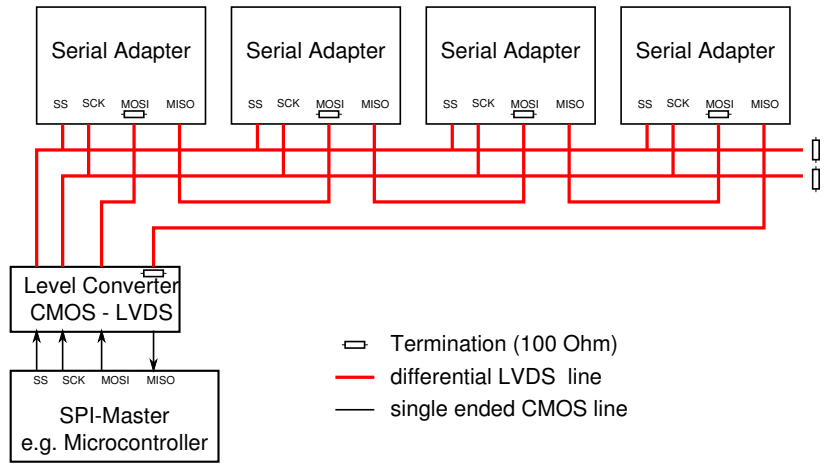
Chip Architecture

Global Architecture

Build an adaptor circuit with a common back end and front ends for I^2C, SPI and APFEL serial configuration interface



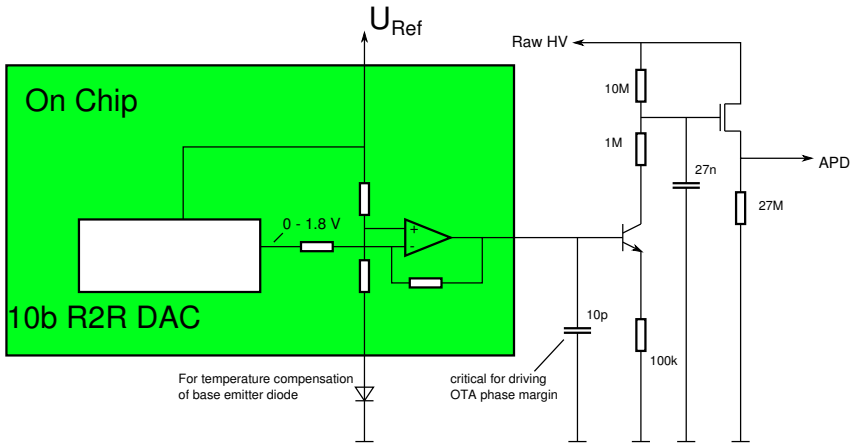
SerialAdapter Block Diagram



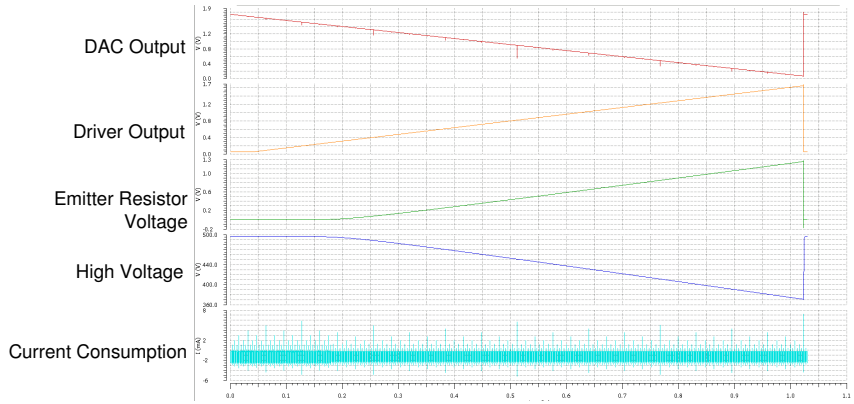
SPI back end connection

Chip Architecture

Analogue Part



Circuit of HV Adjustment

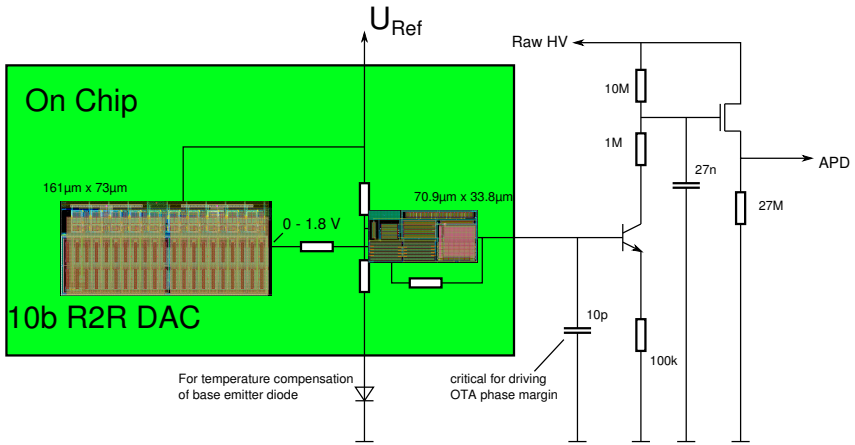


Spice Simulation

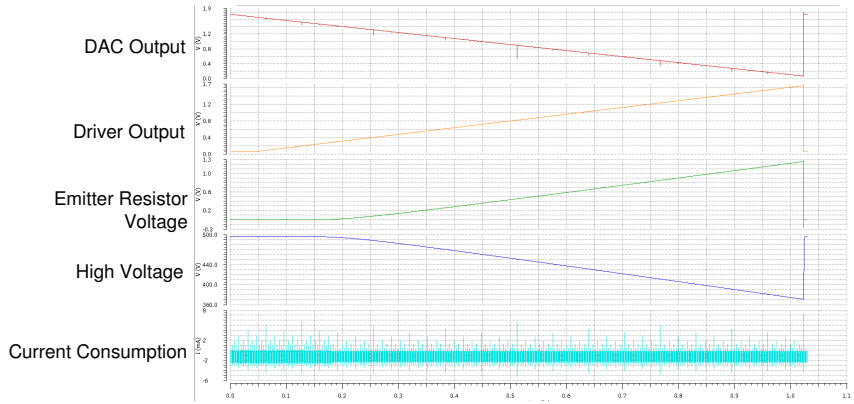
- 10 bit R2R DAC already used in several ASIC projects
- OTA design taken from HitDetection
- Same external circuit as on current HV distribution PCB

Chip Architecture

Analogue Part



Circuit of HV Adjustment



Spice Simulation

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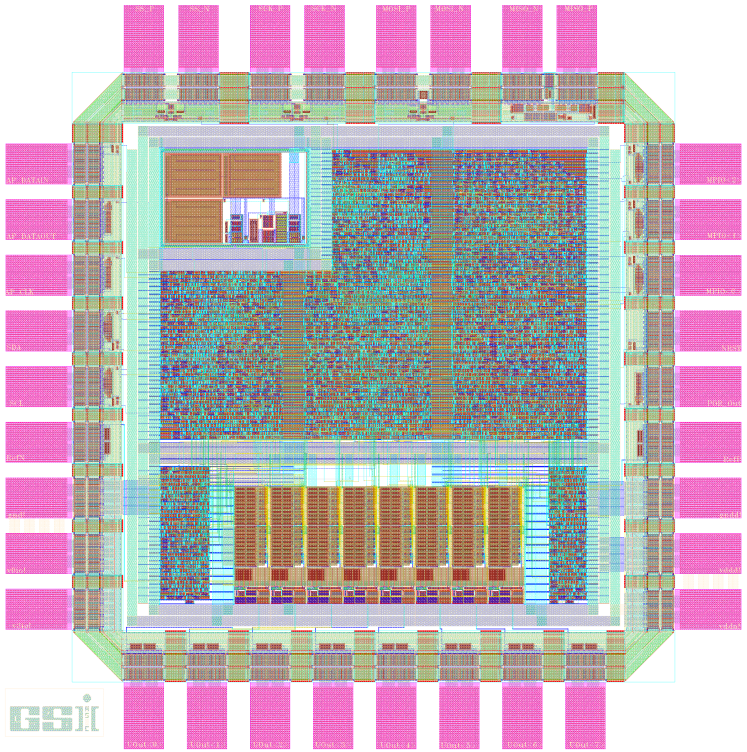
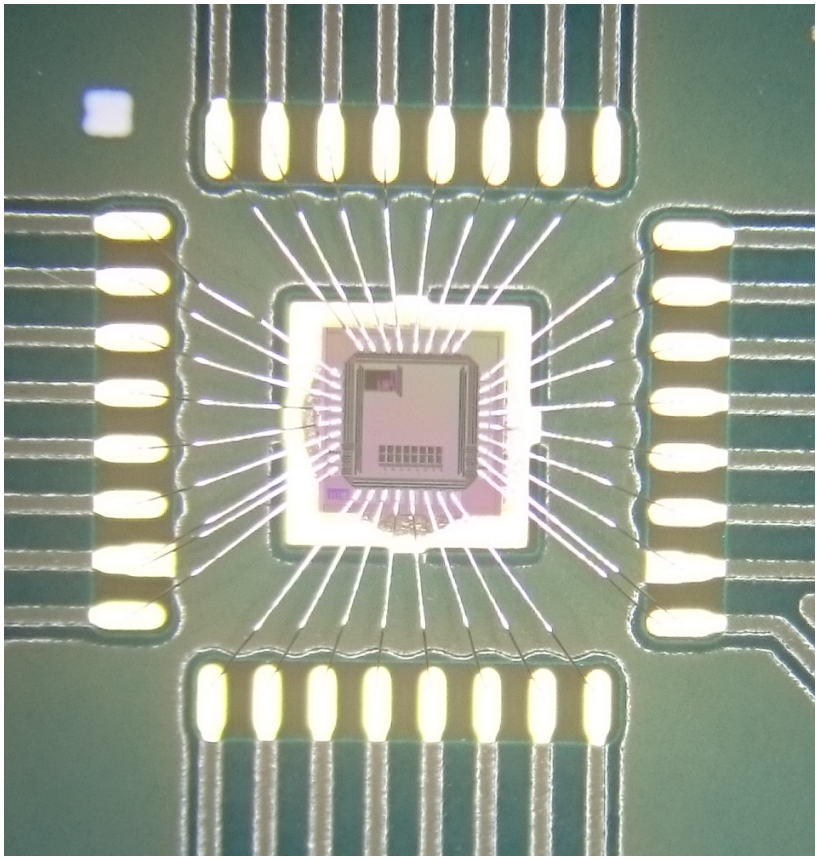
Status and Schedule

- First Idea: March 2016
- Project launch with financing by University of Bonn after September CM meeting in Mainz
- November 28th: Dead line for tape out
- $1.5 \times 1.5\ \mathrm{mm}^2$ Mini ASIC in UMC 180 nm CMOS technology



Status and Schedule

- Delivered in April 2017
- Digital tests by Christoph Schmidt @ HISKP Bonn
- All digital tests successfully!
- Functional test of DACs successfully
- Testsetup with ASIC included in HV distribution in preparation
- Applications in any other subsystem?



HitDetection ASIC

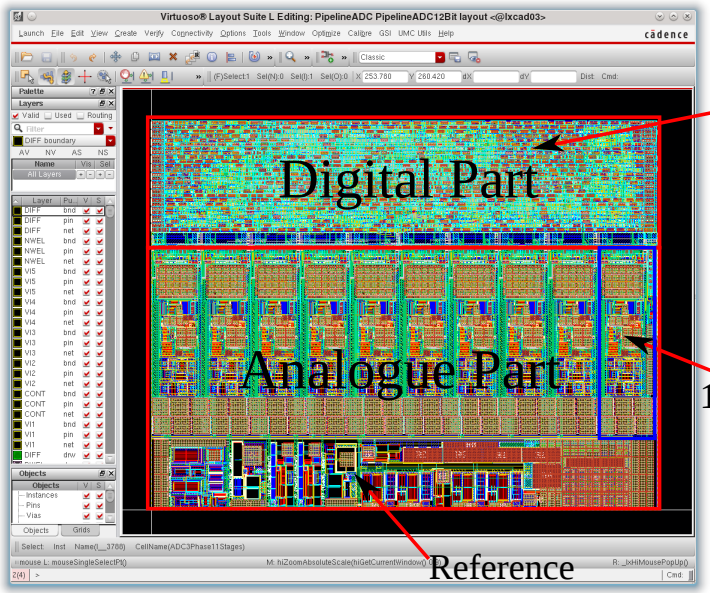
HitDetection V1.00

- Results of HitDetection V1.00 have been presented on FEE-DAQ-Workshop 2016
  - HitDetection V1.00 is operational, sampled APFEL-pulses have been shown
  - Bad linearity of ADC $\Rightarrow$ probably gain mismatch of pipeline stages

HitDetection ASIC

HitDetection V2.00

- Redesign of 12 bit pipeline ADC



On chip digital calibration

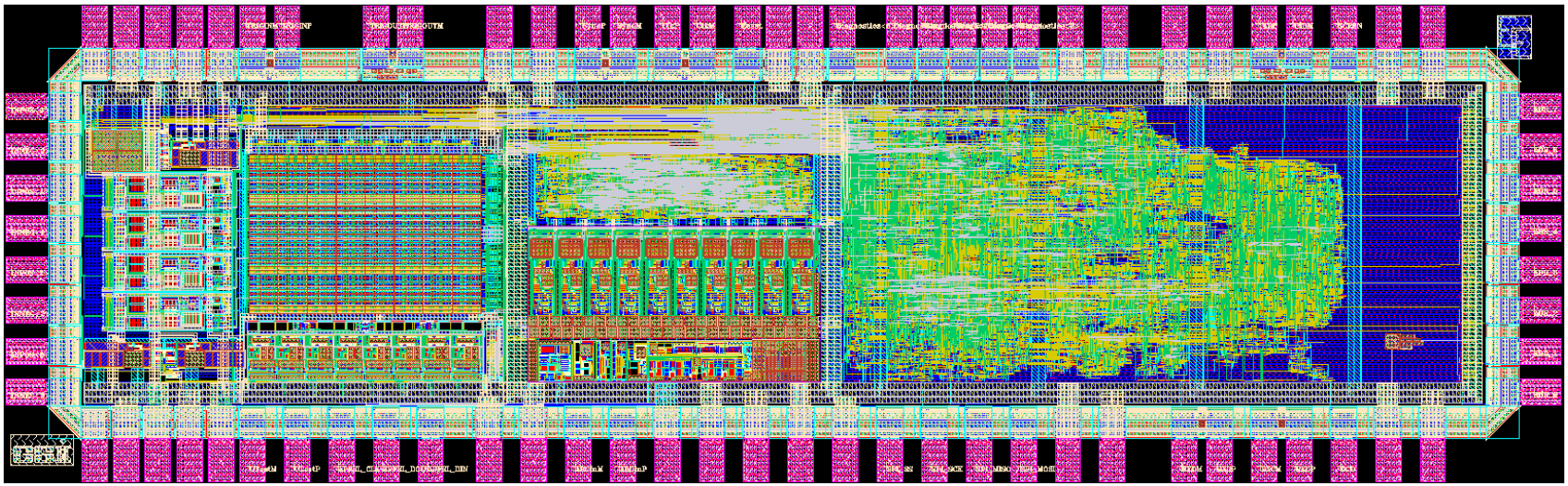
1.5 bit pipeline stage

- Digital gain calibration of each pipeline stage
- Automatic calibration factor determination after power up

HitDetection ASIC

HitDetection V2.00

- HitDetection V2.00 is produced and currently under test
- Communication to HitDetection 2.00 established
- HitDetection works stabil, only some minor bugs found
- Characterisation is in progress with support by O. Noll and P. Grasemann from HIM



HitDetection ASIC

Chip Characterisation

Measurements already done:

- Static linearity of ADC: INL $\leq \pm 3$ LSB
- Static noise of ADC: 1.8 LSB RMS
- 3rd harmonic surpression > 60 dB
- Dynamic linearity of ADC: 9.8 ENOB
- Improvement by digital calibration observable

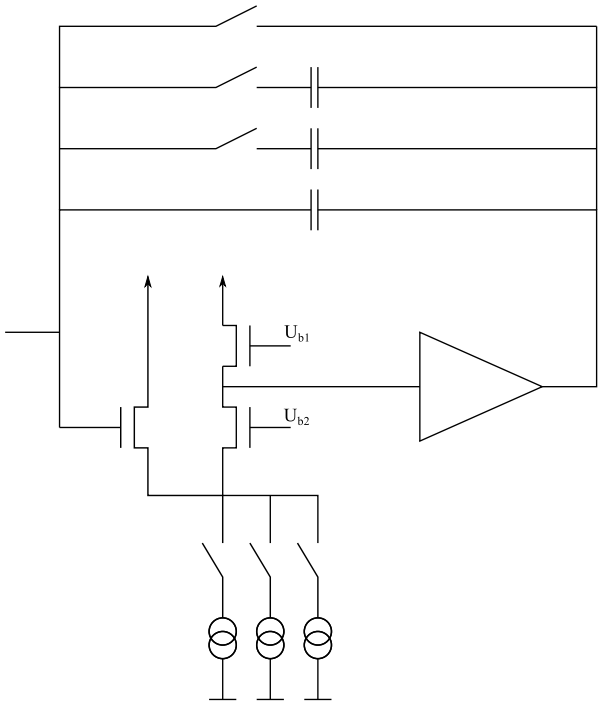
To be measured:

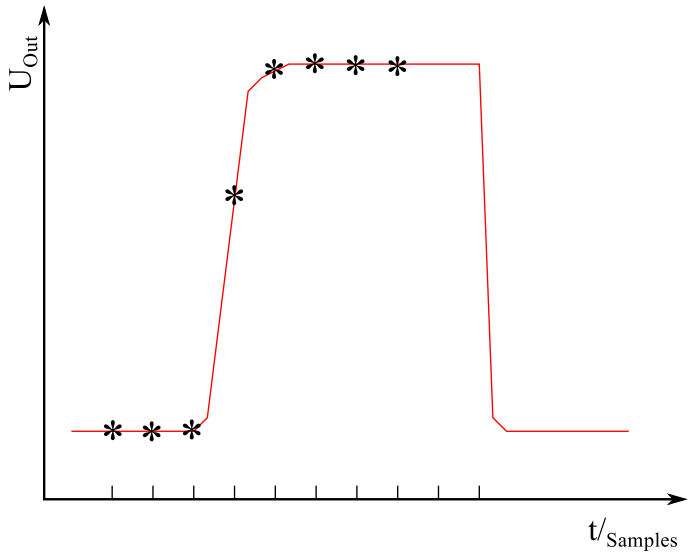
- Threshold Scan of analogue inputs
- DC measurement of analogue memory to determine cell offsets
- Dynamic measurements of analogue memory + ADC with sine input
- Performance characterisation with APFEL signals
- readout of EMC crystals

HitDetection ASIC

Plans for 2017

Replacement of input buffers by configurable charge sensitive amplifier





Tape out end of this Month (Sep. 25th)

Thank you for your attention