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Status of Sub-Systems General FEE Status Current Issues

FEE Coordination

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Status of Sub-Systems General FEE Status Current Issues

Outline



2 General FEE Status



- Irradiation Tests
- EMC (Electro Magnetic Compatibility)



- MVD
 - Readout ASIC development continues at INFN Torino
 - A new Strip read out ASIC will be designed by INFN designers, supervised by Gianni Mazza
- STT & Forward Tracking Two options for STT:
 - ASIC-Read out with PASTREC and TRB3
 - ADC Readout

Decision planned to be taken in 2018

 \Rightarrow Working group implemented

For Forward Tracker ASIC Readout is foreseen

- Second Iteration of PASTREC is available, works reasonable for prototypes
- Currently no manpower for designing third iteration available



- Planar GEM Tracker
 - First FEE prototype based on nXYter ASIC
 - Lack of man power!
- Barrel Time of Flight
 - Electronics based on TOFPET ASIC in development
- Endcap DISC DIRC
 - Electronics based on TOFPET ASIC in development



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Status of Sub-Systems

Barrel DIRC, courtesy of Carsten Schwarz

FEE: Barrel DIRC

This weeks, the barrel DIRC tests the prototype with beam at CERN





Status Reports

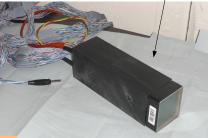
Barrel DIRC, courtesy of Carsten Schwarz

The readout-system for the Barrel-DIRC is in moment the **TRB3 with PADIWA** discriminators. The prototype uses \sim 800 channels.

The Channel-Plates and the PADIWA discriminators are assembled as a module and thresholds are constant within 0.2 mV over days.

This is not the final FEE setup, we plan to use in future the DRICH.





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FEE Coordination

- Forward RICH
 - Currently PADIWA and TRB3 used
 - DIRICH foreseen as future readout system
- Forward ToF
 - Readout based on TRB3
- Barrel EMC
 - Front end ASIC APFEL 1.5 produced
 - Front end PCBs in production but delayed
 - Sampling ADC board by P. Marciniewski, HitDetection ASIC currently under characterisation as an option ⇒ See last talk
 - HV Distribution and backplane PCB under development at Giessen, New ASIC under tests: SerialAdapter ⇒ See last talk
- BWE EMC

Similar electronics as in Barrel EMC



• FWE EMC

- Discrete Preamps developed in Basel as analogue FEE in production
- Sampling ADC board by P. Marciniewski
- HV Distribution an backplane PCB under development at Bonn
- Forward Shashlyk Calorimeter
- Luminosity Detector
 - HV MAPS as detector / FEE
- Muon System
 - \Rightarrow See talk by Nikolay Zhuravlev

General FEE Status

- Read out concepts for all sub systems available
- For most detectors prototypes are available, few are even in production phase
- Very criticle issue: Read out ASIC development for MVD Fortunetaly good news from Torino

• Personal impression: Panda FEE is on a good way

Current Issues

Irradiation Tests

- Still many components are not radiation tested sufficiently!
 - γ -, xray- or e⁻-irradiation
 - accumulation of charge in oxides by ionising
 - Irradiation under biased conditions!
 - p- or n- irradiation
 - bulk damage \Rightarrow deep traps
 - Changes in doping properties (neutron induced doping)
 - single event effects (SET, SEU, SEL)
- Communication is needed to optimise irradiation effords
 - Which components are already irradiated
 - Who has access to irradiation facilities
 - Where are irradiation campaigns planned
- Irradiation data base discussed with Udo Kurilla



Current Issues

EMC (Electro Magnetic Compatibility)

- Electromagnetic Interferences might have a big impact on signal quality
 - Ground loops
 - PC board design
 - shielding
- PANDA FEE coordination as forum for sharing of knowledge
 - Where are engineers, electronics designers or physicists located who are experienced in this field?
 - Measurement equipment, simulation tools...
 - Could be a main focus on one of the next meetings
- How is this handled in other experiments?
- Ground loops also concerns back end electronics, DAQ-components, power suplies etc.

