Summary of the Grünberg Workshop

DAQT Part

09:30 - 10:00 DAQ Introduction *30'*
Speaker: Wolfgang Kuehn (JLU-Gießen)
Material: **Slides**

10:00 - 10:30 Panda Software Trigger Status (2015) *30'*
Speaker: Klaus Goetzen (GSI Darmstadt)
Material: **Slides**

10:30 - 11:00 Coffee Break

11:00 - 11:30 SODAnet *30'*
Speaker: Myroslav Kavatsyuk (KVI, University of Groningen)
Material: **Slides**

11:30 - 12:00 Burst Building Network *30'*
Speaker: Marcel Tiemens (KVI, University of Groningen)
Material: **Slides**

12:00 - 12:30 STT Tracking with FPGAs *30'*
Speaker: Yutie Liang (Giessen University)
Material: **Slides**

12:30 - 14:00 Lunch

14:00 - 14:30 Update of Compute Node Hardware *30'*
Speaker: Thomas Gessler (JLU Giessen)
Material: **Slides**

14:30 - 15:00 PCIe connectivity for Compute Nodes *30'*
Speaker: Simon Reiter (JLU Giessen)
Material: **Slides**

15:00 - 15:30 Modelling of the PANDA DAQ Network *30'*
Speaker: Mateusz Michalek
Material: **Slides**

15:30 - 16:00 Coffee Break

16:00 - 17:00 Discussion: Phase 1 Physics and Detector Configuration *1h0'*
Speaker: Myroslav (on behalf of Johan Messchendorp), Lars et al.
Material: **Slides**

17:00 - 18:30 Discussion: TDR structure, input, assignment of tasks *1h30'*
Speaker: Wolfgang et al.

The second day of the workshop was devoted to data acquisition and event filtering. We heard a talk by Wolfgang Kühn, presenting an overview of PANDA data acquisition and event selection, emphasising the points which need urgent attention with respect to the TDR. **He pointed out that it is crucial to define both physics and detector configuration for Phase 1 running. In the discussion, we agreed to start with a selection of up three typical benchmark channels with different topologies and different requirements with respect to the luminosity. Event filtering will depend strongly on the detector configuration and the physics channel. It is, however, clear that even for Phase 1 luminosity, event filtering has to be shared between the FPGA level and the CPU/GPU farm level.**

Following this discussion, we heard a talk by Klaus Goetzen, reminding us of the software trigger status. Unfortunately, due to the lack of manpower, not much work has be done since 2015. I**n the discussion, it was pointed out that we need software trigger simulations for the benchmark channels which will be selected for the DAQ TDR. Finally, it was pointed out that the goal should be suppression of events which are not interesting rather than trying to improve the signal/background ratio for interesting event at the expense of efficiencies. This needs to be done on a case-by-case basis and there can be no global event filtering which would permit to run the full physics programme, spanning many orders of magnitude for the cross sections at the same time.**

After the coffee break, we hear talks by Myroslav Kavatsyuk, reviewing the features of SODAnet , providing clocking and synchronisation, slow control of FEEE and punching of collected data. Furthermore, he showed test results verifying the long term stability of **SODAnet, which is better than 30 ps, fully meeting the requirements of PANDA DAQ. SODAnet implementations are available for a variety of FPGAs, including Lattice ECP3, Xilinx Kintex 7 and Xilinx Virtex 6.**

This talk was followed by a presentation of **Marcel Tiemens about the implementation of the burst building network for the EMC**. The barrel EMC and the backward endocarp EMC will be read out by **25 data concentrators (DCs) whereas the forward endocarp EMC requires 14 DCs.** The assumption is that a DC has 20 optical links running at 16Gb/s. After a two-stage process including burst building, the data is send to a Compute Node (CN).

Y**utie Liang presented his work about STT tracking on the CN FPGA platform**. The algorithm is capable of treating overlapping events with and without externally provided t0. Momentum r**esolutions of 3.2 % for pt and 4.2 % for pz at 1 GeV/c are obtained.** The execution time is 7 **us for a single instance** of the algorithm implemented on a Virtex 4 FPGA.

Thomas Gessler gave an **update of the Compute Node hardware**. A new version consisting of anATCA carrier board with Kintex 7 Ultrascale FPGA is currently in the design phase. A first prototype is expected before the end of this year. The new carrier board will be compatible with the Virtex 5 based xFP cards currently used for PANDA and Belle II. In a second phase, the xFP cards will be upgraded to Kintex 7 Ultrascale. **The new boards will have 4 times more memory (16 GB per FPGA) 12 instead of 2 links, each running at twice the speed.The new CN version will have 10 times the FPGA resources, 10 times better performance and a performance/price ratio which is improved by a factor of 5.**

Simon Reiter presented an approach to **connect the CN to PCIe based server systems. Here, the C-RORC board developed by the ALICE collaboration is used.** 12 optical links are provided and the total throughput is 4GB/s. Currently, an upgraded version of C_RORC is developed in a joined effort by ALICE and LHCb. When available, this board will be investigated as a potential solution to connect the CN system to the server farm. An alternative option is provided with the new Kintex-7 ultrascale based compute nodes which feature a 10Gb Ethernet optical output at the ATCA rear transition module.

Finally, we heard a talk by **Mateusz Michalek, who has investigated the feasibility of using a COTS ethernet switch to implement the burst building network.** The idea is based in Juniper QFX series switches which provide a scalable solution. The system is flexible in that it provides 10Gbps, 40 GBPs and 100 Gbps interfaces. In the discussion, it became clear that this solution **might be technically feasible. However, the expected cost is of the order of several 100 K€. Thus, considering the limited resources for PANDA DAQ, to appears the the present solution using custom FPGA based boards is more economical.**

After the last talk, an extended discussion session took place, where the most imported issues in the context of the TDR were treated. The following decisions were taken.

A skeleton of the DAQ TDR with all the relevant chapter will be provided on the FAIR GIT server (Wolfgang Kühn).
We have to work towards a better definition both of the physics (Johan Meschendorp) and the **detector setup (Lars Schmitt) for phase 1,** which are needed as input to the TDR. It is clear that this process **will take some time but it has to be finalised before the TDR can be submitted. The goal is to prove that with the detector setup of Phase 1 the DAQ/Event filtering system is able to record a sufficient amount of integrated luminosity to provide interesting physics.**
Data formats and interfaces have to be defined. A working group, consisting of Greg Korcyl, Myroslav Kavatsyuk (chair) and Pawel Marciniewski) is charged with that task. The results will be made available in the PANDA wiki.
Information about the number of data concentrators / optical links for all sub-systems of PANDA needs to be collected/updated (Holger Flemming, Wolfgang Kühn)
The group of Kris Korcyl will continue to develop discrete event simulations for PANDA DAQ
Lars Schmitt will organise a meeting for future detector tests with PANDA DAQ components. These tests should be conducted roughly **in a year from now.**
There will be bi-weekly eZuce meetings discussing the progress of DAQT towards the TDR.