FF-LYNX (*): Fast and Flexible protocols and interfaces for data transmission and distribution of clock, trigger and control signals

(*) project funded by the INFN 5th Commission

G. Magazzù for the FF-LYNX Collaboration
INFN – Sezione di Pisa
Dipartimento di Ingegneria della Informazione (DII-EIT) - Università di Pisa

FF-LYNX: project genesis

- **Common requirements in future High Energy Physics (HEP) experiments on distribution of Timing, Trigger and Control (TTC) signals and Data Acquisition (DAQ):**
  - **trigger latency**
  - **data-rates**
  - **flexibility w. r. t. working conditions and system architectures**
  - **robustness against effects of transmission errors and component failures**
  - **radiation hardness**
  - **power dissipation**
  - **material budget**
  - **…**

FF-LYNX: project goals

- **Definition of a “standard” and “flexible” protocol for the integrated distribution of TTC signals and DAQ**
- **Development of functional simulators to validate the protocol and evaluate the overall system performance under different hypotheses on sensor geometry, detector architecture and working conditions**
- **Implementation of the protocol in custom low power and radiation tolerant digital interfaces designed and produced in a commercial CMOS technology (≤130nm)**
- **Test and characterization (including irradiation tests) of the interface prototypes and development of a library of IP-Cores available to designers of ICs for the future experiments**

FF-LYNX: specifications (1)

- **Integrated distribution of TTC signals and DAQ → transmission of TTC and DAQ data handled by the same protocol and the same hardware components:**
  - **no more Trigger encoded with missing clock pulses (LHC)**
  - **no more "slow control" protocols or "custom" fast control protocols**
- **Different data types:**
  - **Variable Latency (VL) → configuration/monitoring data or "raw" data (transmitted from Front-End ASICs after the reception of a Trigger)**
  - **Fixed Latency (FL) → "trigger" data, to be used in the generation of the L1 Trigger (e.g.: hit timing and position)**
- **Robustness of critical data (e.g.: Triggers, Frame Headers) w.r.t. transmission errors**

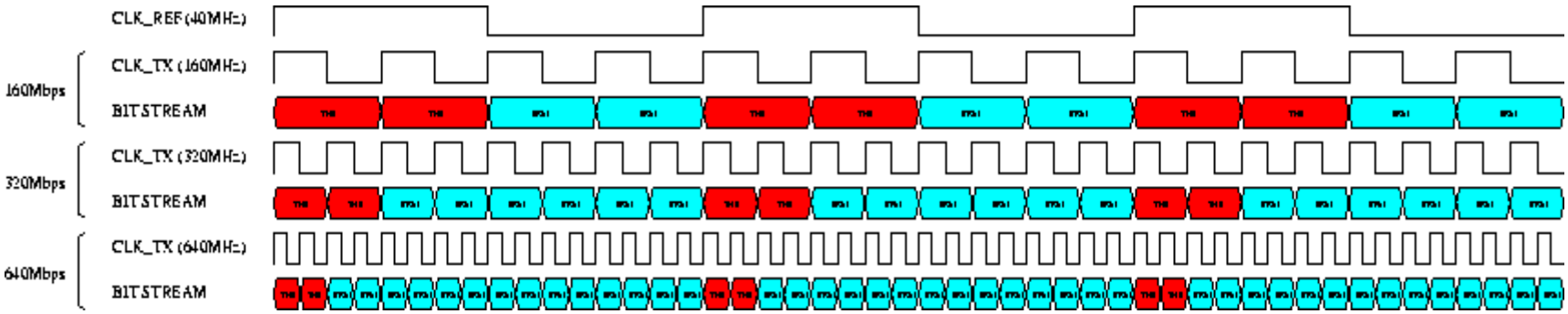
FF-LYNX: specifications (2)

- **Different values of the link speed supported: 4xF, 8xF and 16xF (F = frequency of the reference clock) in both the Down-Link (toward the detector) and Up-Link (from the detector):**

  F = 40MHz @ LHC→ 160,320 and 640 Mbps
- **Reference clock recovered in destination devices from the high speed clock used in the transmission of the serial stream (synchronization handled by the protocol)**
- **Easy coupling of FF-LYNX interfaces with "host" ASIC cores (serial and parallel data ports)**
- **Flexibility with respect to system architecture (e.g.: Star, Ring)**
- **Compatibility with different implementation of the physical links:**
  - **"double wire" (V.1) → Data/Strobe ("Space-Wire" like)**
  - **"single wire" (V.2) → xb/yb ("8b/10b" like)**

FF-LYNX: THS & FRM channels

- **Two separate channels merged in one data stream (Time Division Multiplexing)**
  - **THS channel → Triggers, frame Headers and Synchronization commands**
  - **FRM channel → Data organized in frames whose structure is independent w.r.t. data type and packet size**
- **6-bit error robust encoding for Triggers, Frame Headers and Synchronization commands → pattern detected and timing correctly reconstructed also with single bit flips**
- **Transmission of frames in the FRM channel flagged by frame header transmitted in the THS channel**



FF-LYNX: frame structure (1)

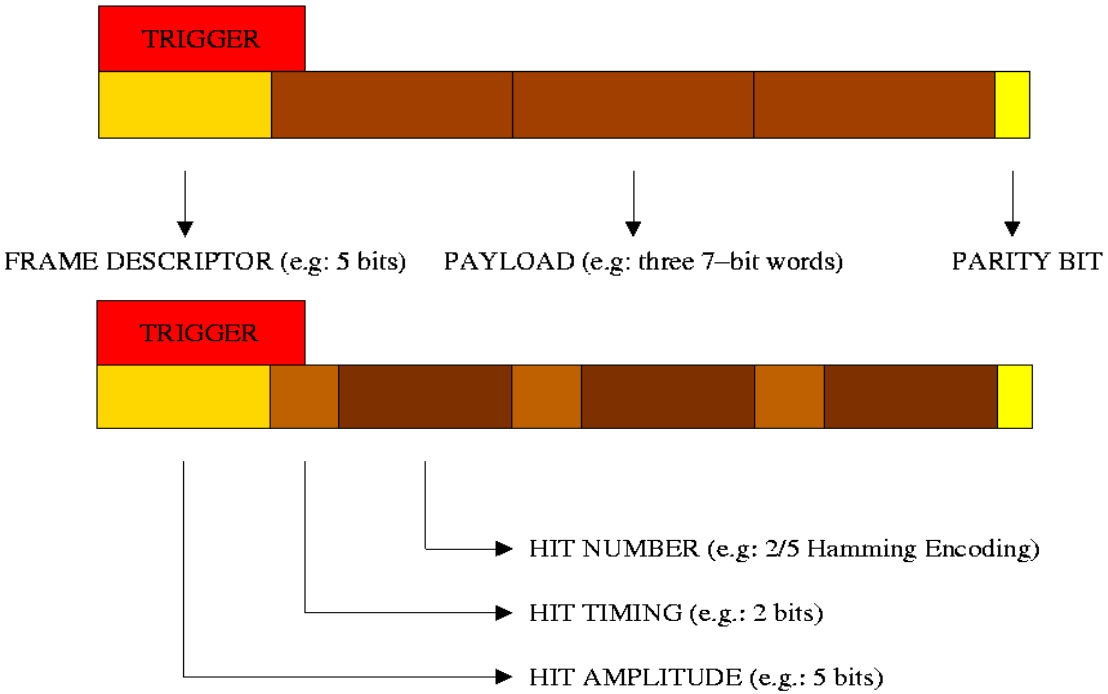
Variable Length (VL) frames

- **Frame Descriptor (8/12 Hamming Encoding)**
  - **Frame Length (4 bits) → number of words (16-bits) in the payload (including the optional label)**
  - **Data Type (1 bit) → data type (i.e.: configuration/monitoring data or "raw" data)**
  - **Label On (1 bit) → optional label included**
  - **Last Frame (1 bit): → last frame associated to a data packet**
- **Label (16-bits) → optional field containing information associated to the pay load (e.g.: address and operation code of commands in the Down-Link, time stamp or trigger number of "raw" data in the Up-Link**
- **Payload → data organized in 16-bit words (0 → 15)**
- **CRC (8-bits) → optional field for Cycle Redundancy Check**

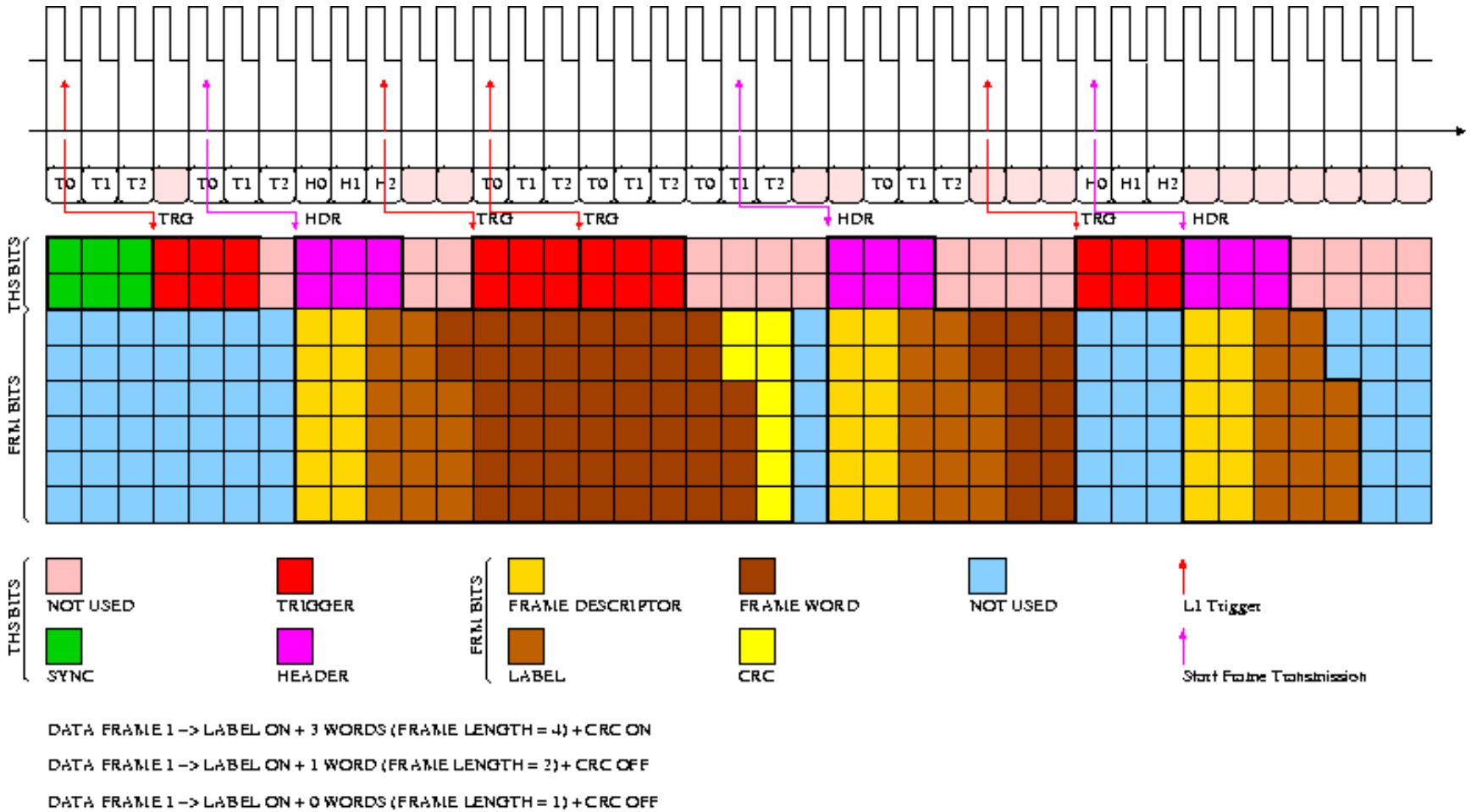
FF-LYNX: frame structure (2)

Fixed Length (FL) frames

- **Frame Descriptor (Hamming Encoding) ⟶ Frame Length (e.g.: number of n_b-bit words in the payload)**
- **Payload (n_wxn_b bits)⟶ data organized in n_w-bit words**
- **Parity bit ⟶ Payload Parity**

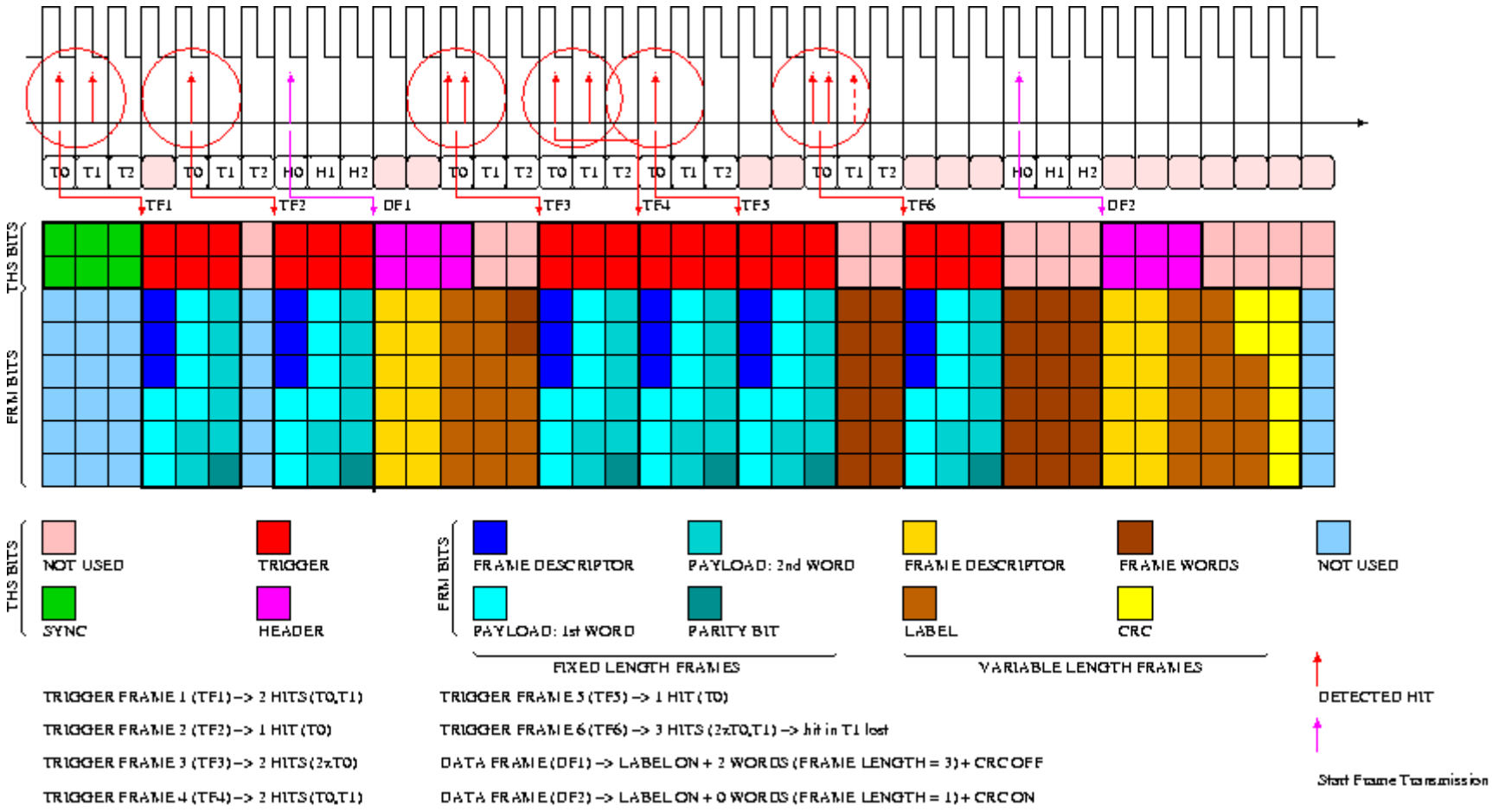


FF-LYNX: Down-Link



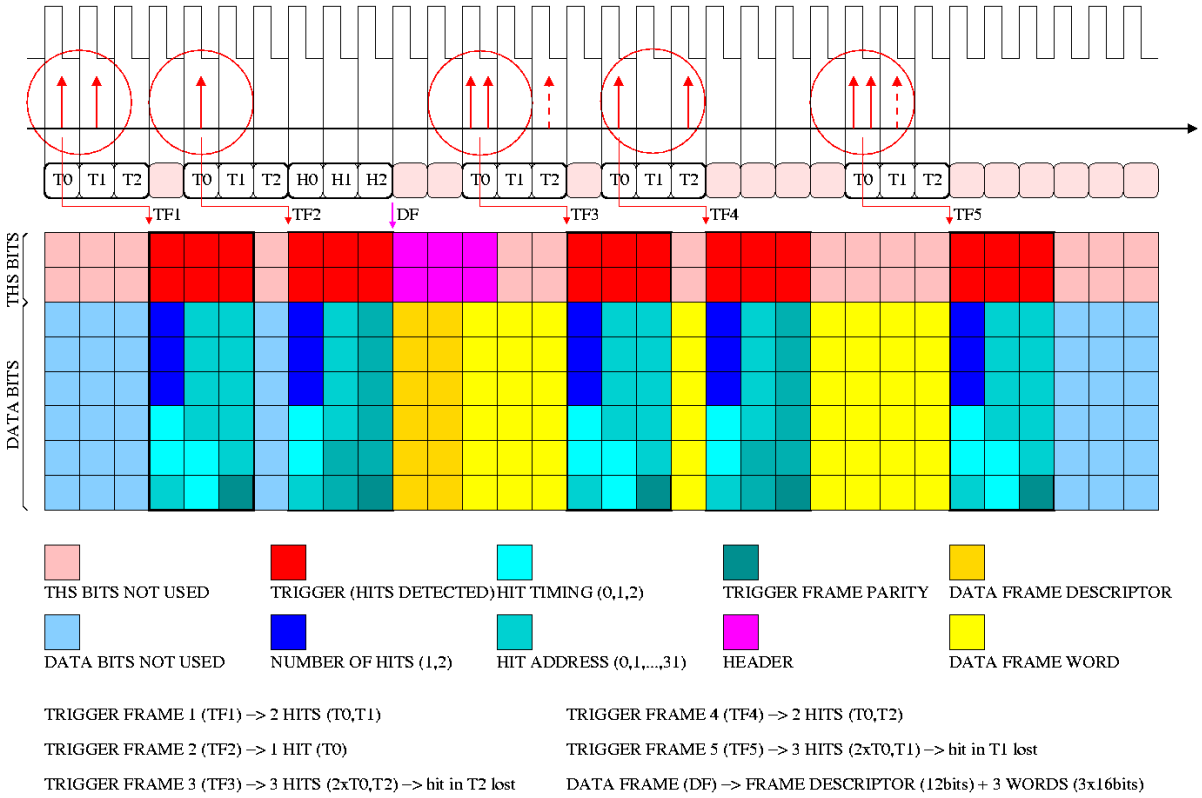
Possible data stream in the Down-Link (link speed = 8xF)

FF-LYNX: Up-Link



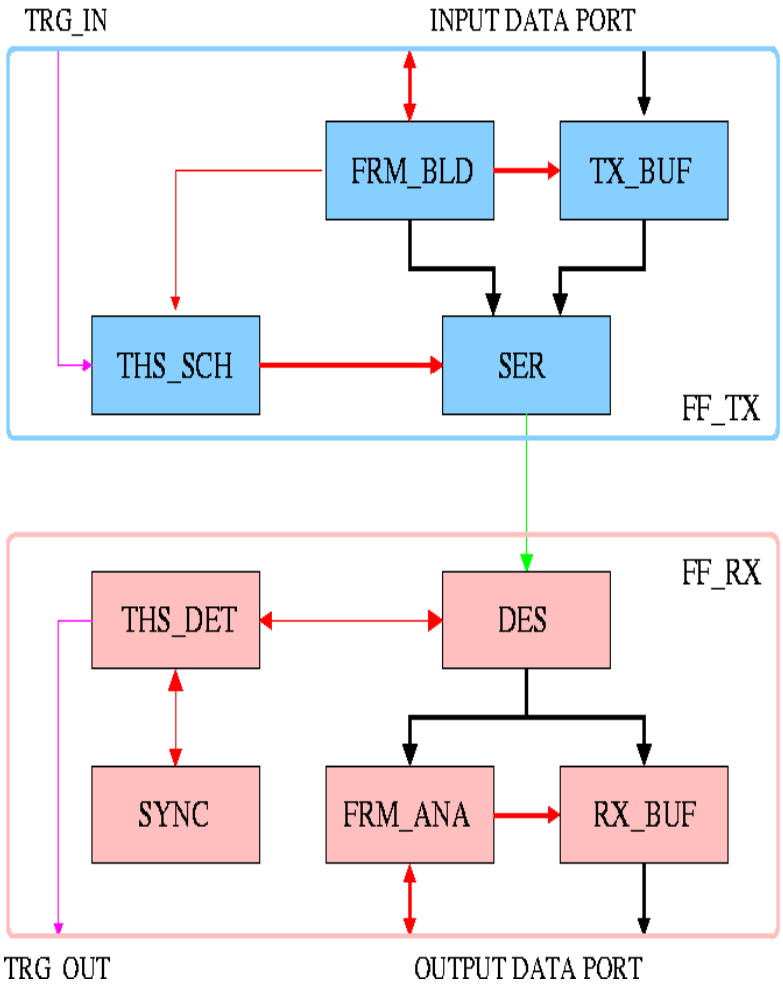
Possible data stream in the Up-Link (link speed = 8xF)

FF-LYNX: “trigger” data



“Trigger” data transmission in the Up-Link handled by protocol P320_C3_H2: link speed = 8xF, latency = 3 cycles of the reference clock (24 bits), up to 2 hits transmitted in each frame (2 bits for hit timing, 5 bits for hit position → 7bits/hit; 3 bits for the frame descriptor with 1/3 Hamming encoding)

FF-LYNX: interfaces



Architecture of the FF-TX and FF-RX interfaces

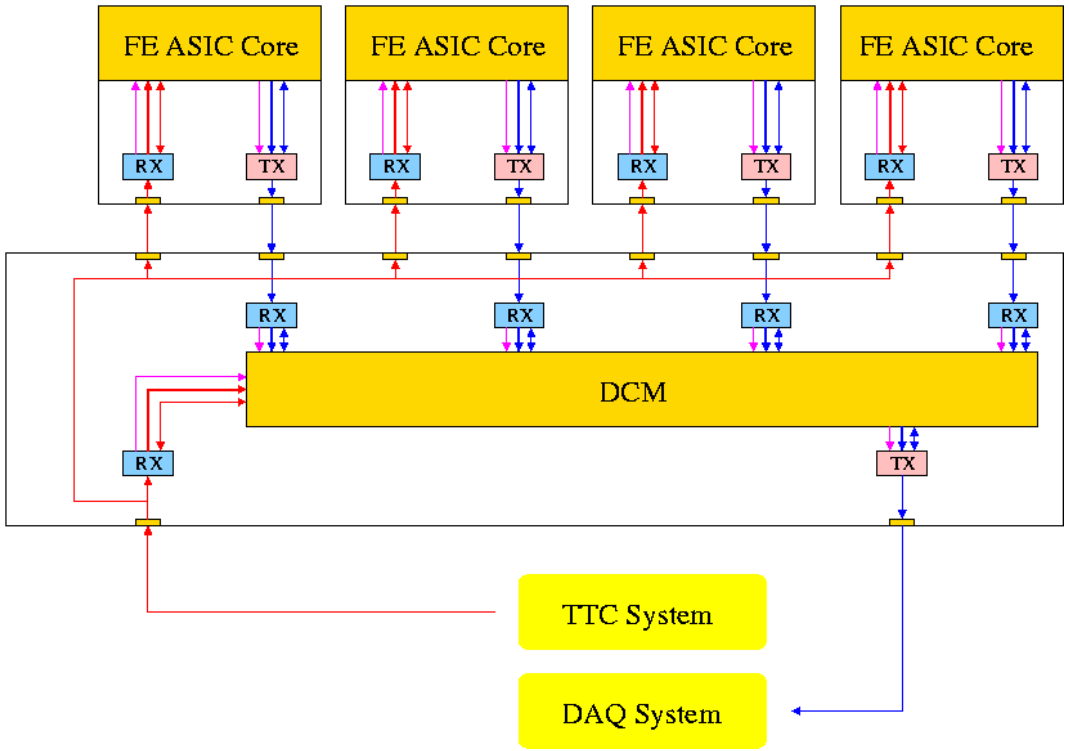
FF-TX

- **TX Buffer (TX_BUF) → Buffering of input data**
- **Frame Builder (FRM_BLD) → Assembly of data frames**
- **THS Scheduler (THS_SCH) → Arbitration between Triggers and Frame Headers**
- **Serializer (SER) → Generation of the output serial stream**

FF-RX

- **Deserializer (DES) → Extraction of THS and FRM data from the input serial stream**
- **THS Detector (THS_DET) → Detection of patterns associated to Triggers, Frame Headers and Sync commands in the THS channel**
- **Synchronizer (SYNC) → Recovery and synchronization of the reference clock and detection of THS and FRM channels in the input stream**
- **Frame Analyzer (FRM_ANA) → Analysis of the frame descriptor and control of the data transfer to the output buffer**
- **RX buffer (TX_BUF) → Buffering of output data**

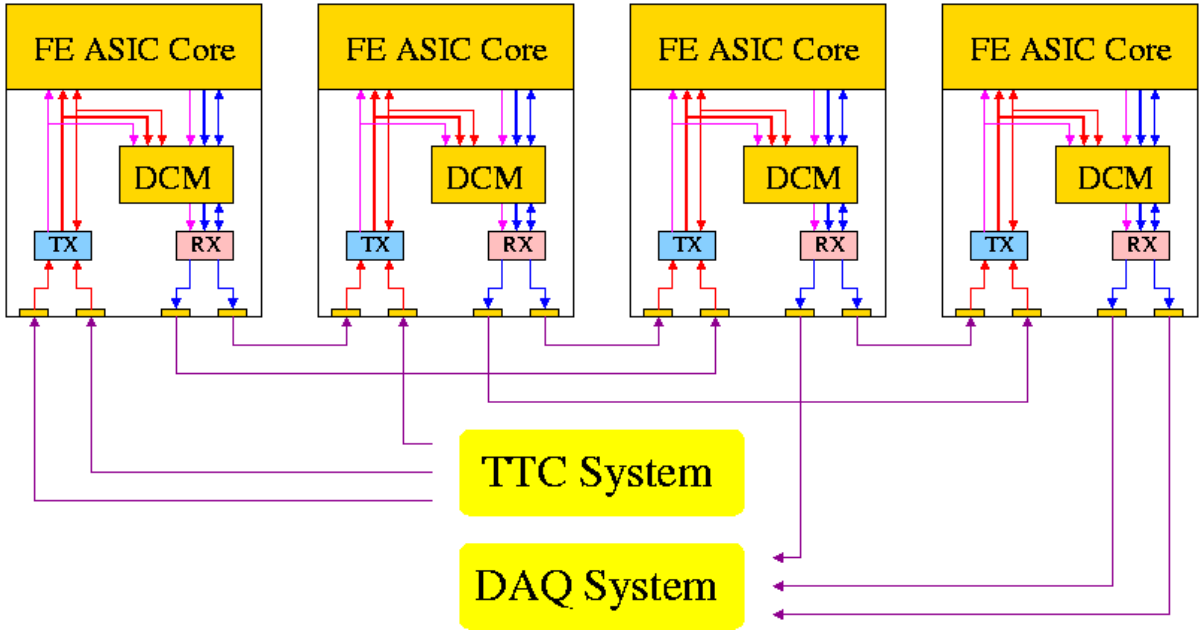
FF-LYNX: architectures (1)



"Star" architecture:

- **Front-End ASICs are directly connected to Electrical to Optical Converters (EOCs) or through Data Concentrator (DC) ASICs**
- **DC ASICs merge data streams and eventually perform event building and distribute TTC signals to groups of Front-End ASICs**
- **Clock, Trigger and Commands are distributed in parallel to Front-End ASICs through Down-Links, "raw" and "trigger" data are acquired in parallel through Up-Links**

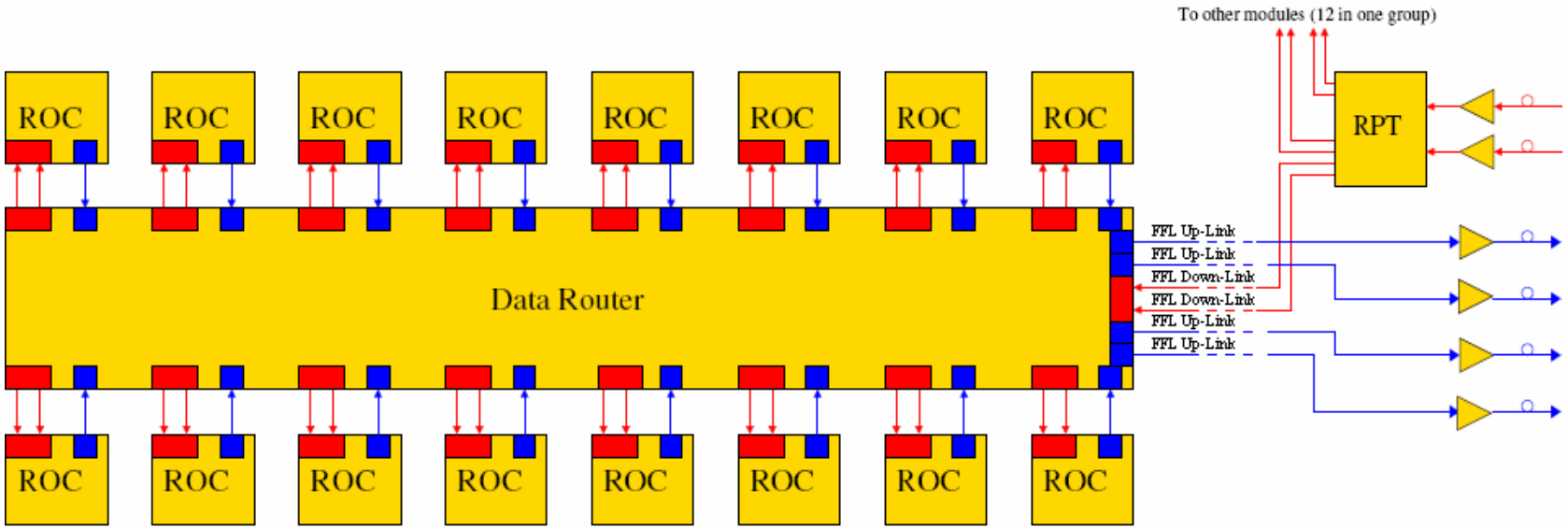
FF-LYNX: architectures (2)



"Ring" architecture:

- **Front-End ASIC are daisy chained with redundant connections to provide robustness against component failures**
- **Trigger and Commands propagate along the chain (highest priority to Triggers) and Data Concentration (Event Building) is distributed along the chain**
- **No distinction between Down-Links and Up-Links**

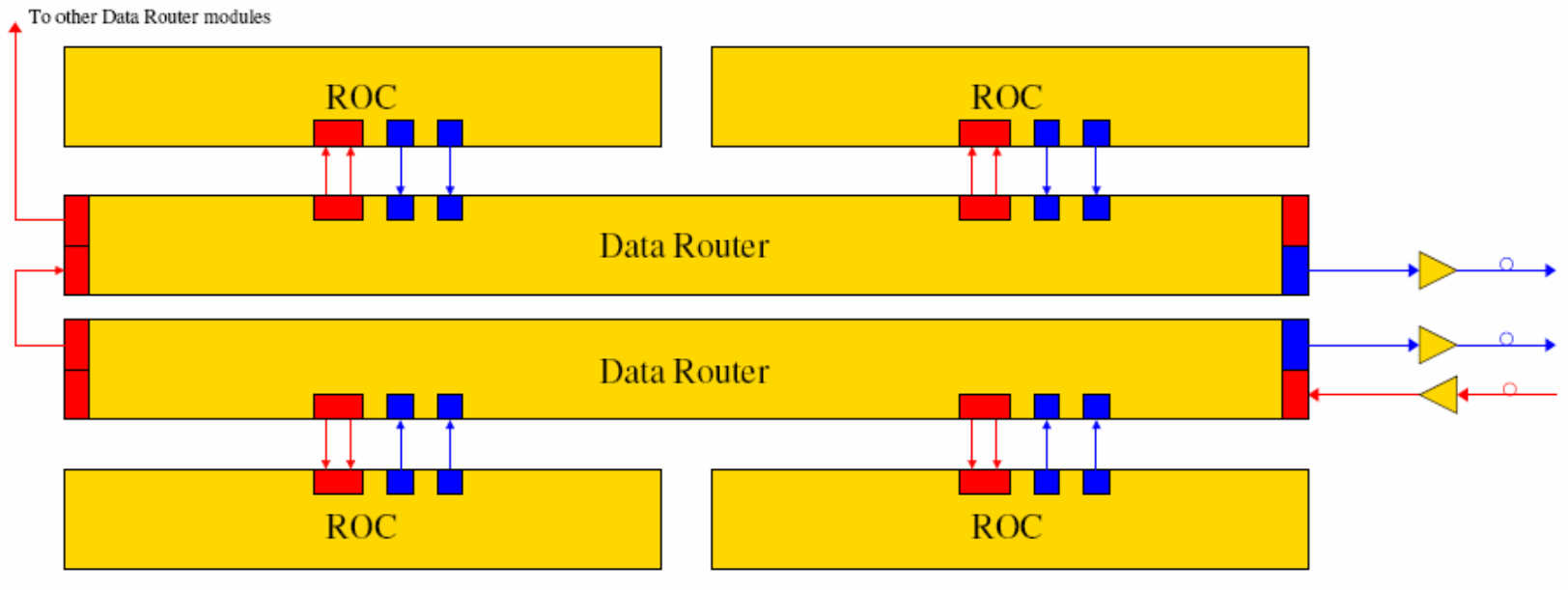
FF-LYNX: case studies (1)



Phase I upgrade of the CMS pixel detector: FF-LYNX based TTC distribution and DAQ with trigger based individual ROC readout → 4 ×160 Mbps optical fibers available for DAQ and reduced latency of data readout data (w.r.t. token based readout)

<u>Expected data rates for Phase I (inner layer)</u>: 40 Mbps from each ROC, 6÷16 hit ROCs/module → 240 ÷ 640 Mbps from each module (16 ROCs).

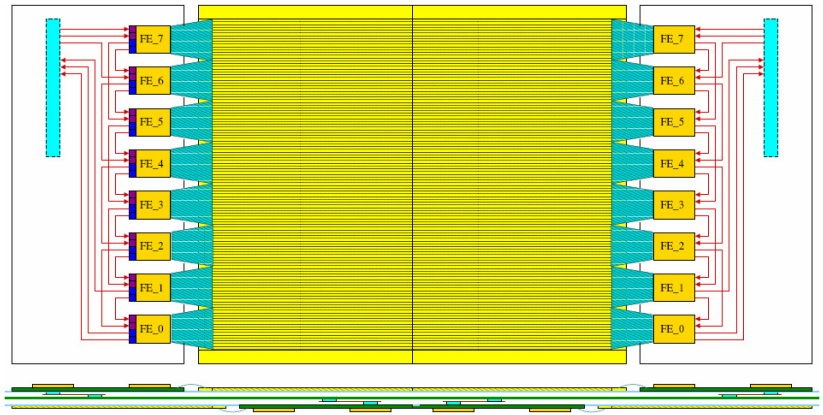
FF-LYNX: case studies (2)

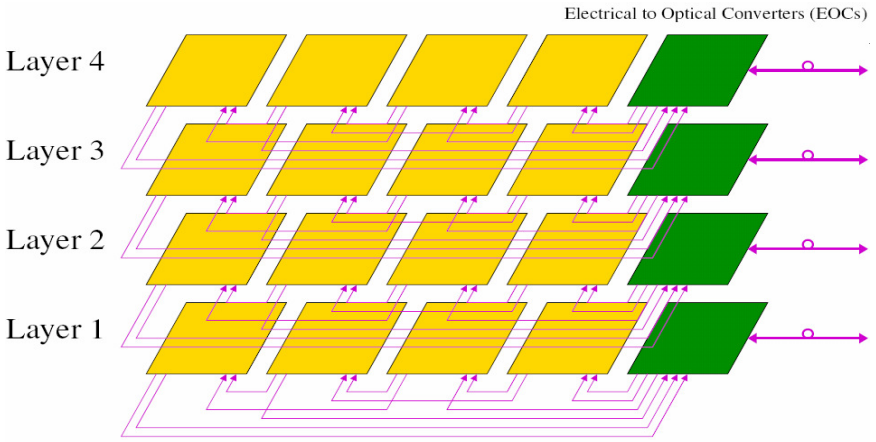


Phase II upgrade of the CMS pixel detector: two 640 Mbps electrical links from each ROC; two uplink optical fiber (≥ 1.6 Gbps) for each 4-ROC module and one downlink optical fiber optionally shared among several modules.

<u>Expected data rates for Phase II (inner layer)</u>: 800 Mbps from each ROC, up to 3.2 Gbps from each module (4 ROCs).

FF-LYNX: case studies (3)

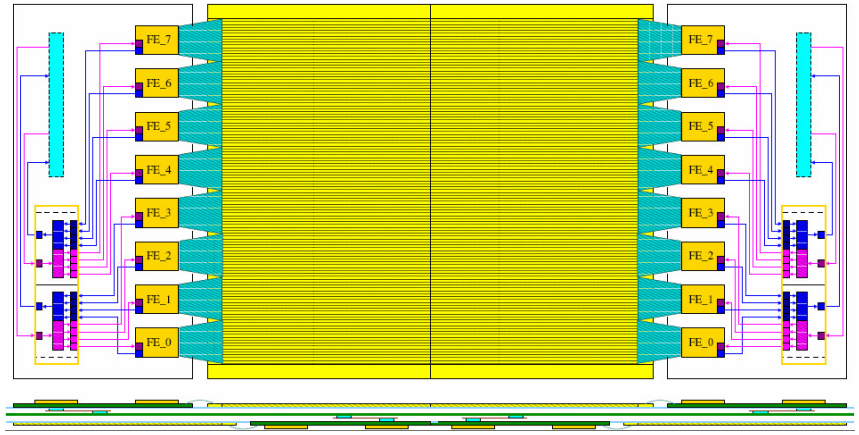


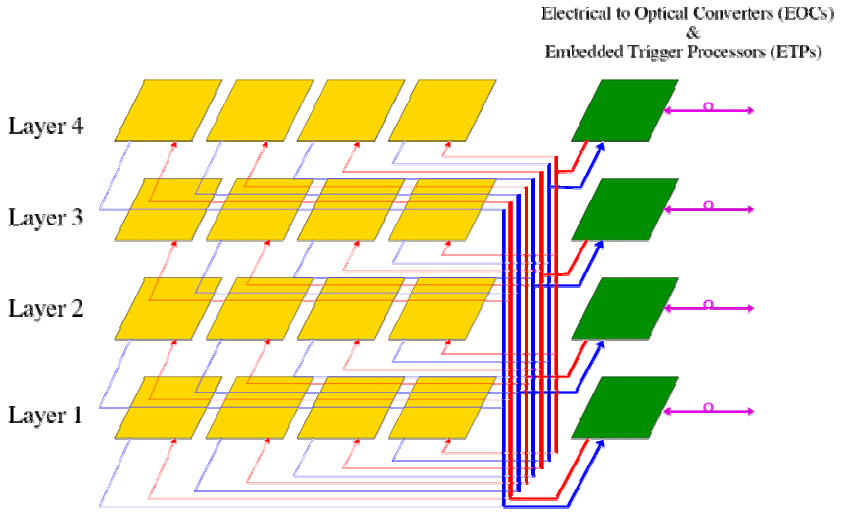


Phase II upgrade of the CMS Strip Tracker (no trigger data readout): daisy chains of Front-End ASICs within the modules and, optionally, daisy chain of modules.

<u>Expected data rate for raw data, at r = 78 cm</u>: 5 Mbps/FE chip → 40 Mbps/module.

FF-LYNX: case studies (4)





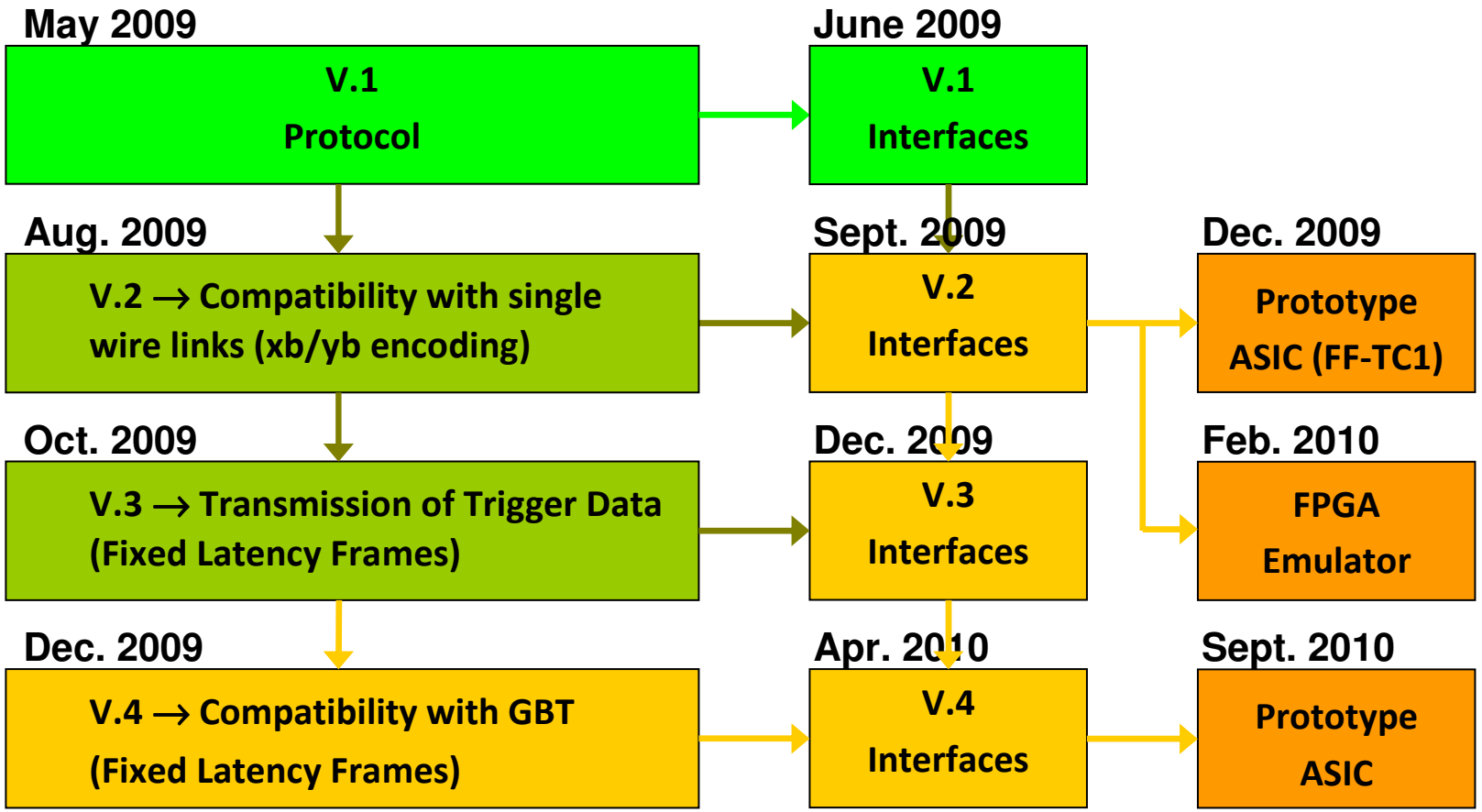
Phase II upgrade of the CMS Strip Tracker (trigger data readout and embedded trigger processors): data concentrators in the modules and high speed links between modules and trigger processors.

<u>Expected data rate for trigger data, at r = 78 cm</u>: 120 Mbps/FE chip → 960 Mbps/module.

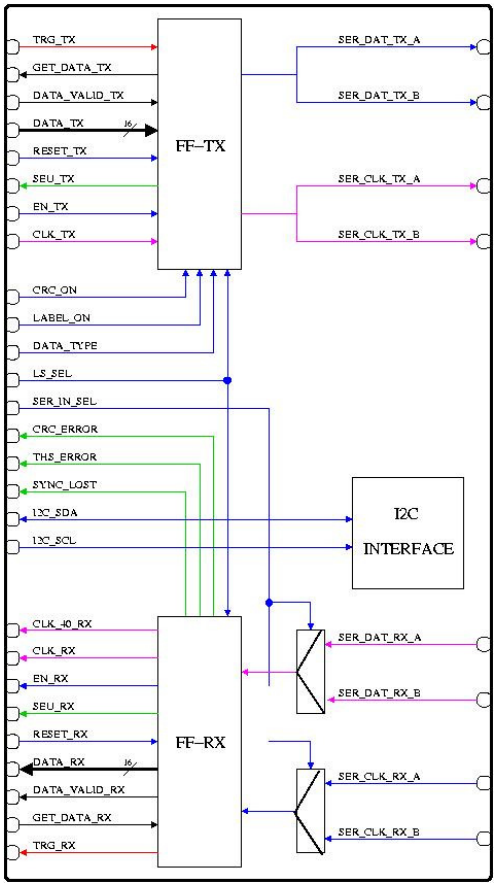
FF-LYNX: current status

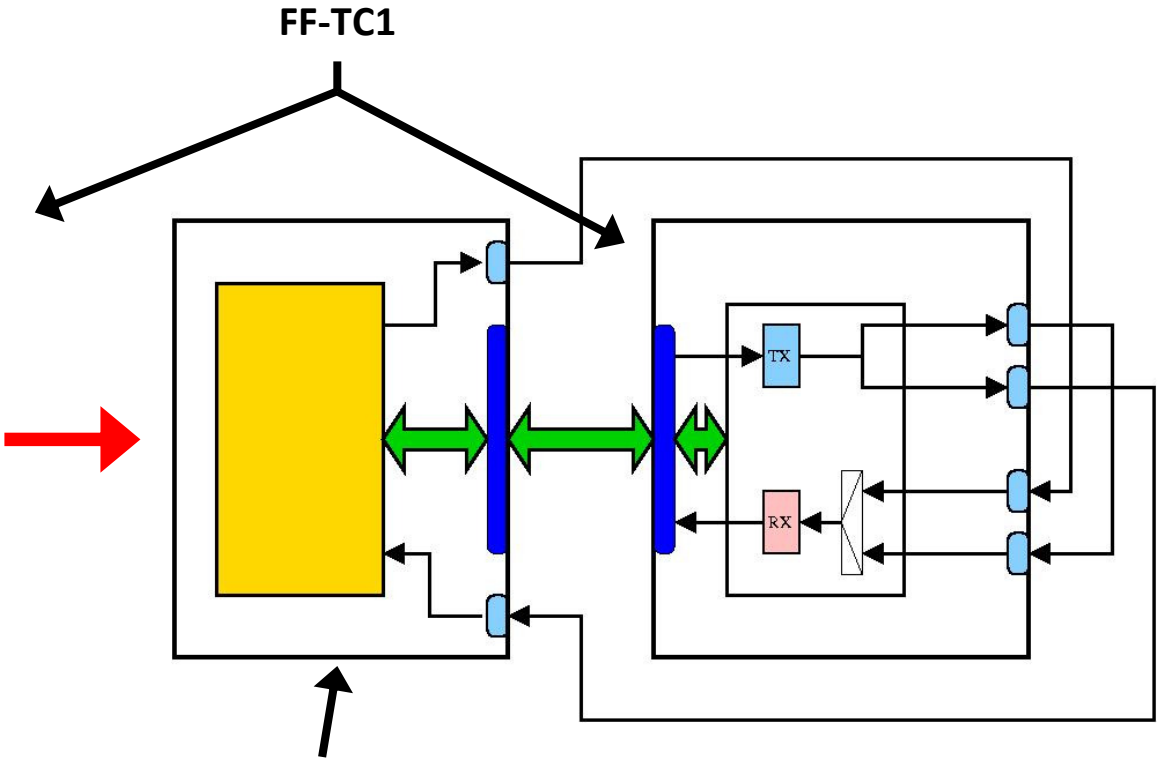
- **Analysis of system requirements and existing custom and standard protocols used in the HEP experiments and in consumer electronics performed**
- **Test bench for functional simulations (based on the current control and readout system of the CMS pixel detector) developed and used to validate and compare different possible protocol implementations w.r.t. pre-defined figures of merit (i.e.: trigger detection efficiency, data losses)**
- **Protocol (V.1) defined (May 2009) → "double-wire" links , VL frames**
- **High level models of the interfaces (FF-TX and FF-RX) developed and validated (June 2009)**
- **Analysis of different solutions to increase robustness against SEEs (triple redundancy, "SEU robust" encoding of FSM states, use of "ghost" registers) ongoing**
- **Tentative architecture of the test IC FF-TC1 defined**
- **Technology (e.g.: I/O libraries and PLL & clock recovery devices) survey ongoing**

FF-LYNX: project roadmap



FF-LYNX: test IC FF-TC1





FPGA based Test Setup & FF-LYNX Emulator

Preliminary specifications (pin-out and architecture) of the test IC FF-TC1 defined to be reviewed by referees in July

FF-LYNX: …

The work is ongoing and …

- … we appreciate comments and suggestions from potential FF-LYNX users (e.g.: we already interact with colleagues working for the CMS and ATLAS pixel and strip Tracker detectors),
- we are an open collaboration (e.g.: UCSB recently joined the project in the framework of an R&D activity for the CMS upgrades) …

Guido.Magazzu@pi.infn.it
Luca.Fanucci@iet.unipi.it