Decision Process

(Proposal and Discussion)

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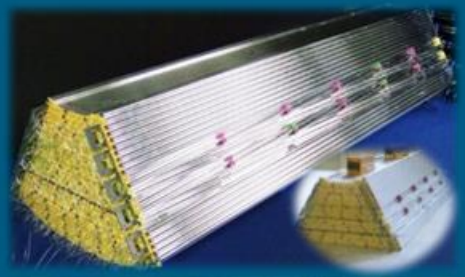
STT RO WShop | Krakow | Jan-30/31 2017



Set Up Decision Process

- Organisation
- Timelines
- Criteria & Deliverables

- Agreement

Readout Decision

- Readout system readiness (“pre-series”) general basis for the decision
- Approval of system readiness: fulfillment of certain criteria & deliverables
- Official milestone FAIR-M8 for readout system

- Enter final production stage after decision
- Full Integration of the readout system into PANDA

  (mech., DAQ, simulation & analysis)

General Manpower Situation

- Manpower situation critical in general
- Data analysis (very) critical: find at least one person for each system
- Propose final analysis with the same SW program or at least same raw data filtering, same pattern recognition and tracking algorithms
  - algorithms, cuts, filtering, calibrations, ..
  - raw data for the straw layouts in the test systems are similar, same calibration methods
  - define common input format and structure (ROOT, event data structure

Organisation of the Process (Proposal!)

- Set up a Decision Panel
  - One person from each involved group, + PANDA TC, + STT Mgr
  - Aim to add 2 external experts from ECE evaluation panel

- 3 groups in ASIC/TRB project: AGH, JU, IKP1
- 3 groups in ADC project: IFJ, ZEA2, IKP1

- Regular status report meetings (TRK / eZuce)

- PANDA integration aspects (Mech./DAQ) by TC & STT Mgr
- Reporting in PANDA Tech.Board session(s)

PANDA TC
STT Mgr
AGH Kra
JU Kra
IFJ Kra
INFN Fra
KVI Gro
IKP1 Jül
ZEA2 Jül
IFIN Buch
PANDA DCS

Manpower & Resources

- Workpackage (WP) organisation needed
- Contact person(s) for each WP
- MP calculation needed (FTEs / year)

- Costbook for pre-series system required (complete)
  - All components, manufacturing, design works, testing
  - Collection of all production steps and manufacturers

- Costbook for ASIC/TRB pre-series system already collected

WP.org example

FE/Analog
Digitzer
DAQ
Online/FPGA
Offline Analysis
Install&Tests
..

Timelines for Decision Process

- Mar-17: system status reports for beam request (in May-17 for Q1/Q2-2018)
- Jun-17: status of system design & production
- Sep-17: status of readout system installation
- Nov-17: status of cosmic run tests and preps for beam time in Q1-2018
- Q1-2018: in-beam tests, proton & deuteron, momentum 0.6– 3.0 GeV/c
- Q2-2018: reporting on final results
- Q2-2018: decision on final readout system

- Side-remark: ASIC/TRB readout system is installed & running (since 2016), reports in 2017 then on open points and on 2016' beam test data-analysis and cosmic run tests in 2017

C&D: Test Systems

- Straw & readout systems:
  - ~ 400 straw channels, close-packed layers, ≥16 straws per layer
  - ≥ 20 hits per track (inclined setup)
  - readout: full chain and all components for 400 channel
  - cabling ~ 8-12m, from detector front-end to readout crate
  - front-end and back-end layouts close to final (space, cooling, cable routing, ..)
- Two setups for the readout systems

- Reliability tests of all components
  - boards, cables, HV-capacitors, ..
  - noise level & EMI, RF-pickup, cross-talk, long-term stability
  - temperature effects
  - shielding, grounding requirements, ..

C&D: DAQ System

- DAQ system:
  - stable running, no hang-ups, long (~1h) data runs with lower trigger rate
  - 2+ weeks beam time, 4+ weeks cosmic runs
  - max. channel rate up to ~ 1 MHz / straw
  - avg. channel rate ~ 50 kHz / cm / straw
  - DAQ trigger rate ~ 100 kHz (~ PANDA starting phase)
    - ~ 12 MB/s (if 5 bytes data word $\times$ 24 hits)

- DAQ modes:
  - trigger mode
  - compatibility test of continuous readout
- Raw data storage in ROOT format

C&D: STT System & PANDA-DAQ Integr.

- PANDA-DAQ, not available for our tests
  - compute nodes and FPGA processing
  - continuous readout of all hits from various detectors into buffer
  - FPGA processing, event reconstruction, e.g. MVD+STT+GEM+SciTil hits
  - event data association and event identification
  - software trigger to start event data storage from buffer to disk (cloud?)

- STT readout integration scheme into PANDA-DAQ has to be worked out
- Presented in a Techboard and/or DAQ workshop

- Consider PANDA luminosity, data rate and bandwidth
- STT readout system at ~ 600 kHz average straw rate, 4224 straws
- FPGA processing time, e.g. pulse shape analysis
- System architecture, e.g. number, stages of FPGA processors

C&D: Testruns

- Beam tests: full signal dynamical range, dE/dx-separation
  - protons & deuteron (COSY) beam in momentum range 0.6-3.0 GeV/c
  - deuteron/proton separation
  - pulse signal dynamical range, dE/dx ~ 5-50 keV/cm coverage
  - ~ 1 MHz/straw max. hit rates
  - < 100 kHz/cm avg. hit rates, to avoid (heavy) space charge effects
  - DAQ robustness test by high data throughput
  - particle bursts can happen (robustness test for DAQ)

- Cosmic runs: clean tracks, efficiency limit
  - spatial resolution and efficiency analysis (limits for mips)
  - test readout stability by long-term data runs (4+ weeks)

C&D: Analysis

- Online
  - Raw data spectra (noise level, BL, pickup, ..)
  - FPGA pulse shape analysis (algorithms, speed, efficiency)

- Spatial resolution & efficiency: beam tracks and cosmic tracks
  - reconstructed tracks, χ2-fit and residuals (=track-isochrone distance)
  - radial hit efficiency
  - ≥16 hits/track and inclined setup to reduce bias (variety of track angles)
  - goal: ~150µm (isochrone), on average, resolution curve (radial)

- PID capability: beam tracks
  - charge measurement by pulse integration / time-over-threshold
  - dE/dx separation for protons & deuterons in COSY momentum range
  - proton/deuteron separation power

Agreement