ADC based DAQ Status

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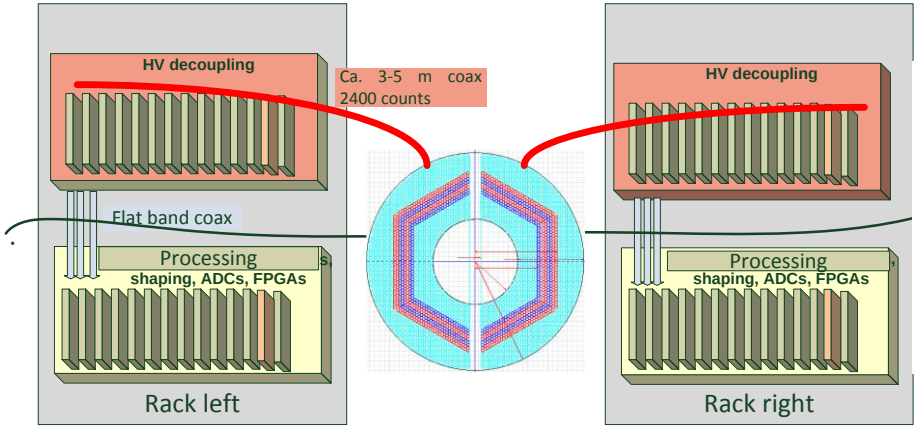
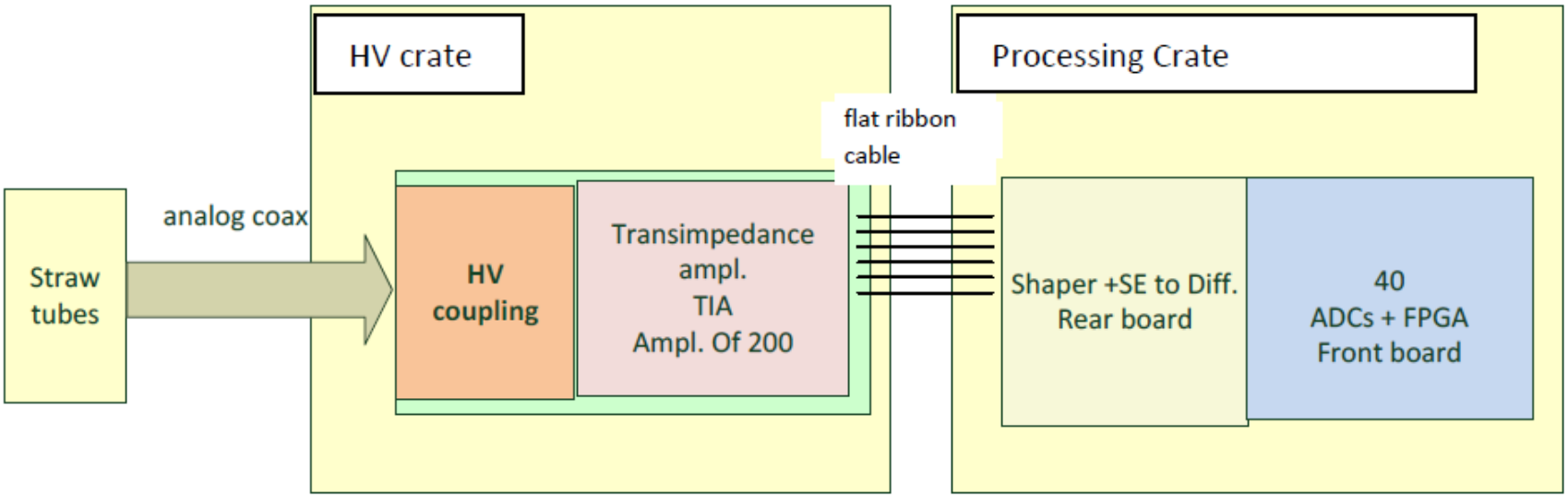
Mitglied der Helmholtz-Gemeinschaft

System overview





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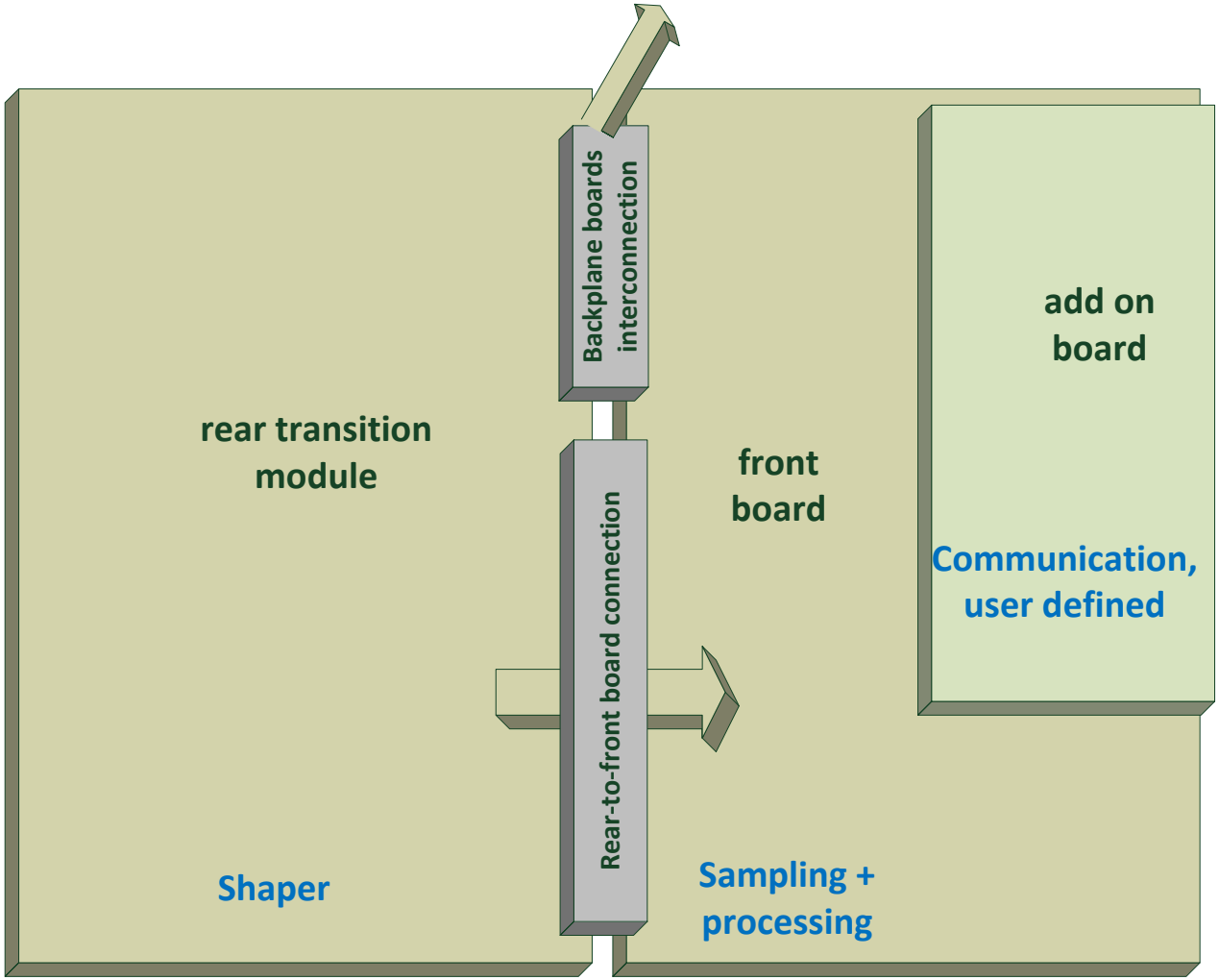
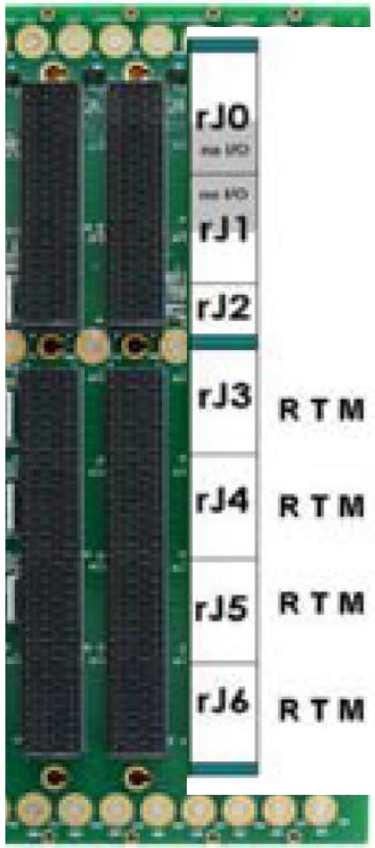
16-Slot open VPX crate





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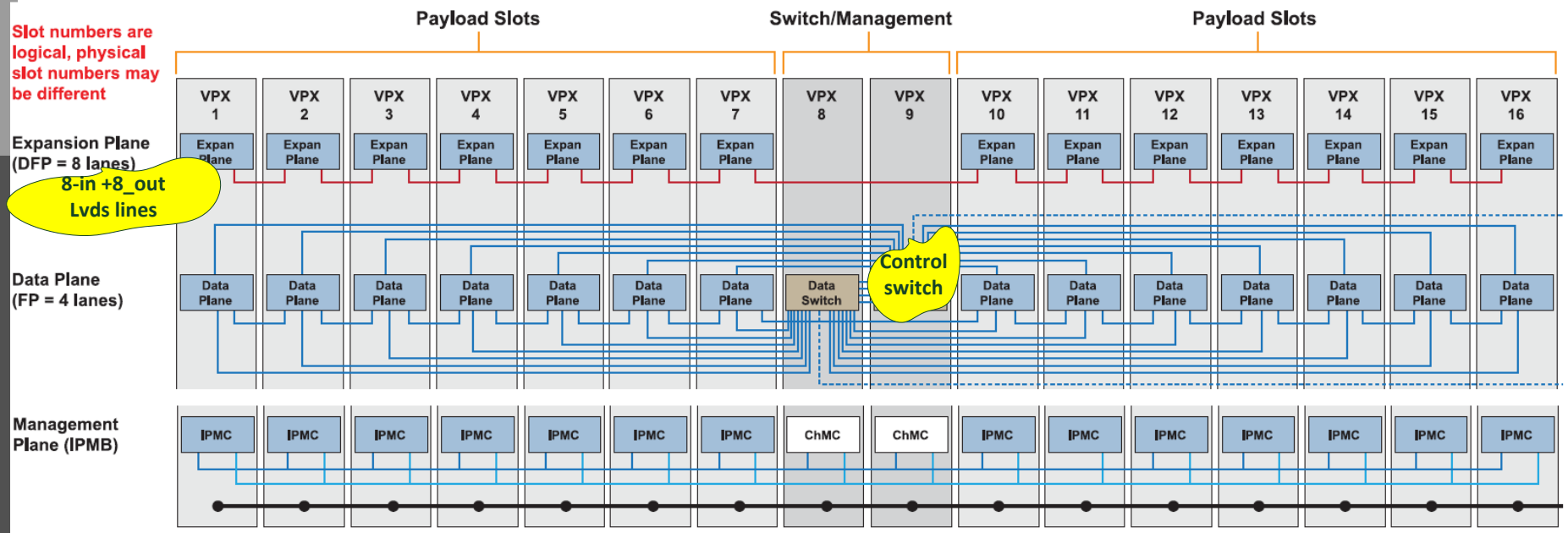
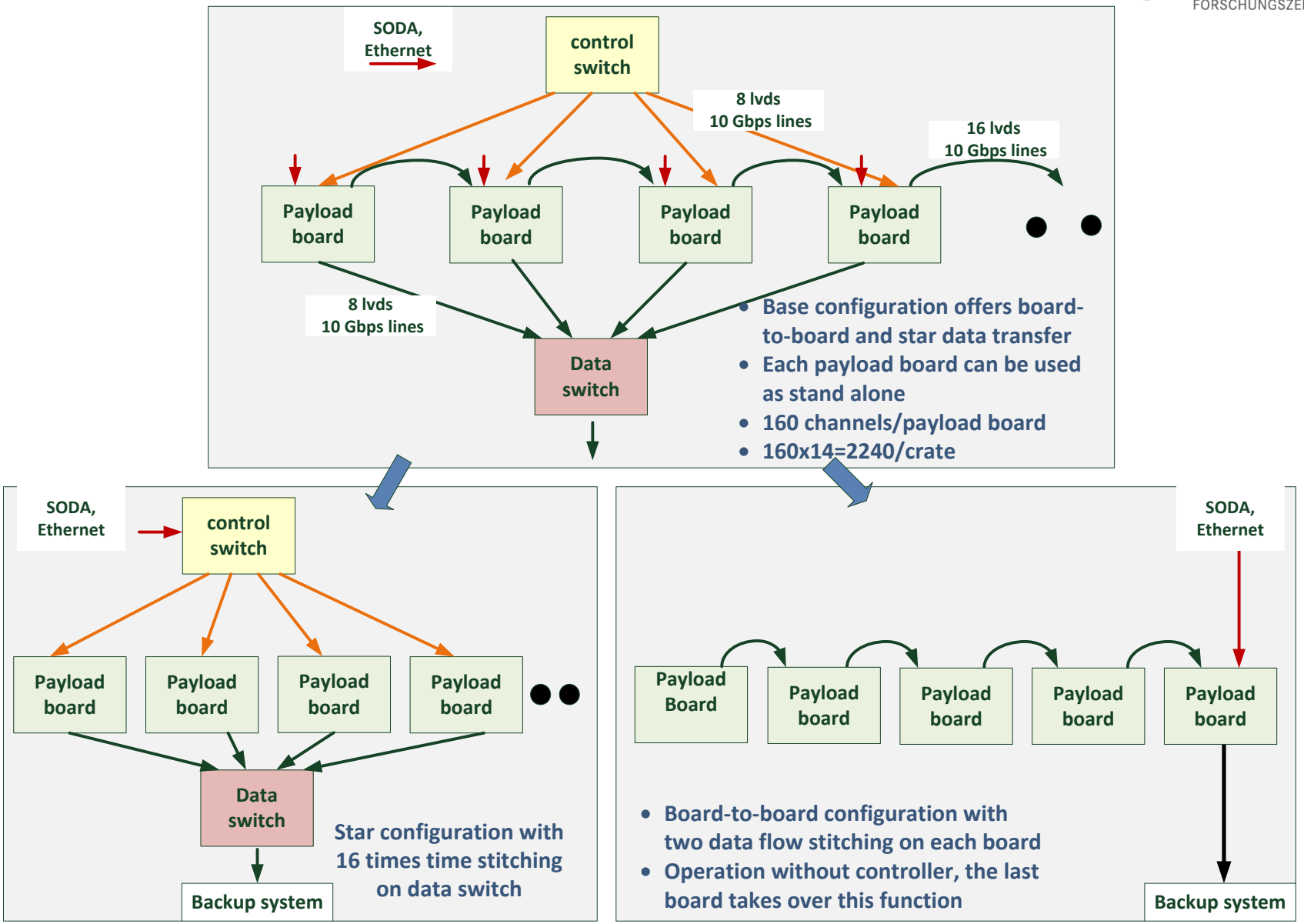
Chassis Topology



16-Slot 6U Multi Plane Development Chassis Topology Wiring Diagram.

System configurations



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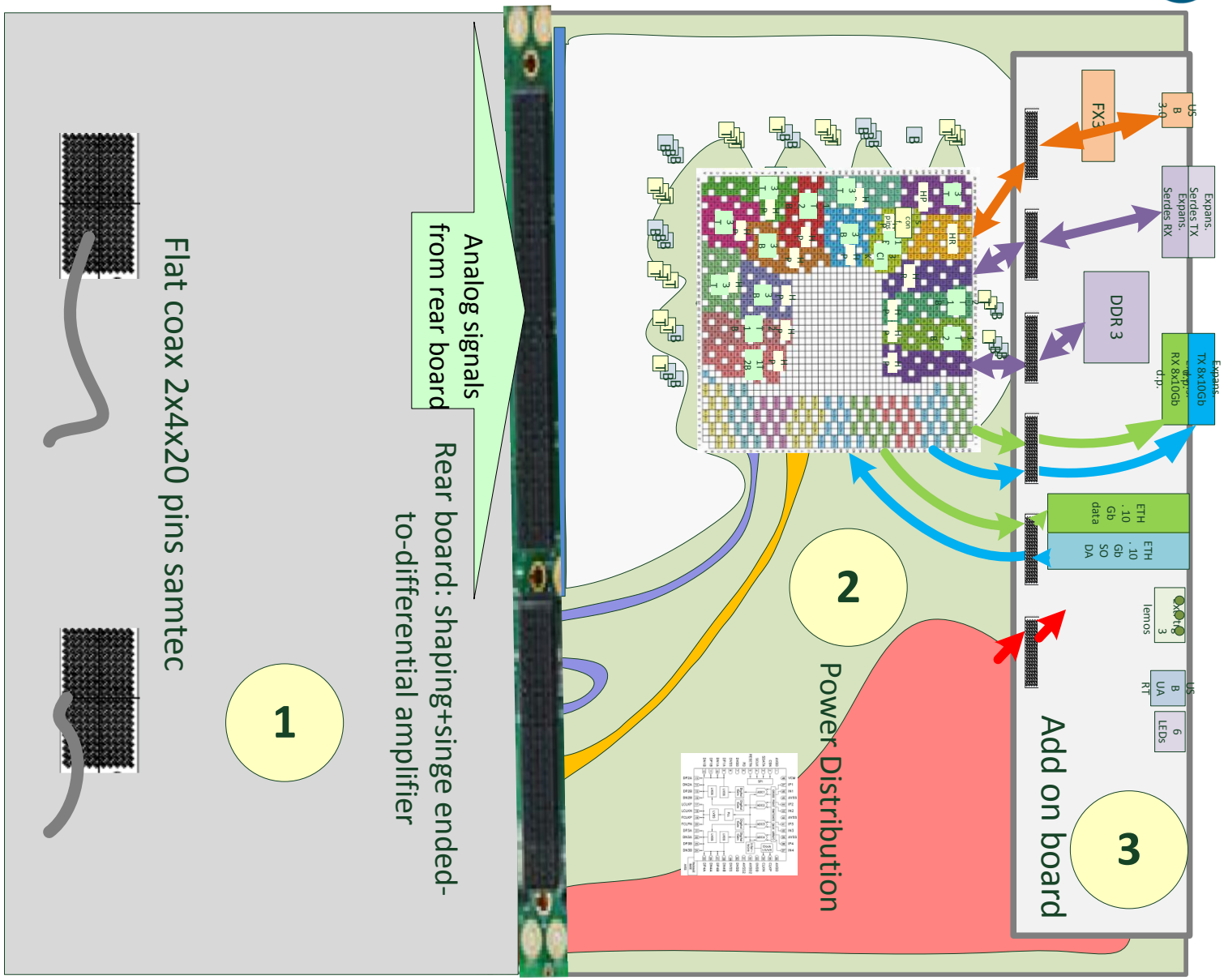
Boards Overview



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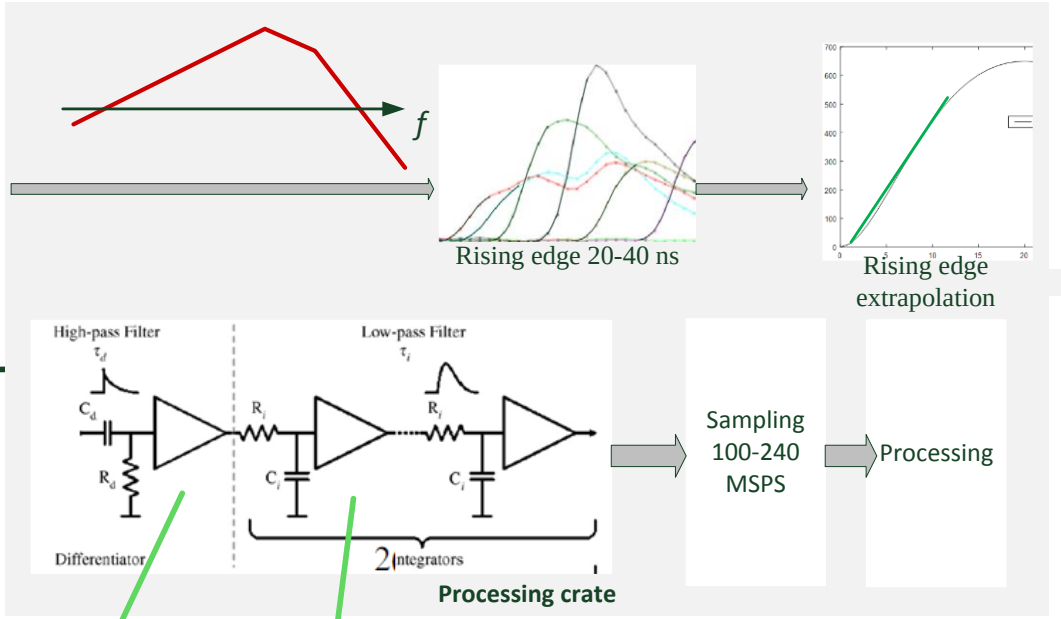
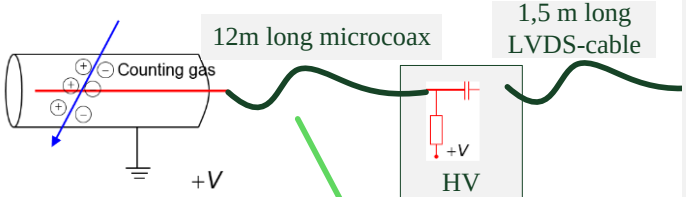
Signal chain





$$H(s)_{\text{total}} = \left(\frac{A_{\text{pr}}}{1+s\tau_{\text{pr}}}\right)\left(\frac{s\tau_{\text{d}}}{1+s\tau_{\text{d}}}\right)\left(\frac{A_{\text{sh}}}{1+s\tau_{\text{i}}}\right)^2$$

MK 5001 microcoax cable: Distributed constants, acts as **10 ns integrator**. (6 Db at 20 MHz, 96 pF/m, 1Om/m)

10-50 ns

2x5 ns

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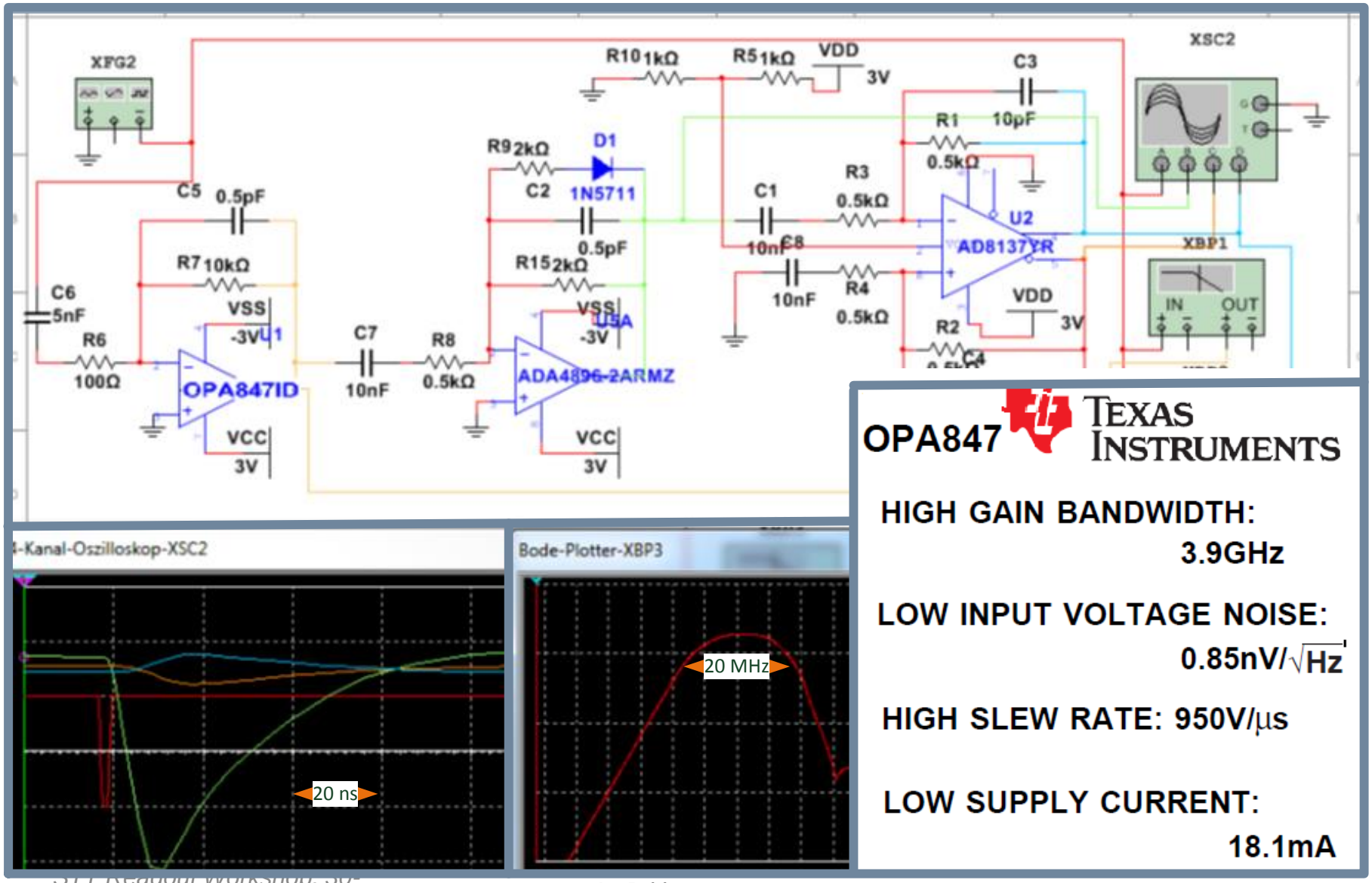
Amplifier/Shaper



OPA847 TEXAS INSTRUMENTS

HIGH GAIN BANDWIDTH:
3.9GHz

LOW INPUT VOLTAGE NOISE:
0.85nV/$\sqrt{Hz}$

HIGH SLEW RATE: 950V/µs

LOW SUPPLY CURRENT:
18.1mA

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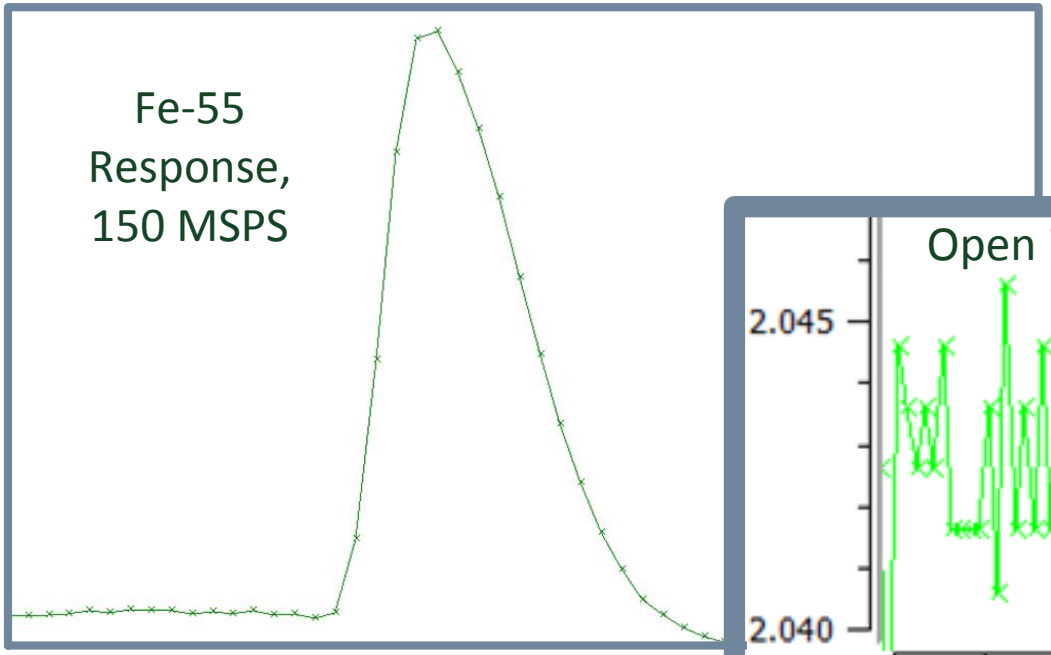
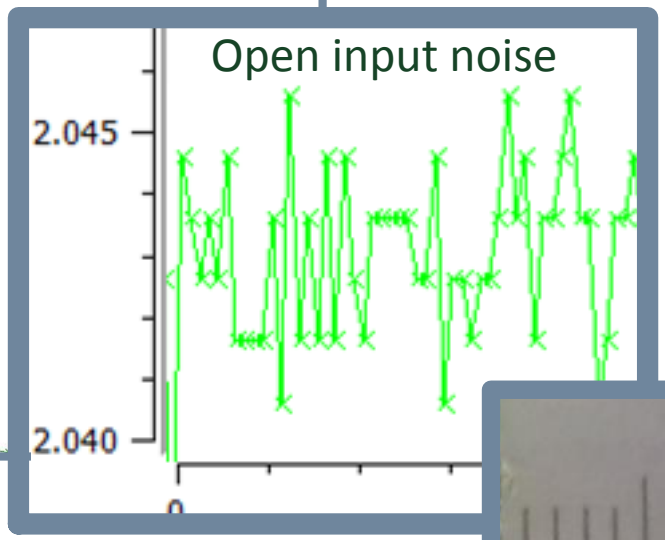
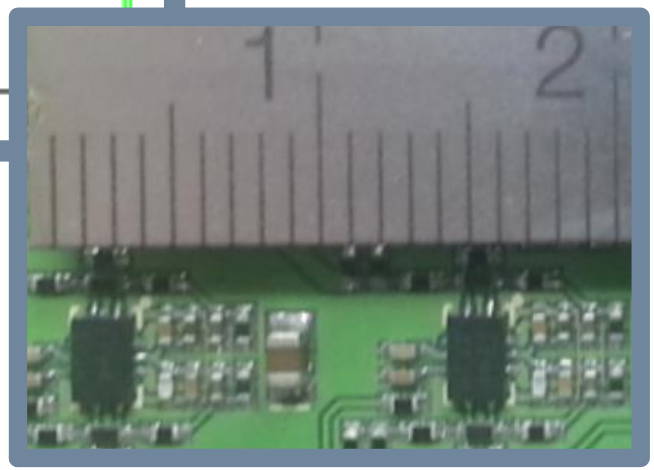
Amplifier: performance, footprint

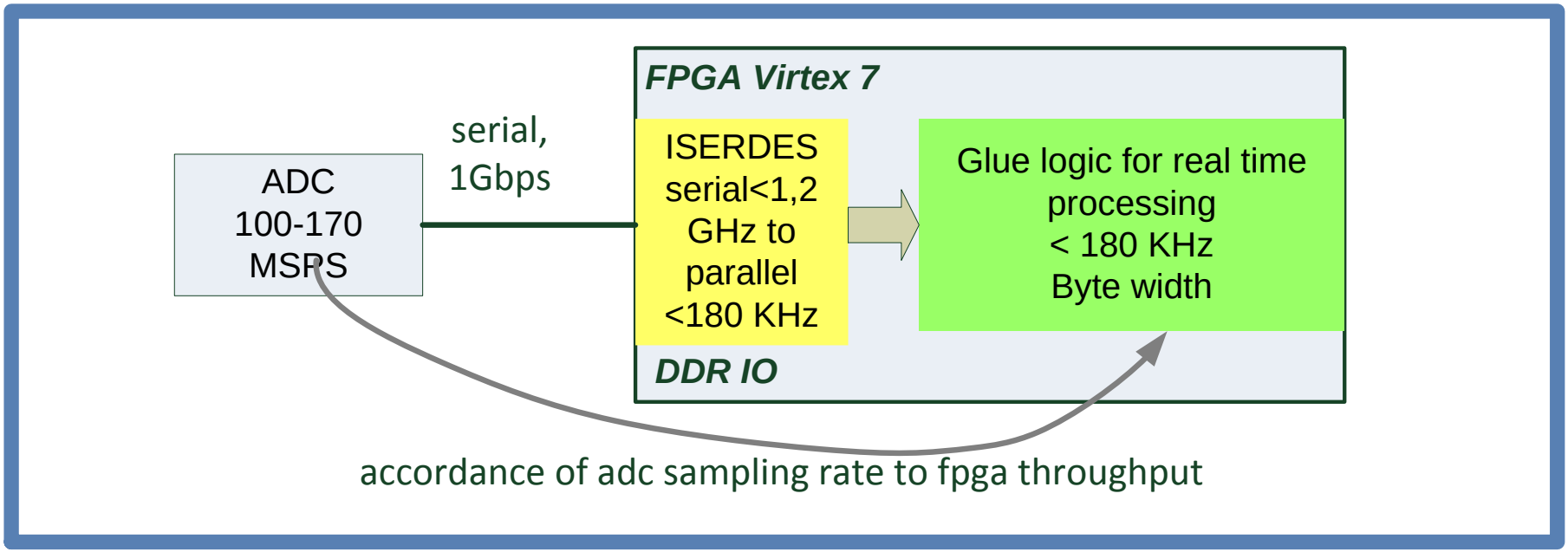






- peaking time of 20 ns,
- amplification of 400,
- 20 MHz BW;
- SNR of 53 dB without cable
- SNR of 35 dB with 12 m cable connected to Straw tube
- <70 mW/channel

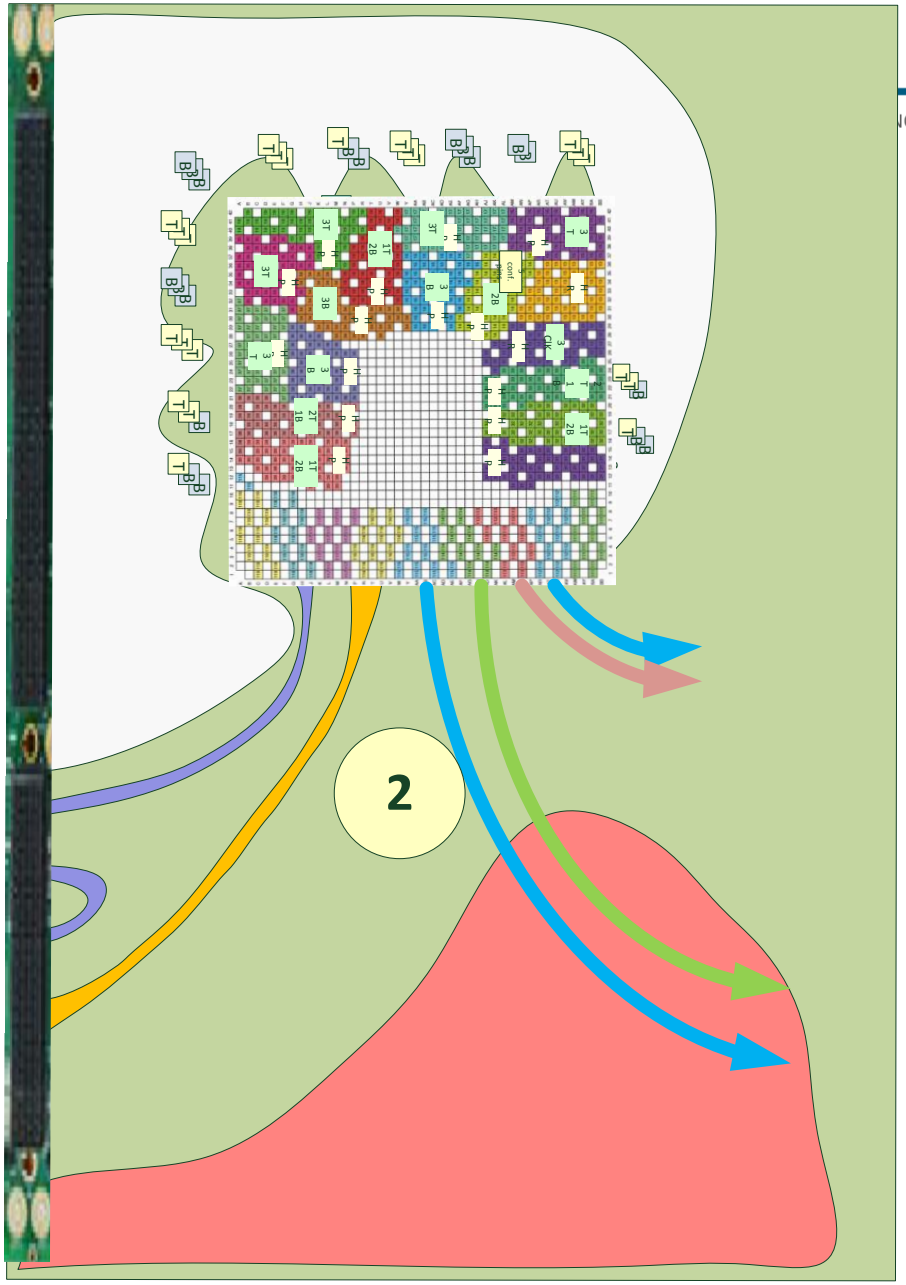
ADC technique



- Pipelined ADC, offering the best trade off between power consumption and sampling rate (100 mW/ channel)
- Serial outputs allow high integration level
- Variable sampling rate from 80 up to 166 MSPS,
- and higher rates in interleaving mode with reduced channel number, change to HMCAD 1520 offering internal interleaving mode

Open VPX Front board

Virtex FPGA chip surrounded with
40 4-channels ADCs,
resulting into 160 processing channels/board



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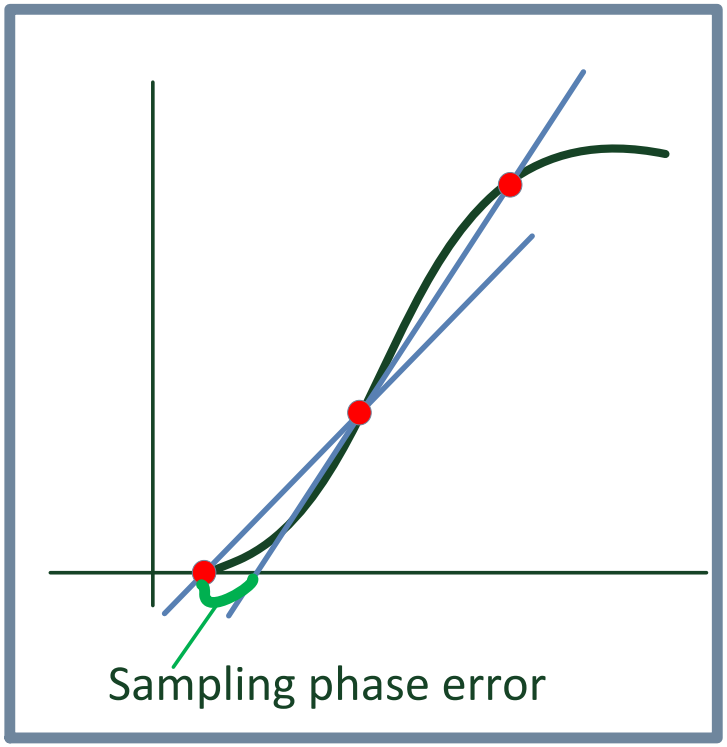
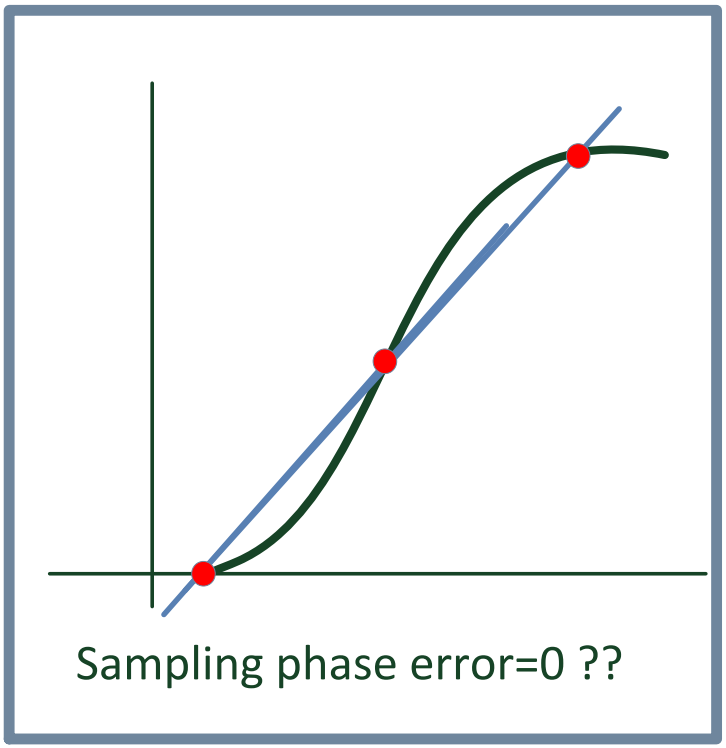
Sampling performance: two error contributions

noise ≀ Sampling phase





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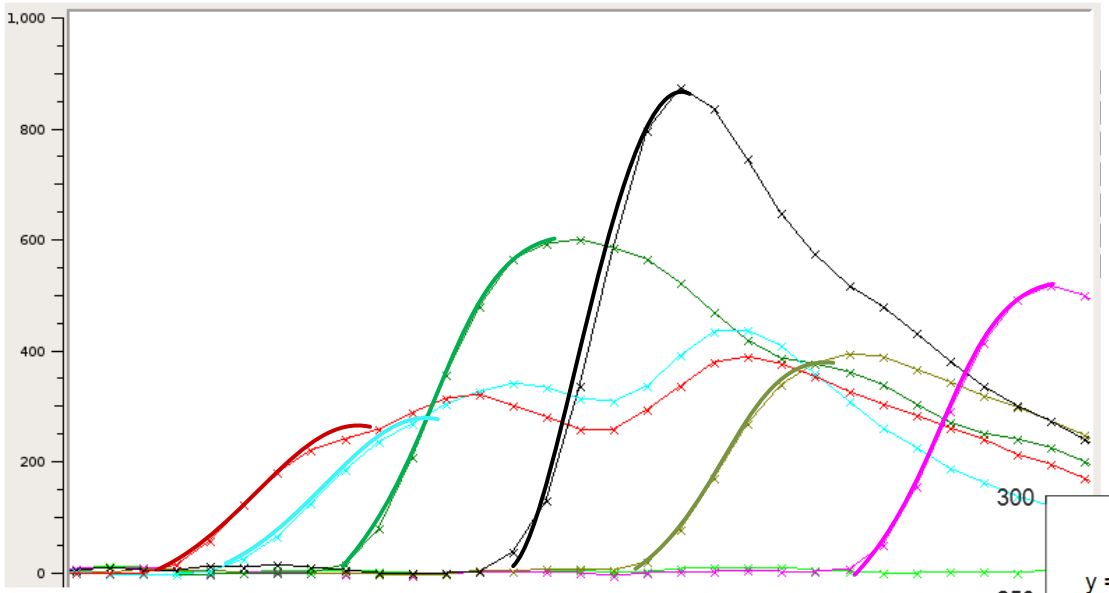
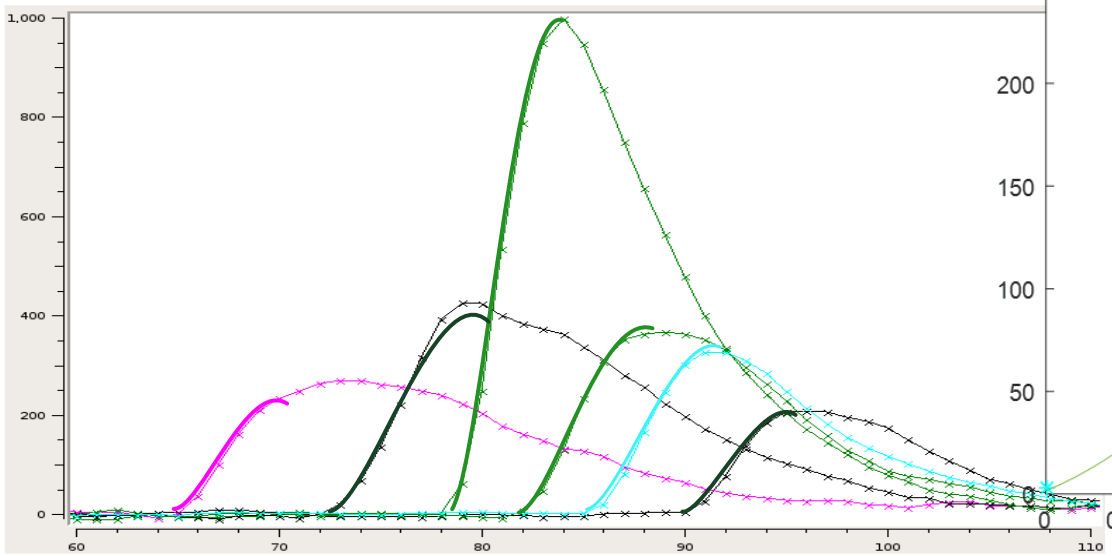
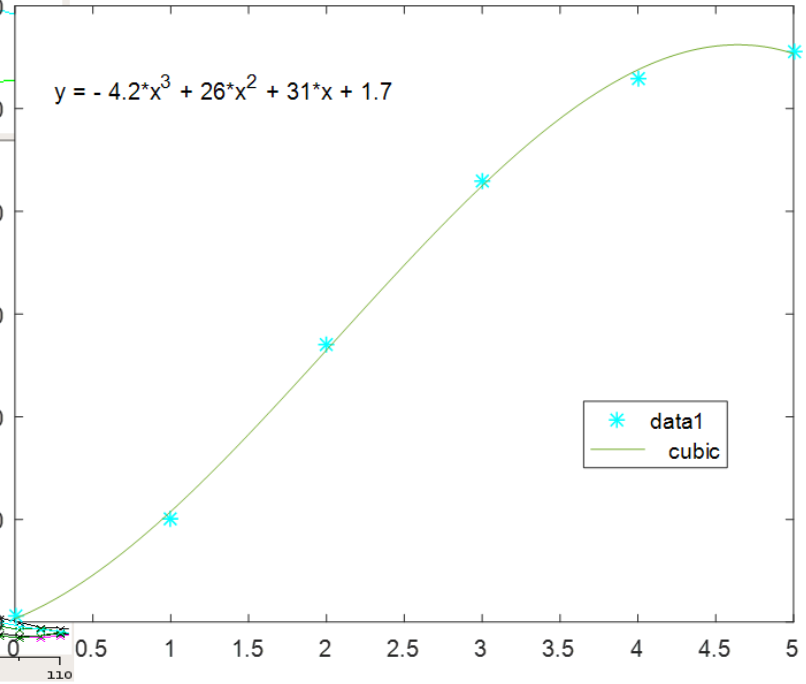
Rising edge fitting







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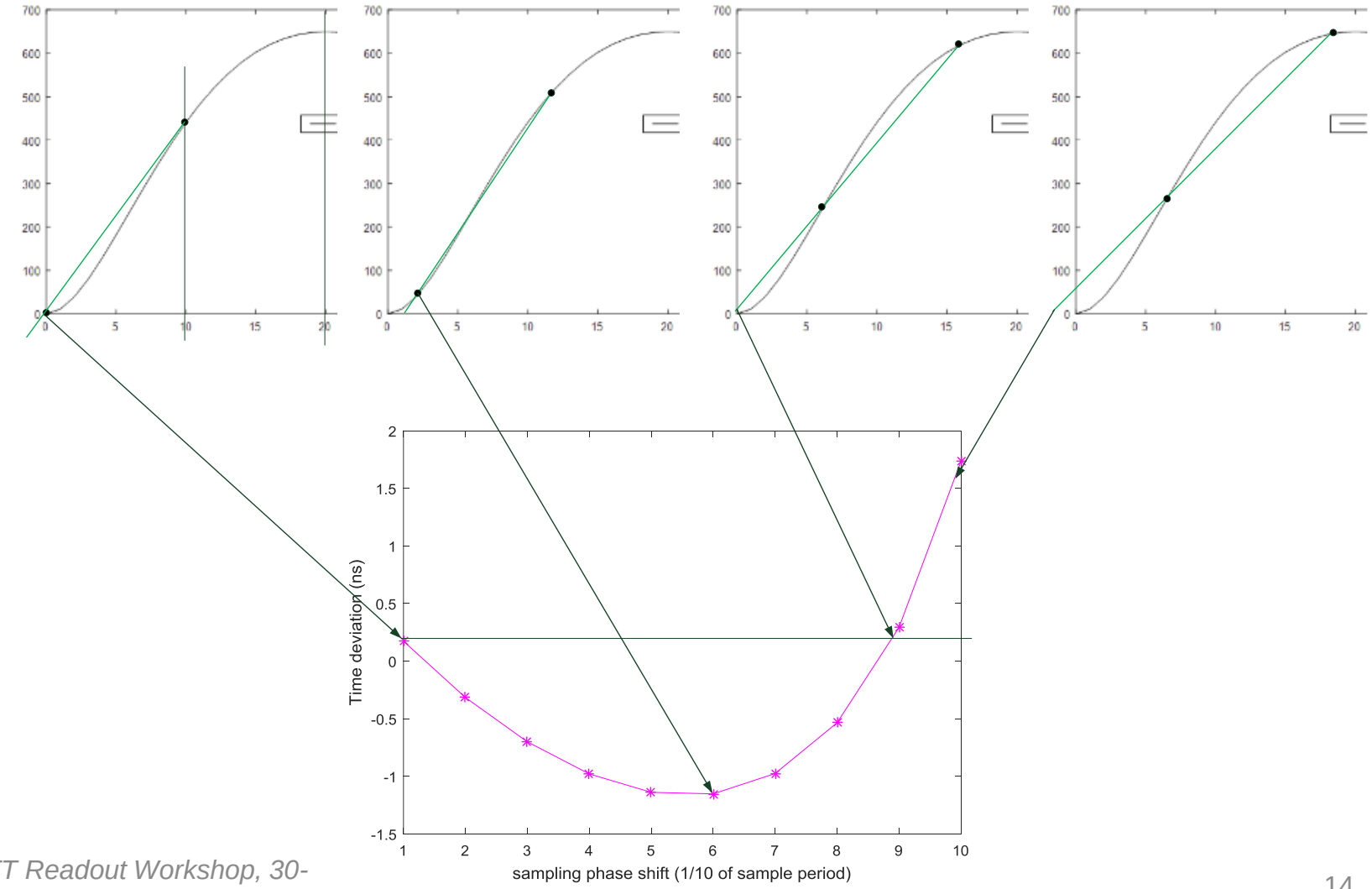
Mat Lab simulation: sampling phase error,
peaking time 20 ns, 100 MSPS



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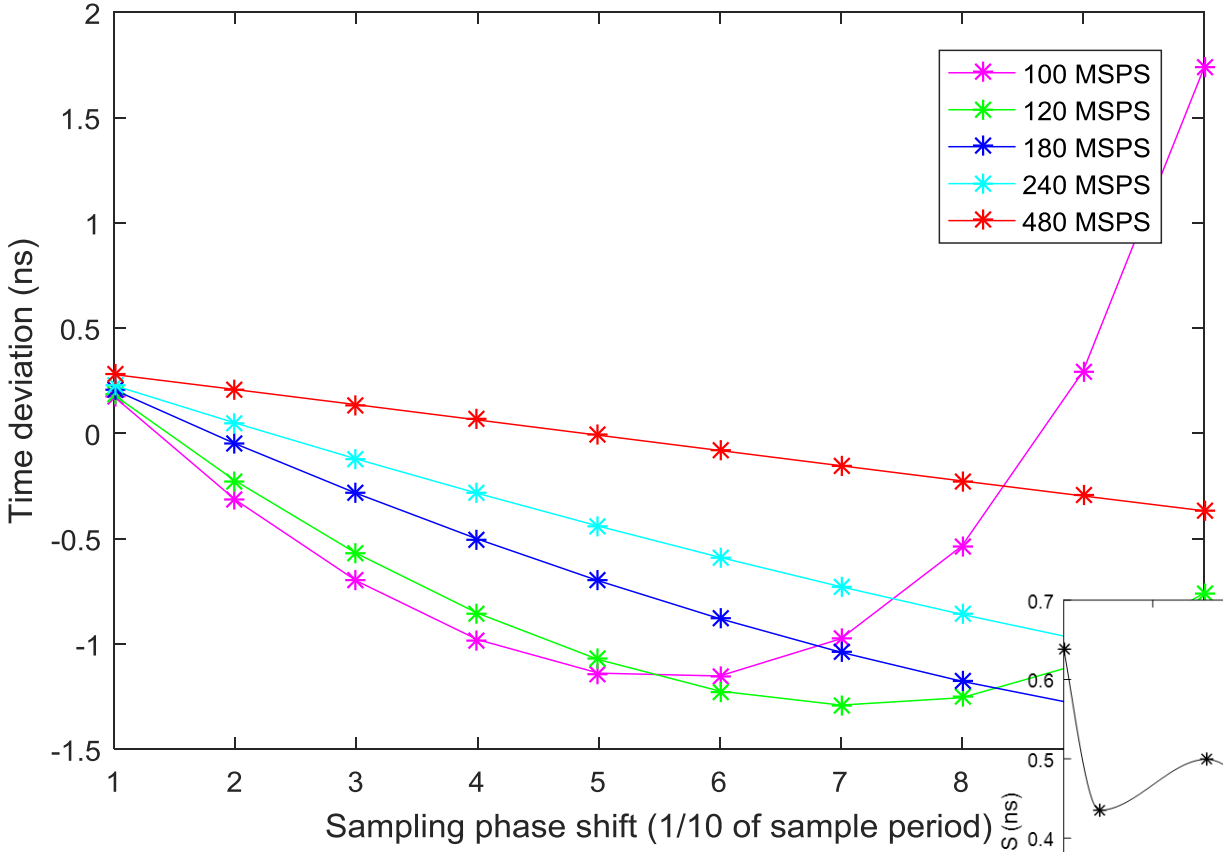
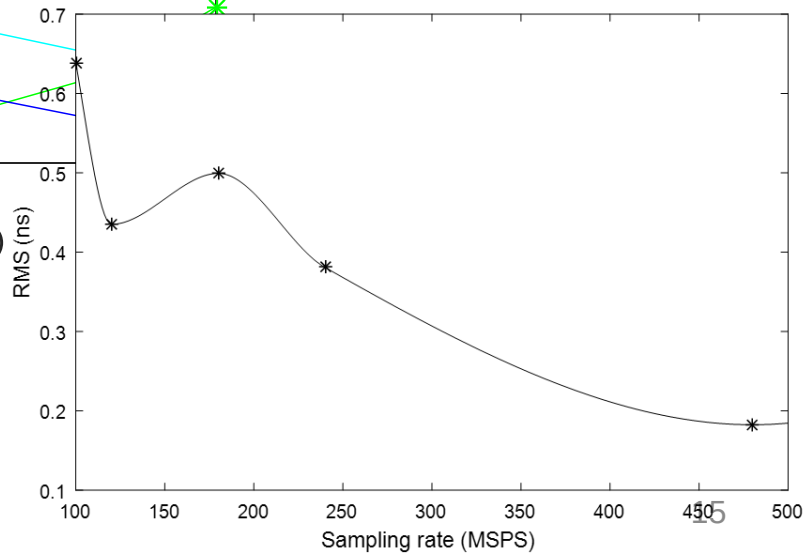
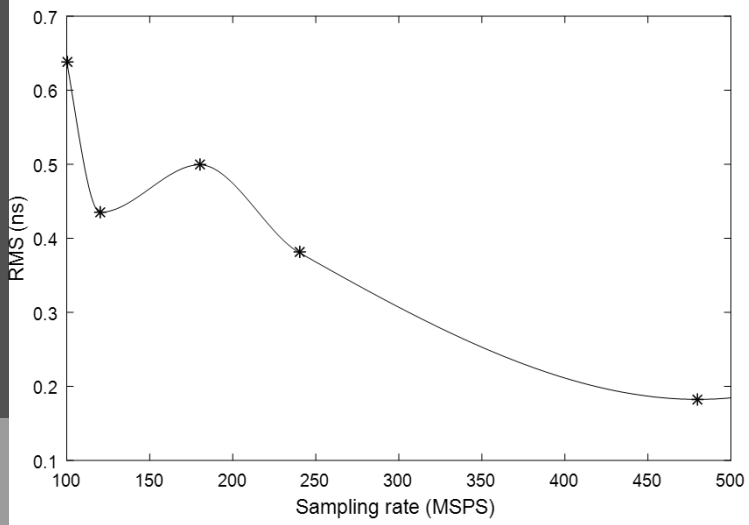
Mat Lab simulation: sampling phase error,
peaking time 20 ns, 100 -480 MSPS

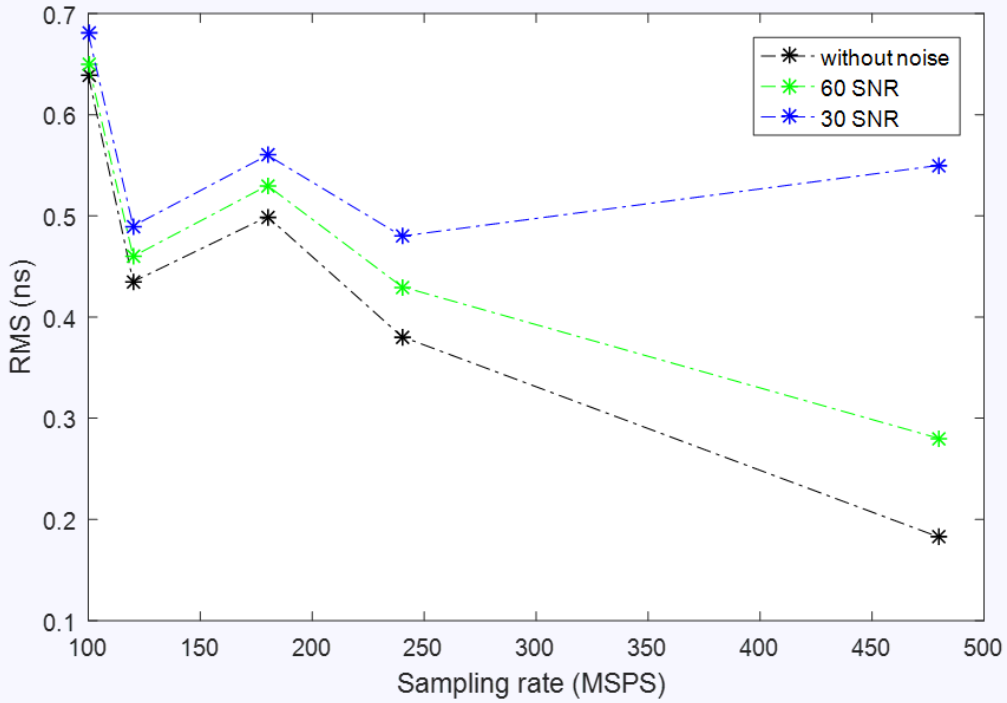




Mat Lab simulation: sampling phase error,
peaking time 20 ns, 100 -480 MSPS + Noise



Added white Gaussian noise with amplitude equal to 1,7 -3% of maximum amplifier value.



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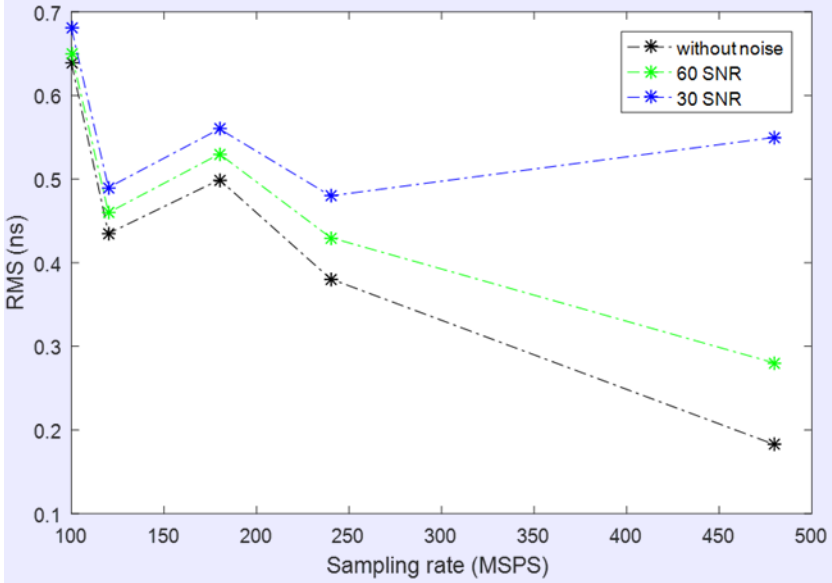
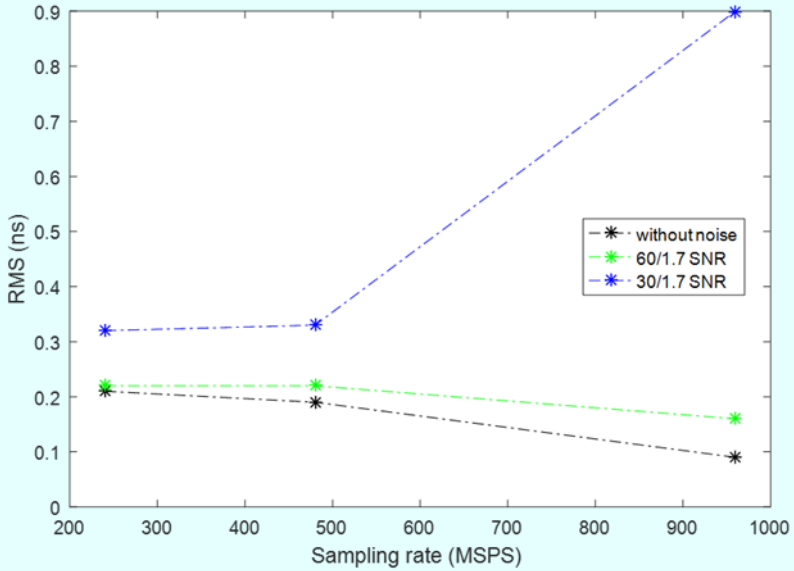
Accuracy dependent on sampling rate

Setup 1: Tpeak=20 ns, STT rising edge of 30-50 ns



110-200 MSPS →0,5 ns

Setup 2 (min peaking time by 12-m long cable): Tpeak=10 ns, STT rising edge of 15-30 ns



200-500 MSPS→0,25 ns

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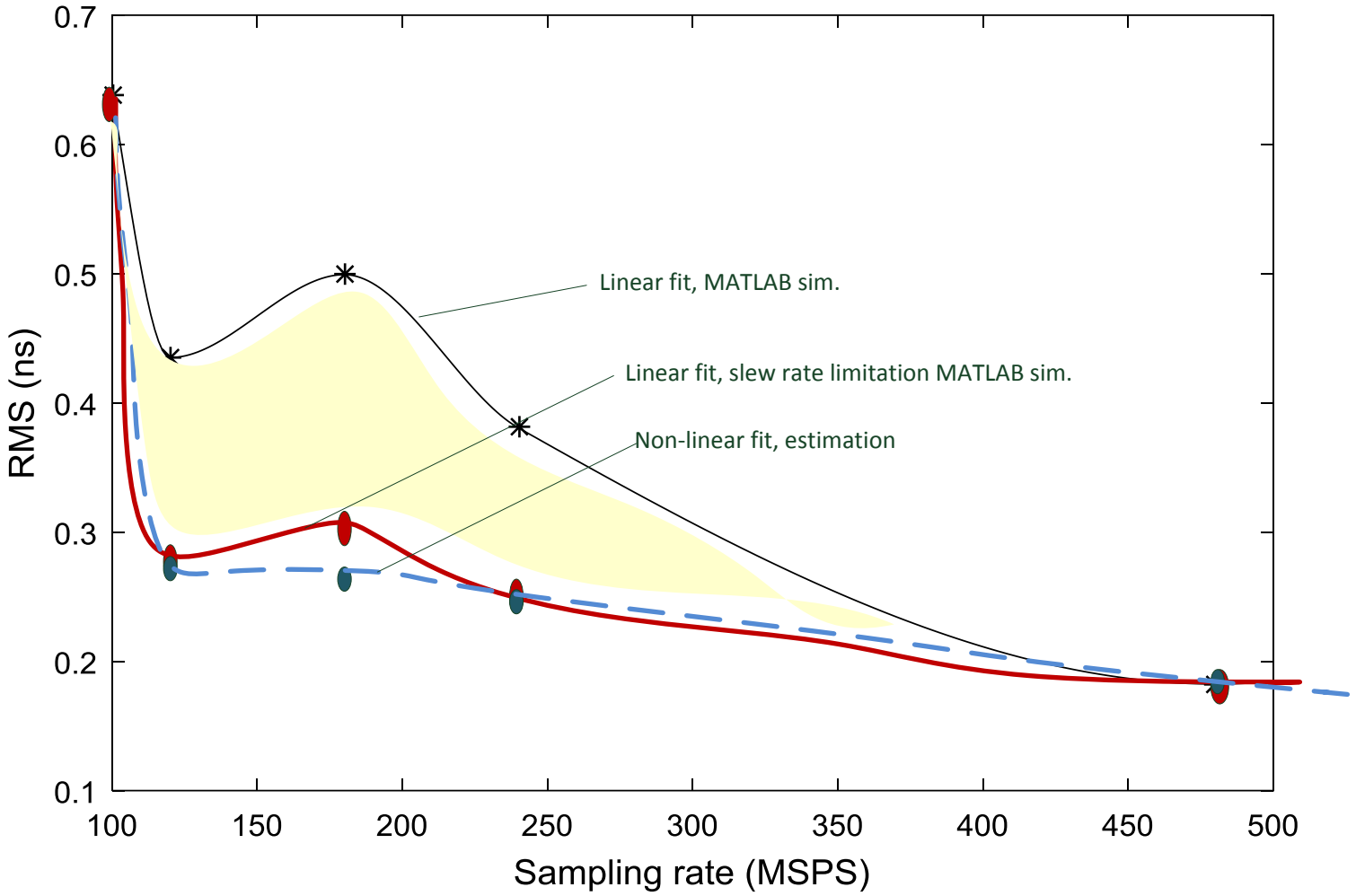
Time resolution: reserve



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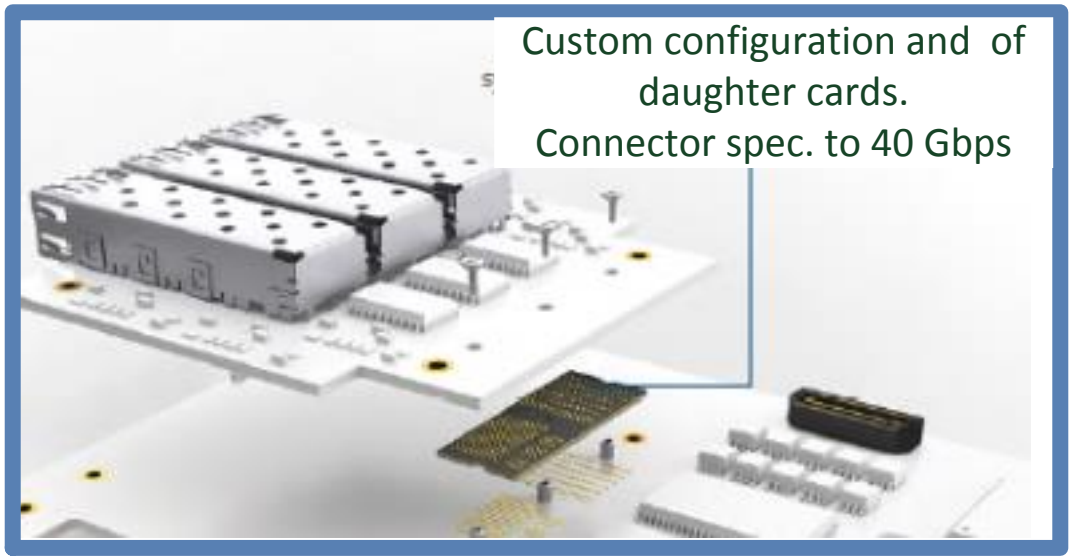
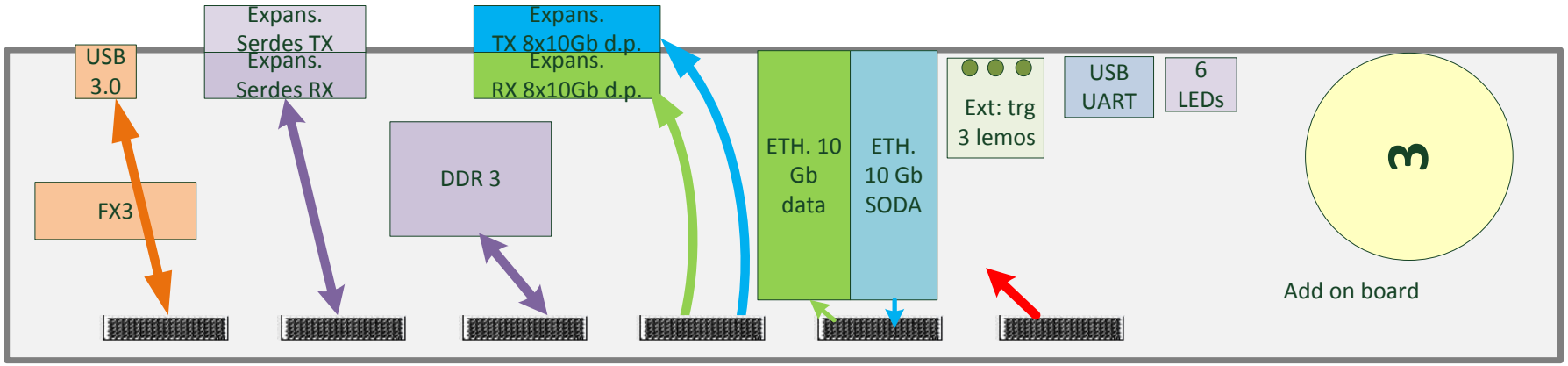
Board stacking: add-on-board





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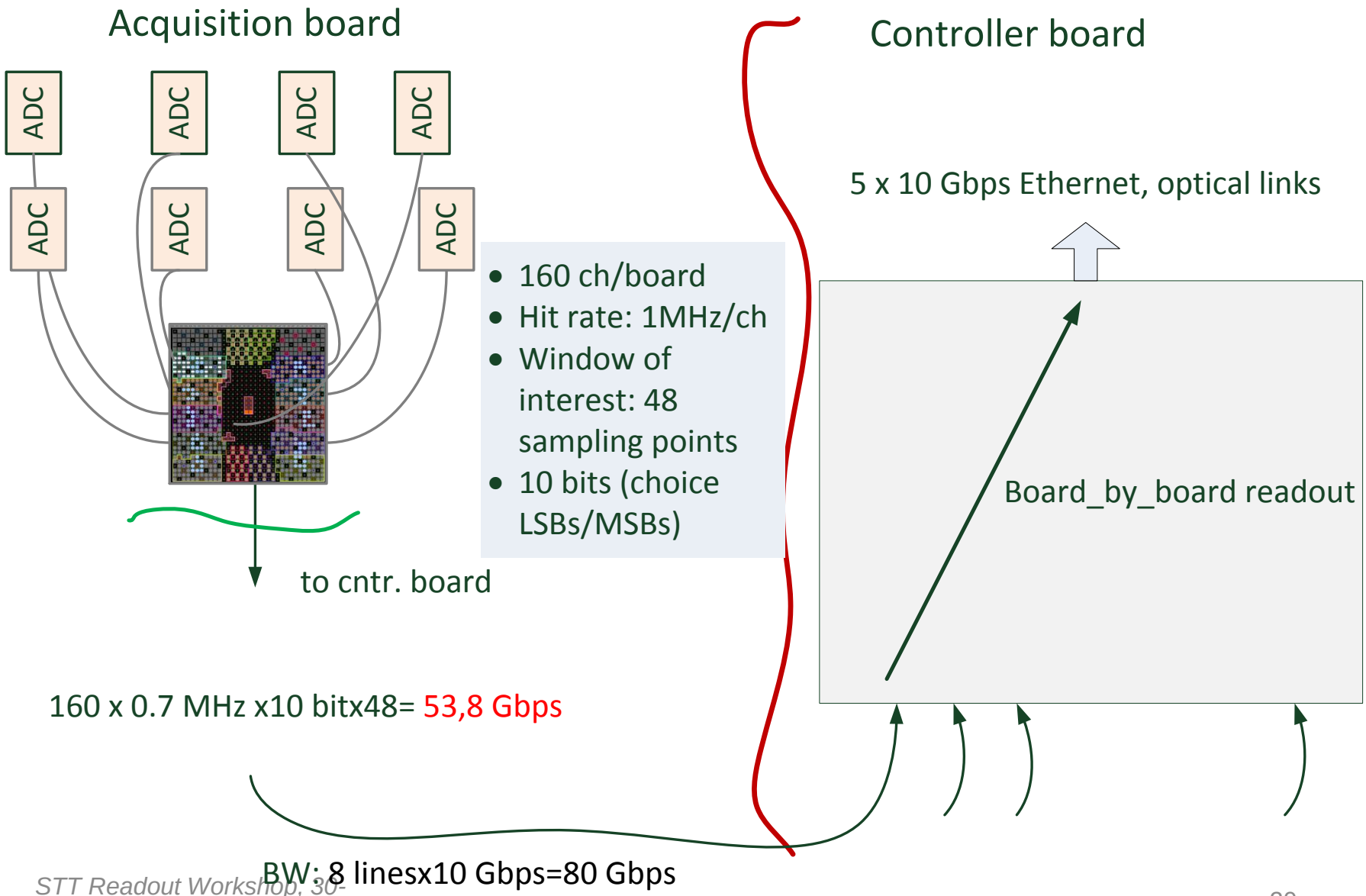
System throughput in dedicated RAW mode



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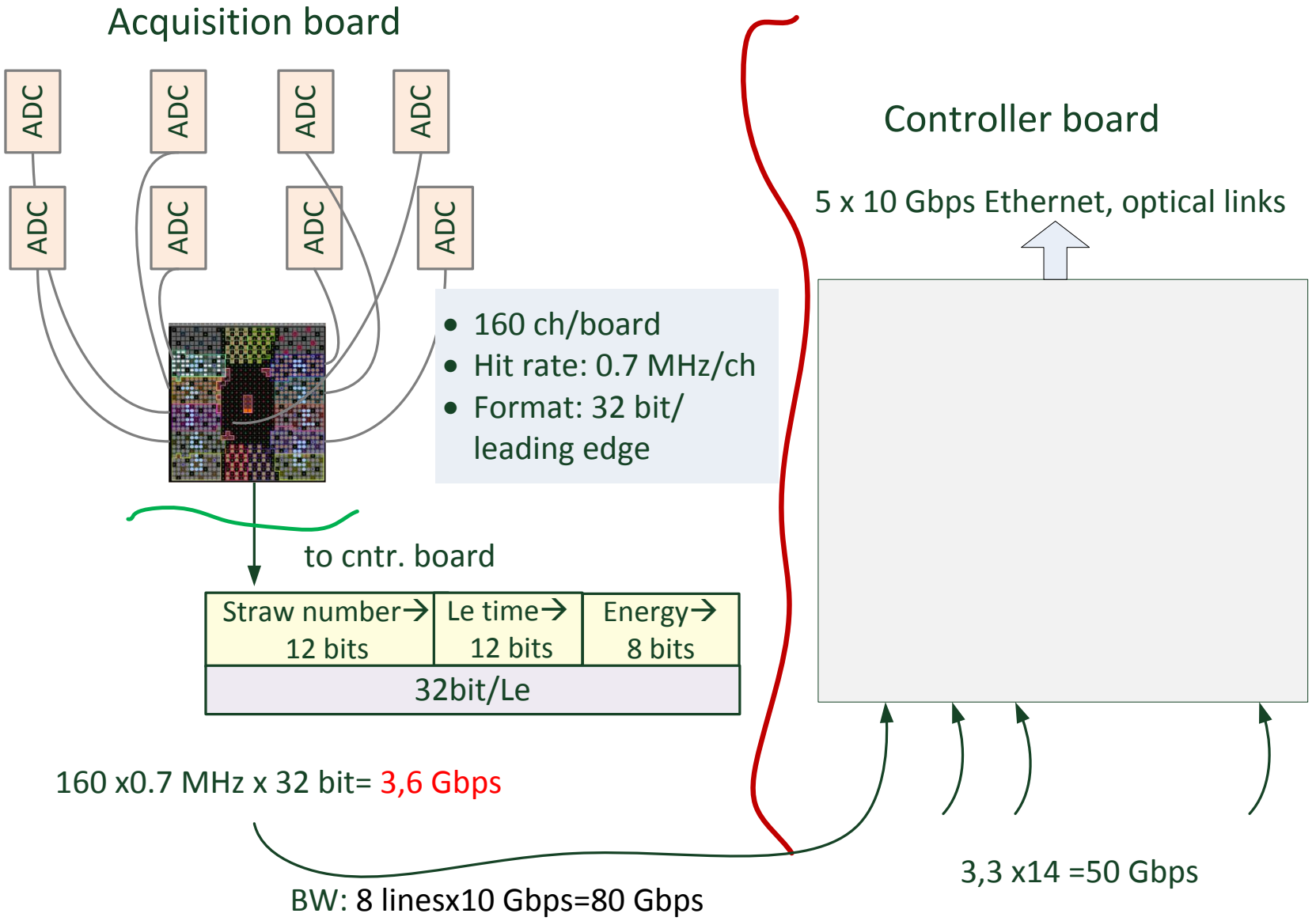
System throughput in time-sorted mode



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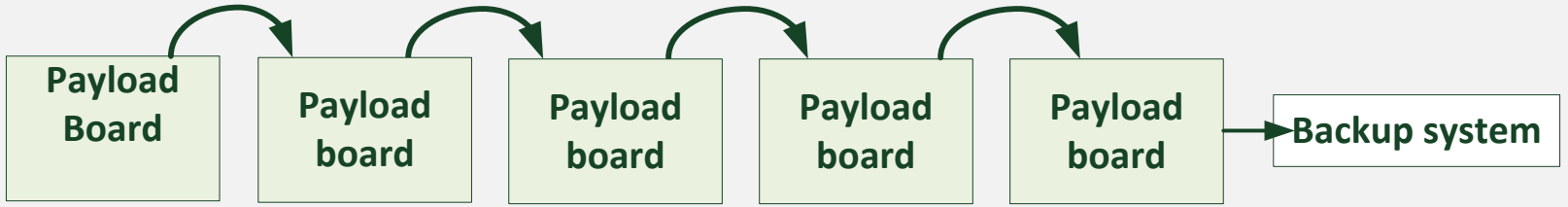
Configuration for Test Beam in 2017



- Board-to-board configuration with two data flow stitching on each board
- Operation without controller, the last board takes over this function
- 160x5= 800 channels
- Self triggered
- Time sorted of whole 800 channels stream
- Board by Board dedicated Raw data
- Communication via USB 3.0/10 Gbit Ethenet delivering data stream 3-10 Gbps

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Summary

- Design consists of 3 units: analog sampling/processing and communication;
- The layout of this units can be started in parallel;
- Analog unit is approved, shows a very good performance;
- Sampling/processing unit is designed to reach a very high system integration grade and allows data sorting and clustering. It is matched to analog unit to achieve a high perfomance;
- Whole design is simulated/evaluated and tested;

to do

- The noise influence will be increased with the higher channel count;
- 12 m cable crosstalk is not simulated/tested;
- Interleaving ADC is not tested;
- GTH Transceivers on Virtex are not proved.

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