# Status of ADC-based readout system for STT

# (FEE-free readout system for STT)

**Andreas Erven** *(Forschungszentrum Jülich, ZEA)*
**Tanja Hahnraths - von der Gracht** *(Forschungszentrum Jülich, IKP)*
**Lioubov Jokhovets** *(Forschungszentrum Jülich, ZEA)*
**Paweł Kulessa** *(IFJ PAN Kraków)*
**Henner Ohm** *(Forschungszentrum Jülich, IKP)*
**Krzysztof Pysz** *(IFJ PAN Kraków)*
**James Ritman** *(Forschungszentrum Jülich, IKP)*
**Thomas Sefzick** *(Forschungszentrum Jülich, IKP)*
**Valery Serdyuk** *(Forschungszentrum Jülich, IKP)*
**Peter Wintz** *(Forschungszentrum Jülich, IKP)*
**Solmaz Vejdani** *(Forschungszentrum Jülich, IKP, Univ. of Groningen)*

In this presentation the following information will be given:

- description and features of the method
- history of its development
- hardware (“analog part”)
- results obtained for proton and deuteron beam
- manpower

Ideas and status of digital part or readout chain will be given in next talk by Andreas Erven.

# Straw Tube Tracker - requirements

Time & amplitude readout (3d-space & energy loss)

$\sigma_{r\Phi} < 150$ μm, $\sigma_z < 2.8$ mm ← precise drift time determination, appropriate tracking algorithm

$\sigma_E / E < 10\%$ ← determination of the amount of charge released due to ionization, symmetrization of the energy loss distributions

Should be feasible

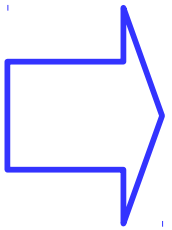
- at high counting rates (up to 1 MHz),
- in triggerless DAQ,
- with the single branch readout electronics.

# ADC-based readout - Method

1. Digitization of undistorted current signal from straw tube with sampling ADC

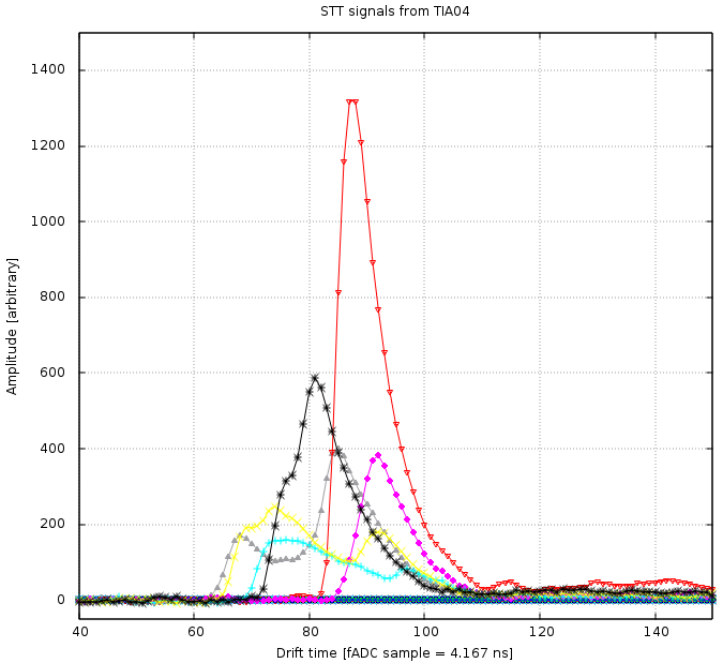
2. Fast pulse-shape analysis with FPGA

**Time determination**
**Energy loss determination**



**FPGA based real time pulse shape analysis:**

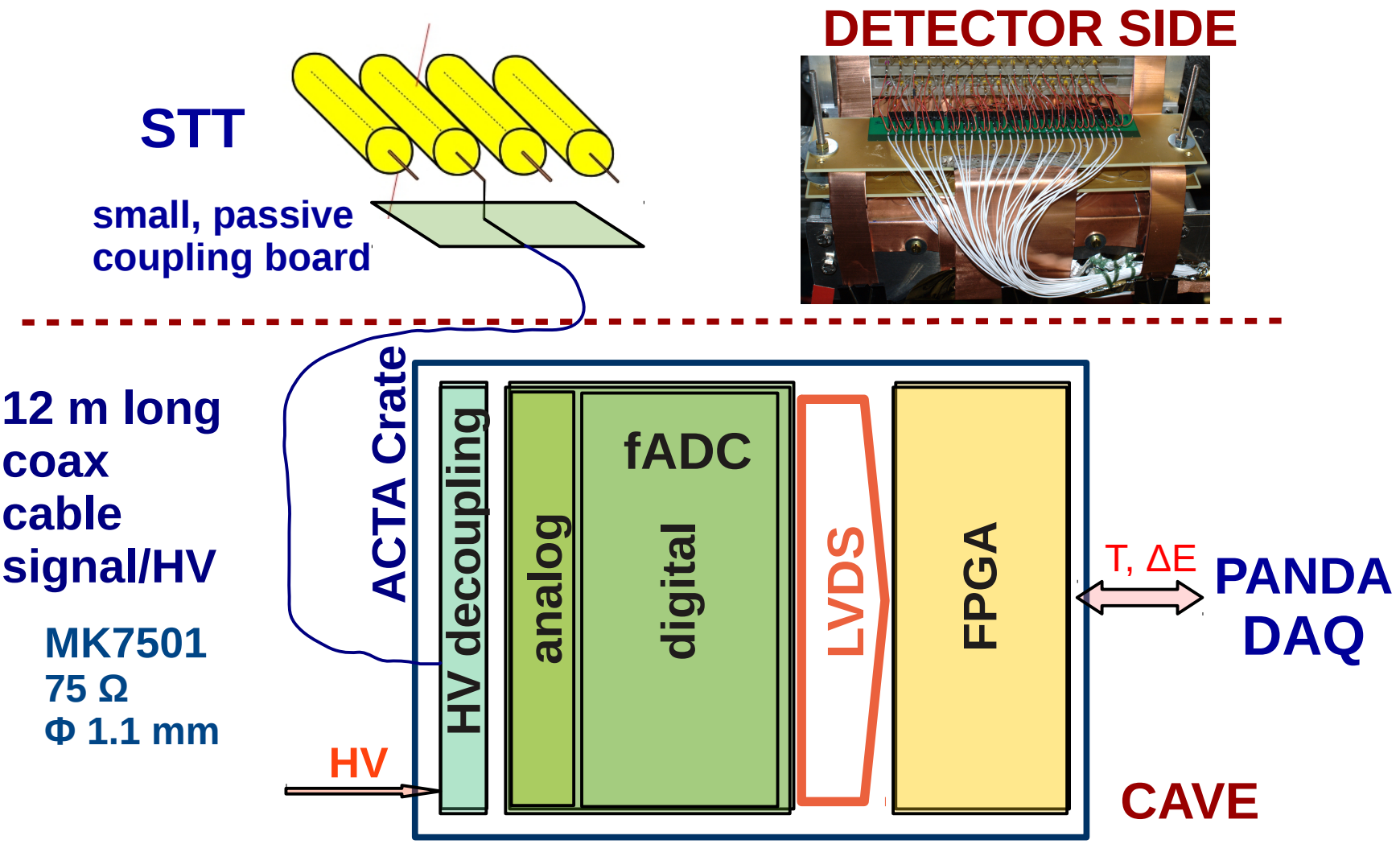
- base line determination,
- signal onset,
- pileup identification,
- rising edge slope calculation,
- zero crossing time,
- integrated charge,
- tail cancellation.




STT signals sampled and recorded with 240 MHz flashADC

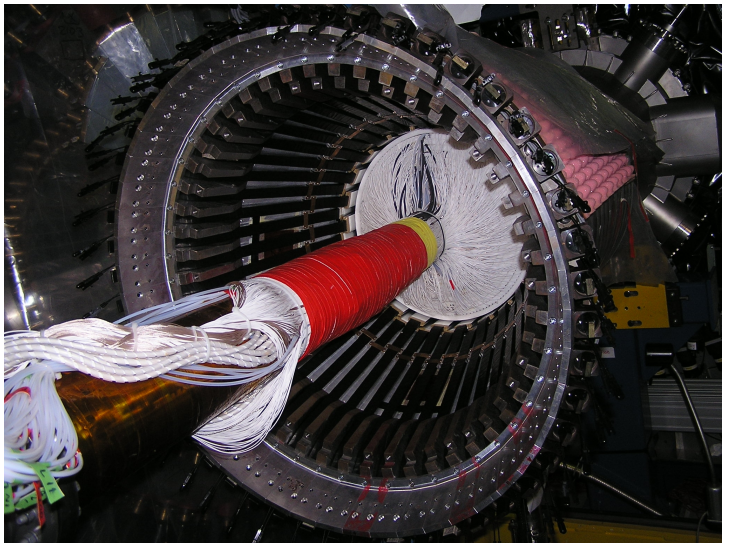
# Front End Electronics free readout system

**There is no active electronics in vicinity of detector (no FEE)**



# Advantages of FEE-free solution

- Existing space problem in the backward side of STT solved;
- Material budget in the backward side decreased;
- No heat release inside the STT barrel;
- No additional cables for HV and LV needed;
- No radiation damage of electronics;
- All components possibly subject to failure are accessible outside the detector;
- Broken tubes in the STT can be decoupled individually from HV.



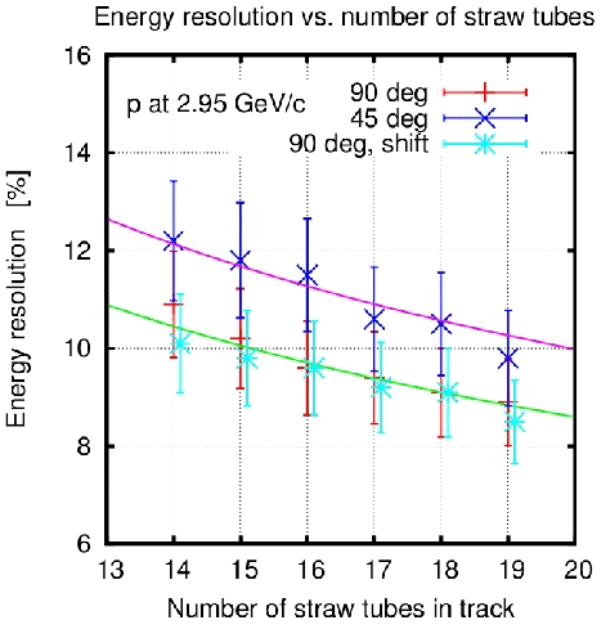
Example: MDC of WASA&COSY

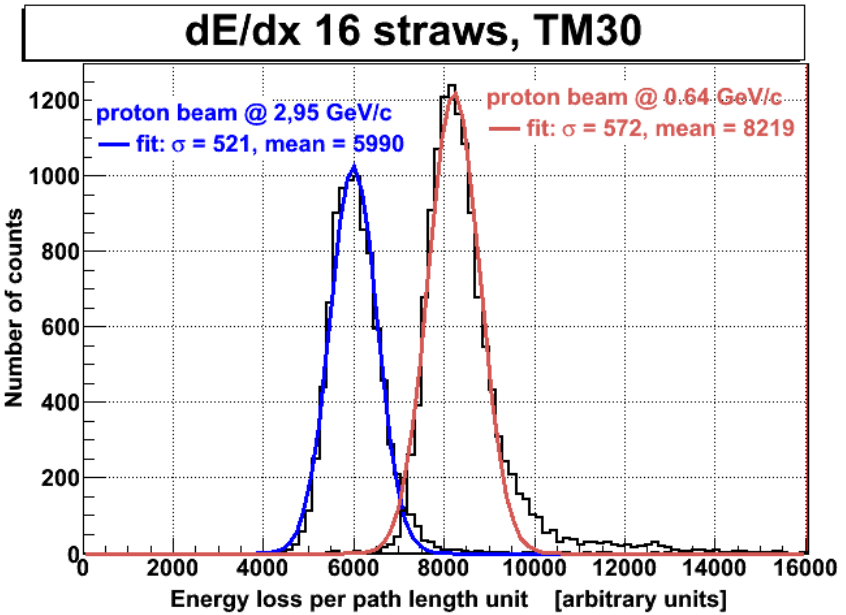
# Some history

2009 Beginning of experimental work oriented for experimental prove of particle identification feasibility by means of dE/dx measurement in multilayer STT

11. 2010 First beam test (2 days) with protons@3.GeV/c. 160 MHz fADC used. BigKarl. Readout optimized for dE measurement.

2011 Dedicated fast current amplifier, 240 MHz fADC, test at high beam intensities.



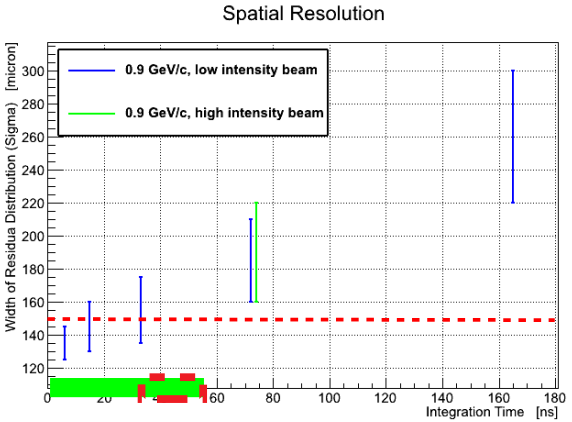



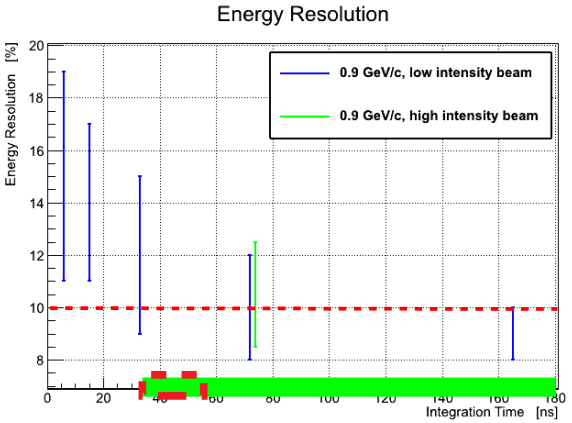

$\sigma_{dE/dx} = 8 \pm 1\ \%$

# Some history

2012 Simultaneous determination of time and dE with the dedicated one-branch electronic - Signal booster + Shaper + FADC

*With signal integration constant of 40 – 60 ns simultaneous and sufficiently precise energy- and position resolution is feasible.*




2013 Commitment of ZEL (ZEA-2). Idea of high integrated mutichannel flash ADC and fast FPGA for real time signal shape analysis.

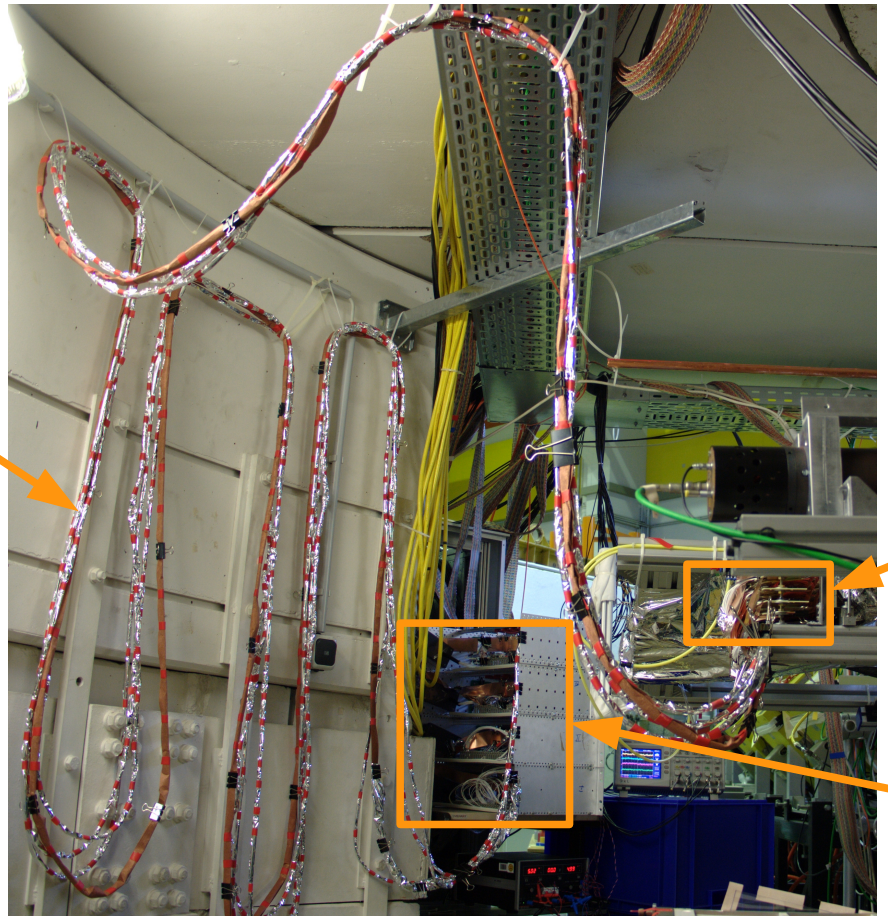
2014 Decision about FEE-free system. Optimized, low noise transimpedance amplifier as an input stage for new fADC.

# Some history

12. 2014 First beam test with FEE-free system – very promising results.

Cable Connection between the STT and the amplifiers

Bunches with 32 coaxial cables
Shielding: 12 µm Mylar + 2x50 nm Al



Cables:
12 m long,
operated at
HV = 1900 V

Connector end of the STT prototype

Crates with preamplifiers

# Some history

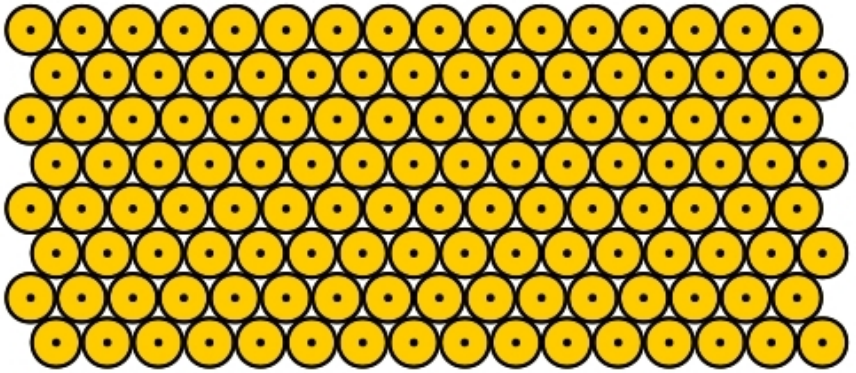
05. 2015 First beam test with prototype of new fADC (15 ch)

04. 2016 First beam time in COSY-TOF hall

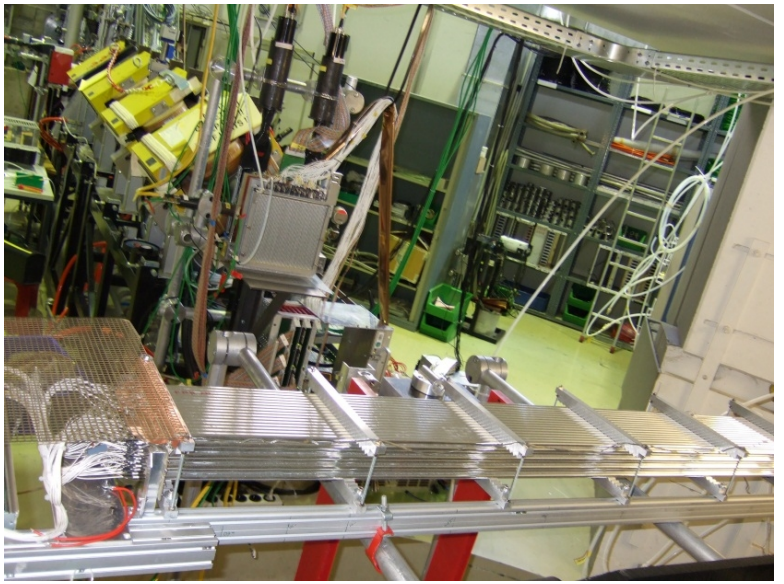
11. 2016 First beam test with prototype of new fADC with on-board integrated preamplifier (14 ch)

# STT prototype

COSY beam

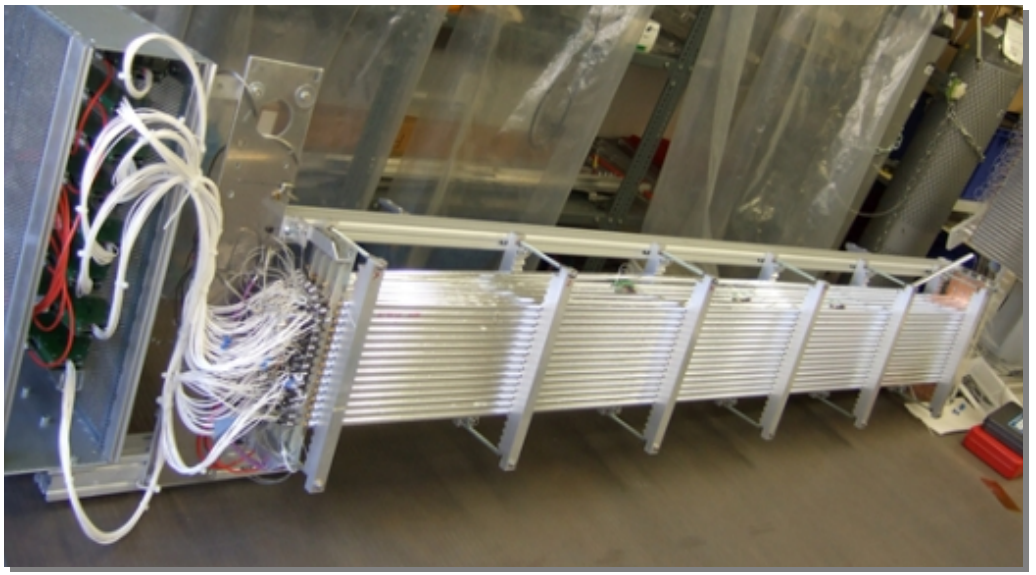


Setup are formed out of self supporting double layers.

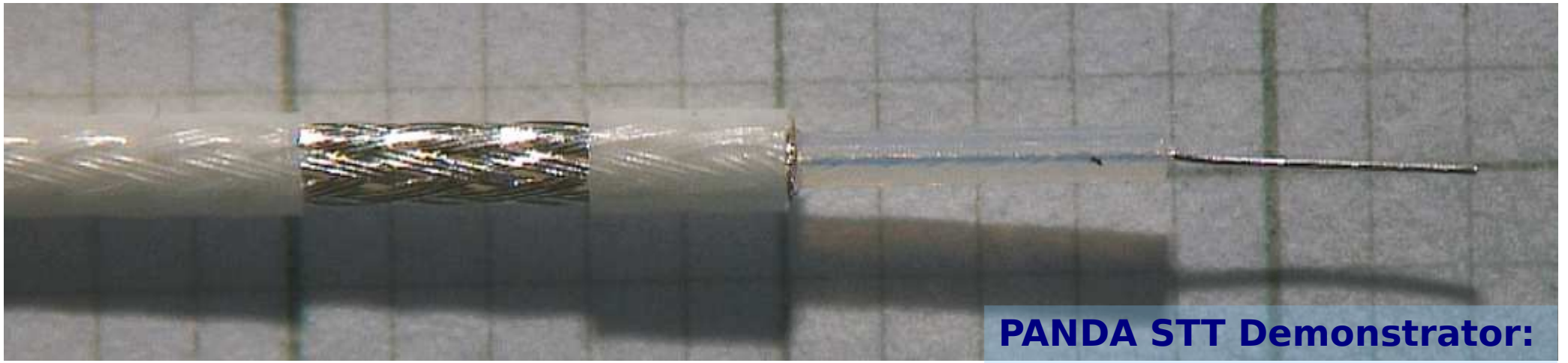


Each layers consist of 16 tubes:

- 1.5 m long
- Φ 10 mm
- 30 μm wall thickness
- 20 μm anode wire
- 1 bar overpressure
- gas mixture: Ar/CO2 (90/10)



# Signal/HV coax cables



**PANDA STT Demonstrator:**

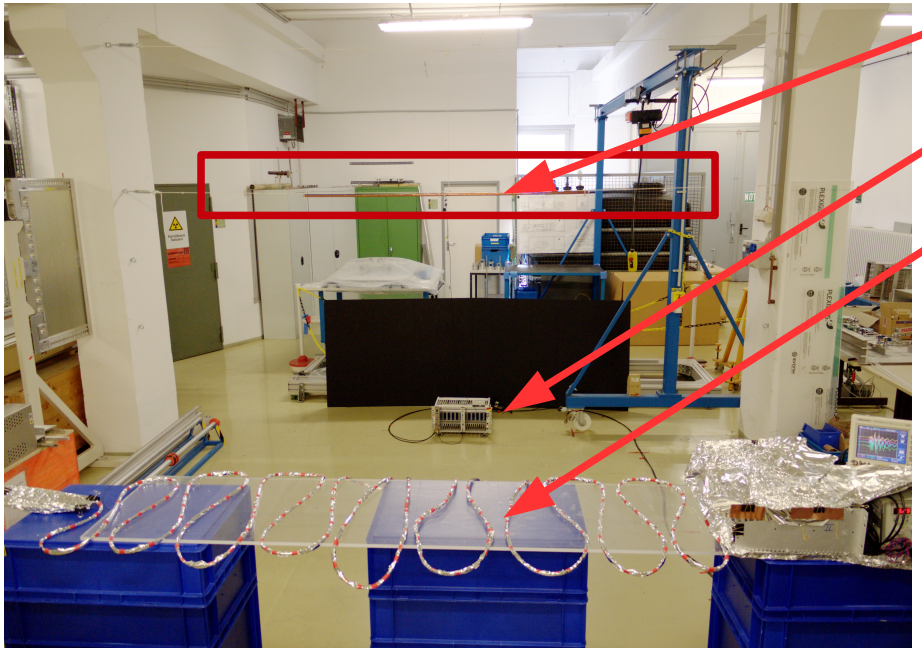
MK7501
Φ 1.1 mm
12 m long

**Important :**

- HV Stability
- protection against induced parasitic signals ("EMI")
- coupling to detector and back-end electronics

HV test at factory: 1000 V
routinely operated at 1800 V
Lab tests: stable at 4 kV

# Shielding against electromagnetic interference



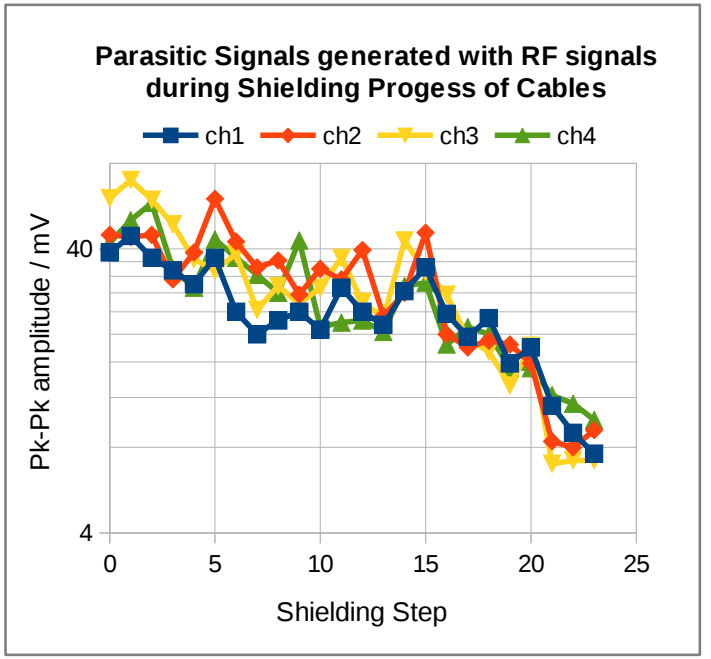
Transmitter dipole

Pulse generator

12 m long STT cables shielded with alu/mylar foil

EMI test area for detectors and electronical components

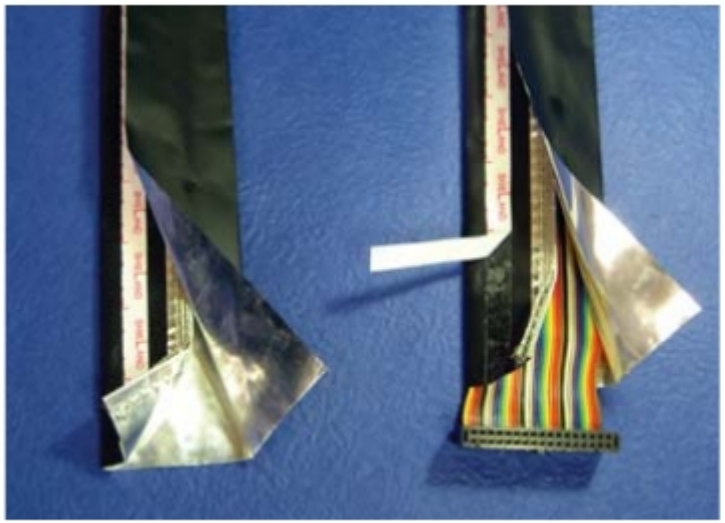
Reduction of induced signals during shielding progress



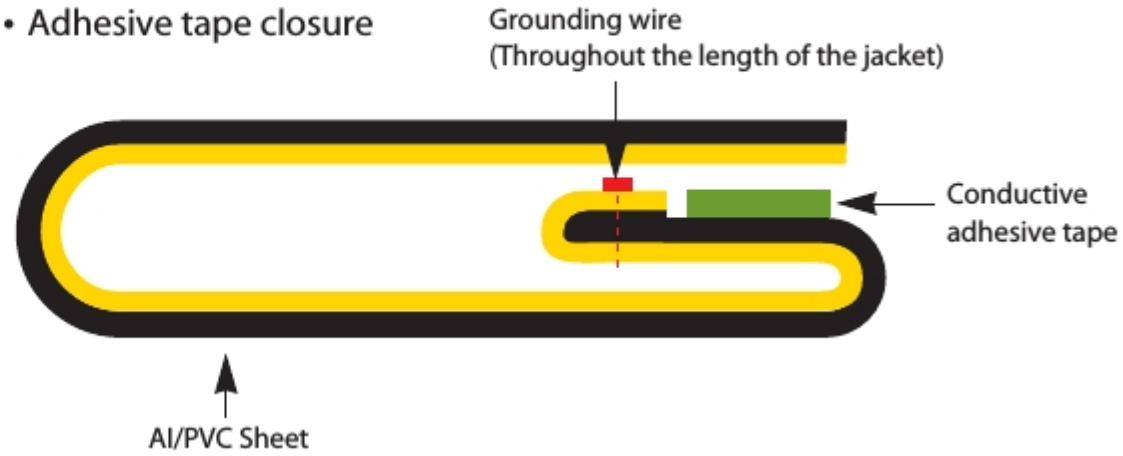

Shielding against EMI can be very effective. It is important to assure an uninterrupted shielding coat covering detector, cables and electronics, kept at detector ground potential.

# Cabling for FADC readout of PANDA STT – option 1

- 4224 channels
- readout/suppy by signal/HV coaxial cables, Ø = 1.1 mm
- no other electrical connections
- cables bundled up into groups o up to 20 pieces soldered at the back-end to the HV-decoupling board (PCB of 12 cm x 8.5 cm).
- each bundle is wrapped with the EMI shielding jacket, example:



- Aluminum foil laminated PVC jacket
- for flat cables
- Adhesive tape closure



# Cabling for FADC readout of PANDA STT – option 1

Assumptions (the worst case):

- length of cables outside detector: 10 m
- thickness of shielding jacket: 0.5 mm
- packing density factor: 1.2

Nominal cross-section of cables: 40 cm2
Nominal cross section of shielding: 20 cm2 Total: 60 cm2

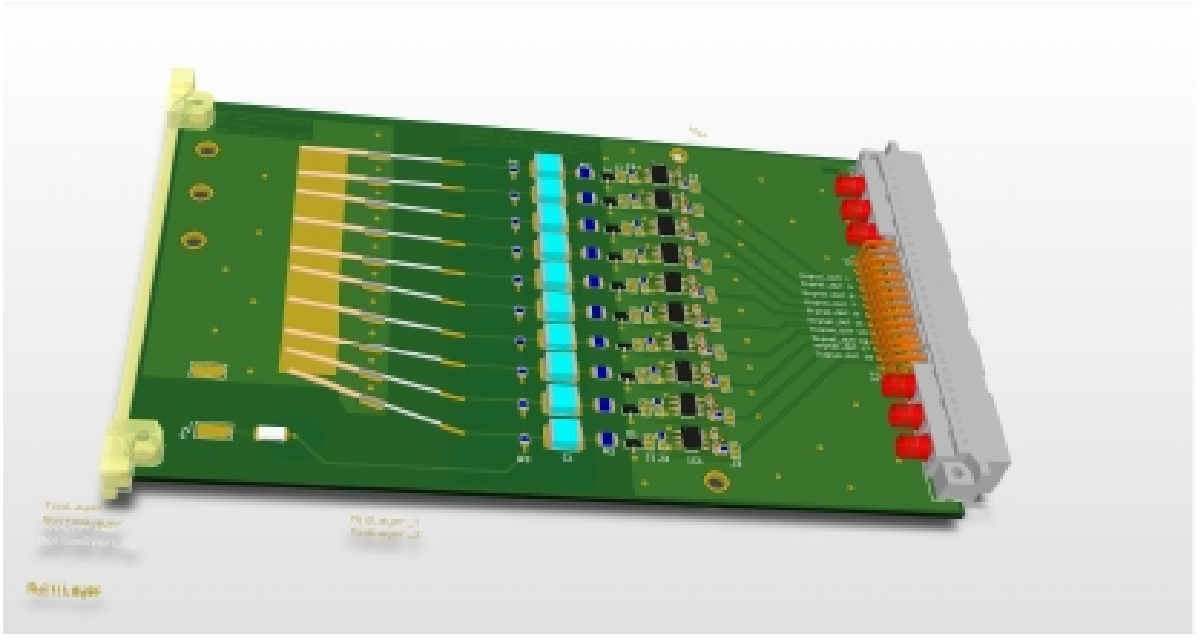
With realistic packing density factor 1.2: Total cross-section: 72 cm2

Nominal volume of cables: 40 l
Nominal volume of shielding: 20 l Total: 67 l
Nominal volume of decoupling boards: 7 l

With realistic packing density factor 1.2: Total volume: 80 l

Storage volume of cables disconnected from racks and rolled up into coil with Ø = 50 cm: 125 l (box of 0.5 m x 0.5 m x 0.5 m)

# Option 1 - HV decoupling board



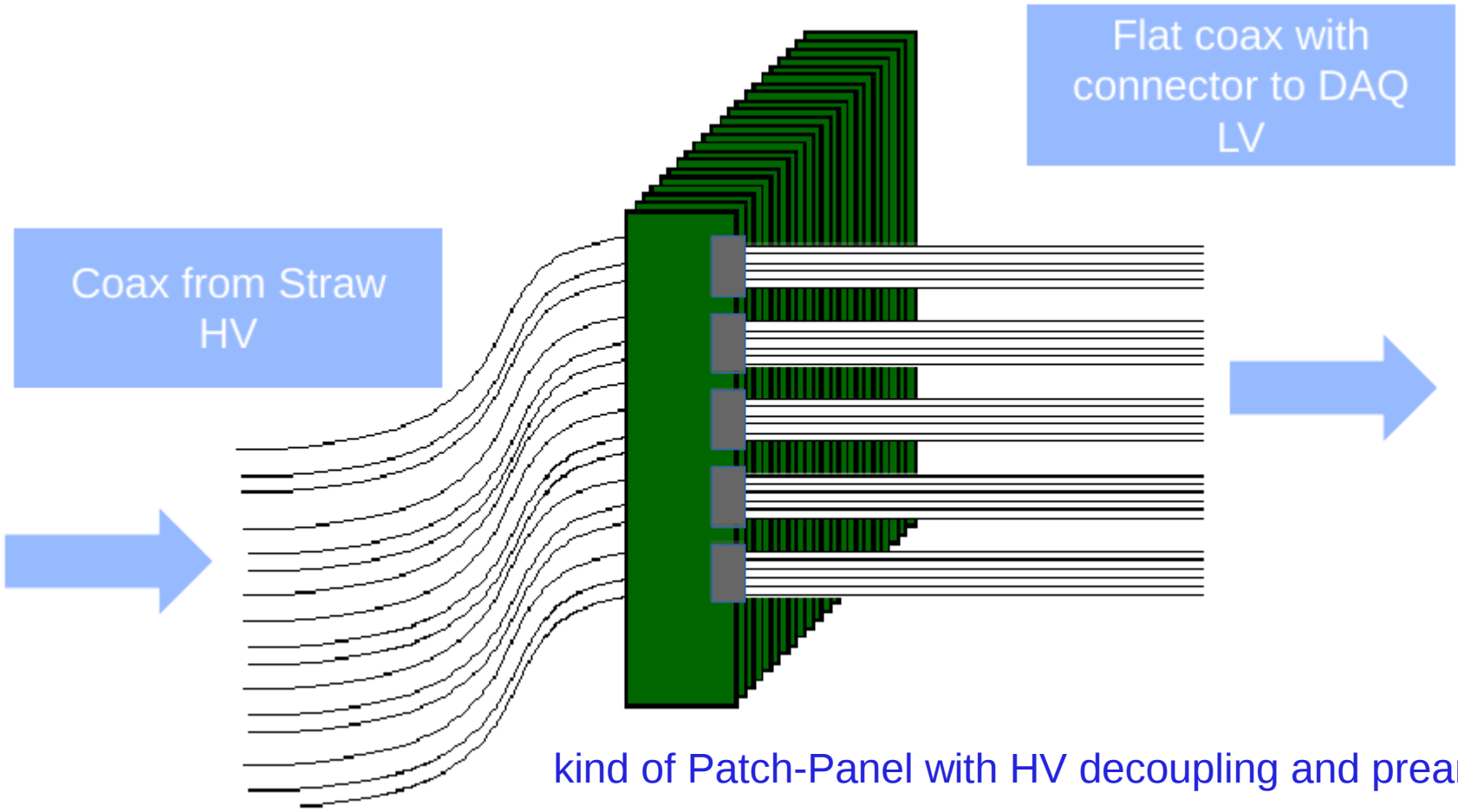
- needed at the cable back-end

- 20 channel

- may contain first stage of preamplifier

- design very advanced (IKP Electronics Workshop)

# Cabling for FADC readout of PANDA STT – option 2



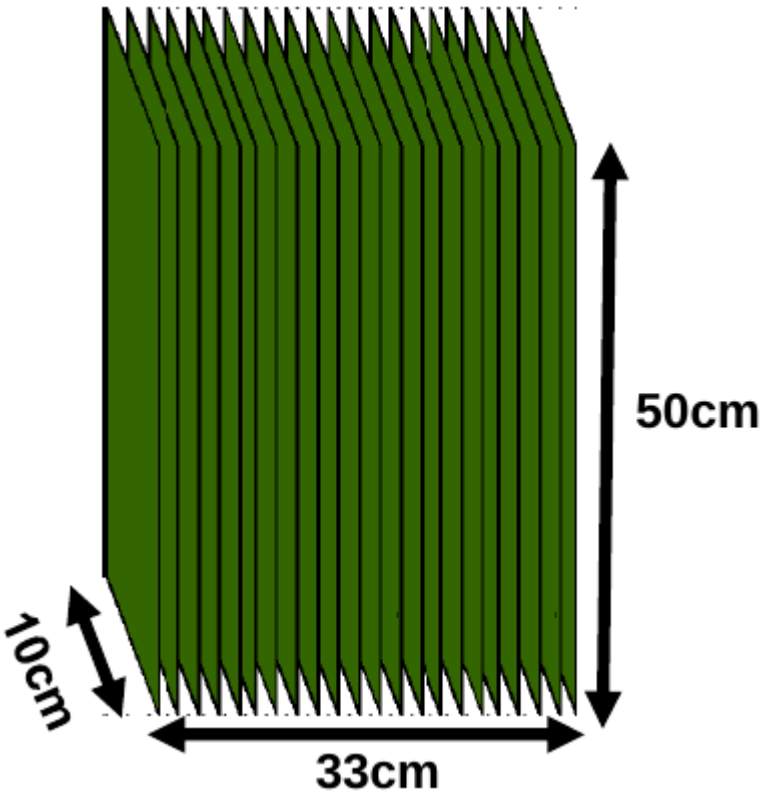

kind of Patch-Panel with HV decoupling and preamp

- shorter coaxial cables (shielding less critical)
- preamplifier closer to detector
- HV decoupling far from digital electronics

# Cabling for FADC readout of PANDA STT – option 2

Estimation of volume:

- boards 50 cm x 10 cm
- 100 channel per boards
- 2 x 22 boards needed
  (2 halves of detector)
- 1.5 cm distance board to board




Volume for half of detector: ~ 17 l
(+ crate)

Final idea still not fixed

# Results

All results presented here were obtained with readout chain composed of

- transimpedance amplifier

- 240 MHz, 16 ch flash ADC (inherited from from WASA-at-COSY)

for proton beams @

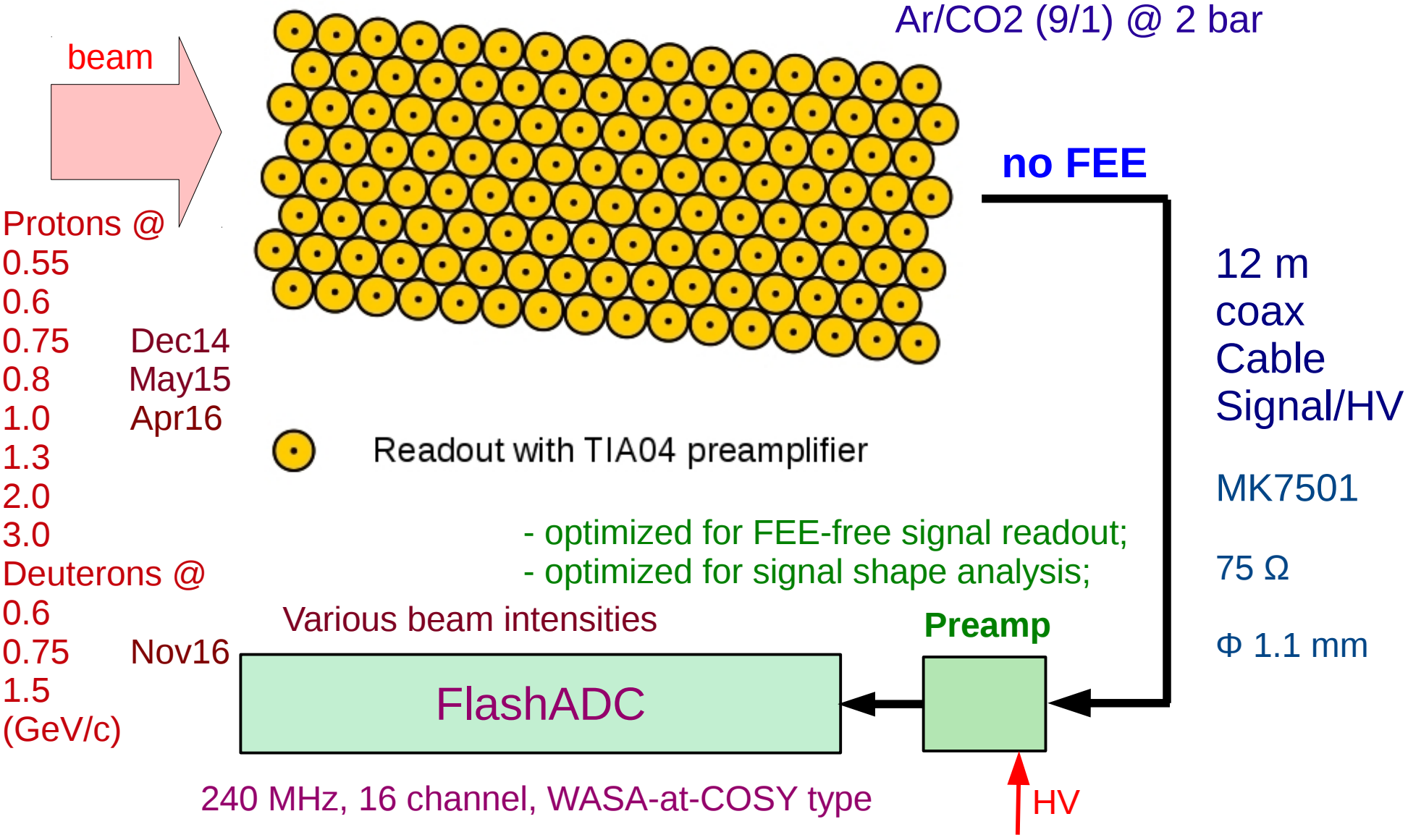
0.55, 0.60, 0.75, 0.80, 1.00, 1.30, 1.50, 2.00, 2.95 GeV/c

for deuteron beams @

0.60, 0.75. 1.50 GeV/c.

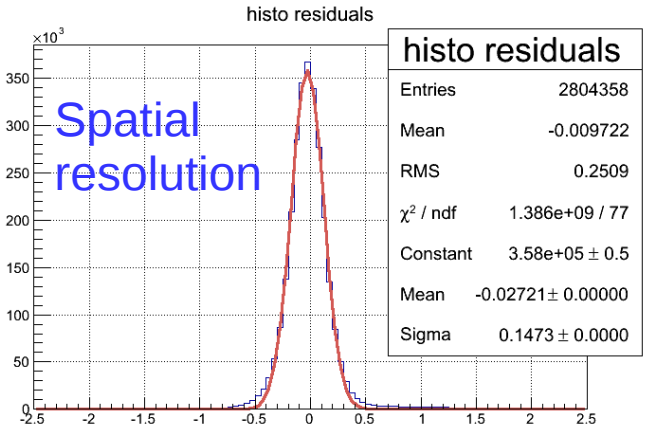
Raw data from fADC have been analyzed without use of FPGA.

# Setup for recent 4 beamtimes

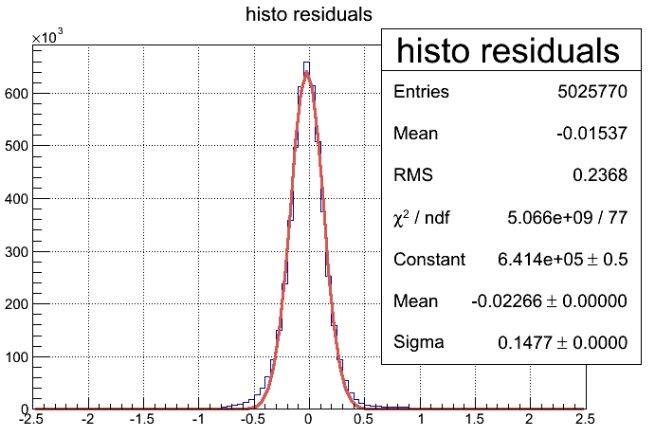


# Example of results from May '15 run

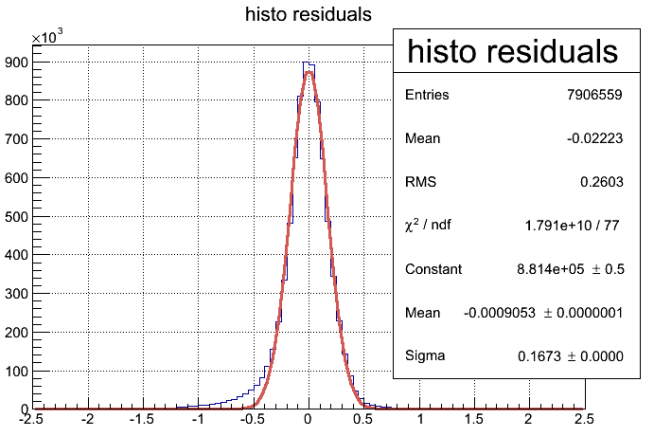
Spatial resolution




0.6 GeV/c

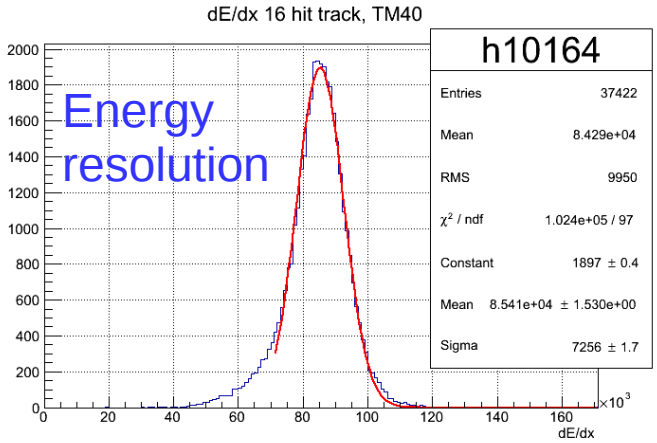


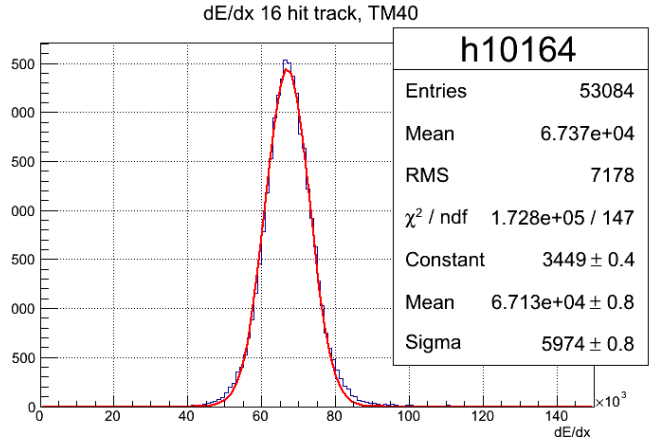

0.8 GeV/c

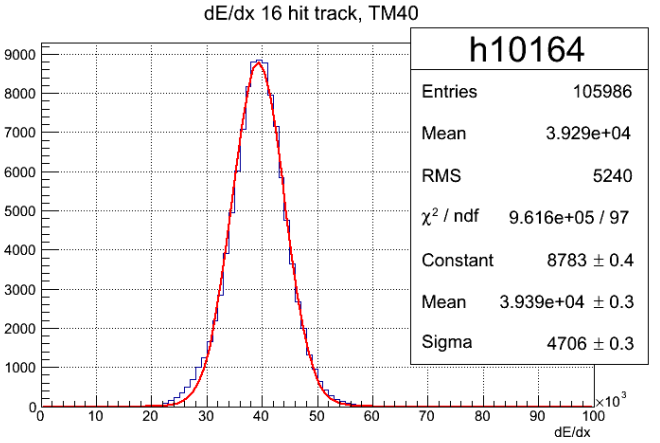



3.0 GeV/c

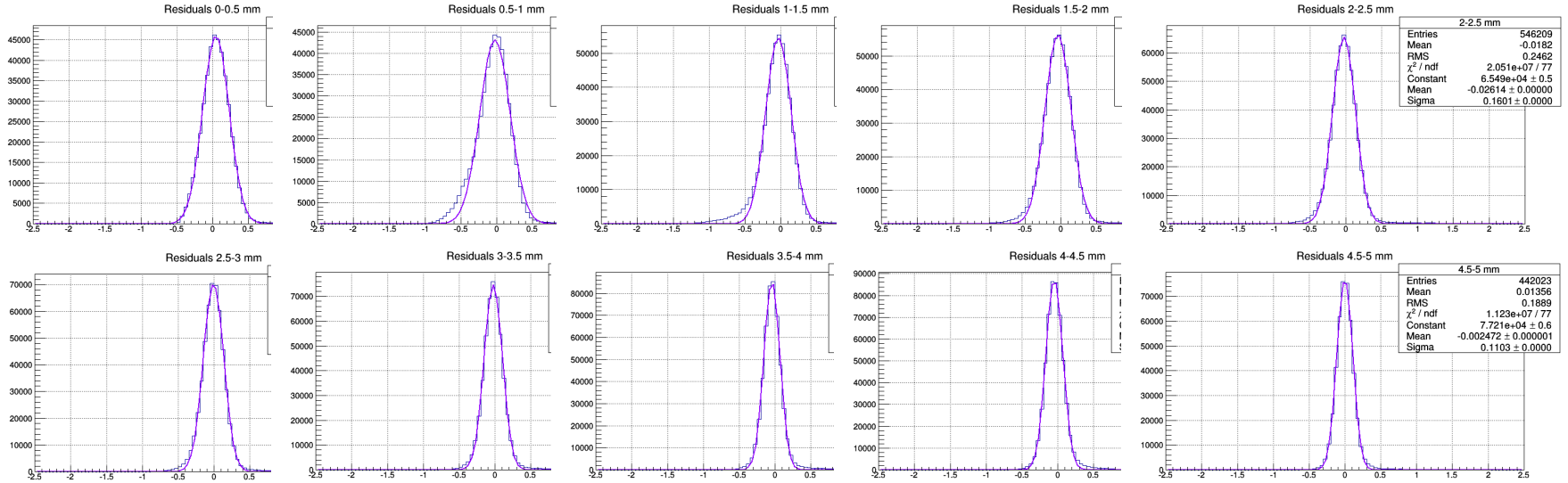
Energy resolution

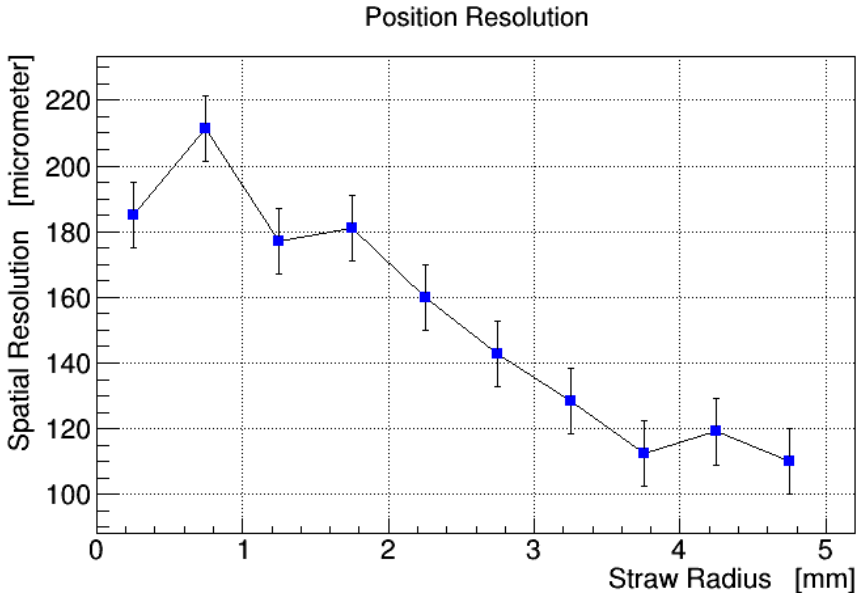


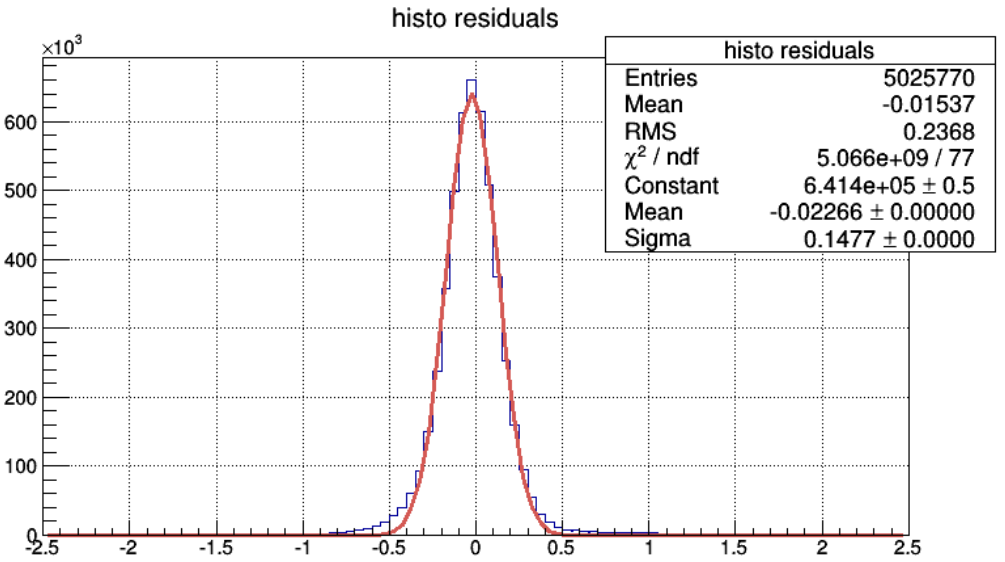



# May 15: residua distributions example for 0.8 GeV/c (1800V)



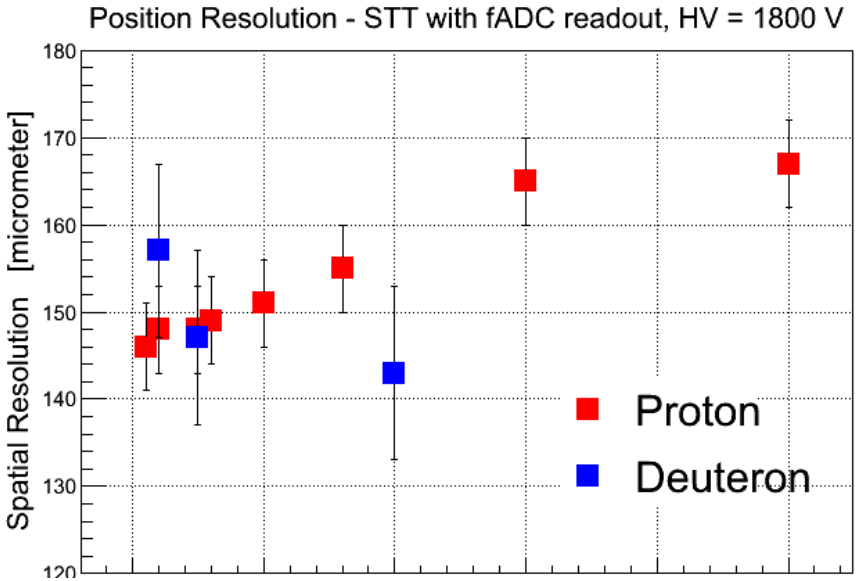



# Summary of results with WASA fADC

All beam momenta

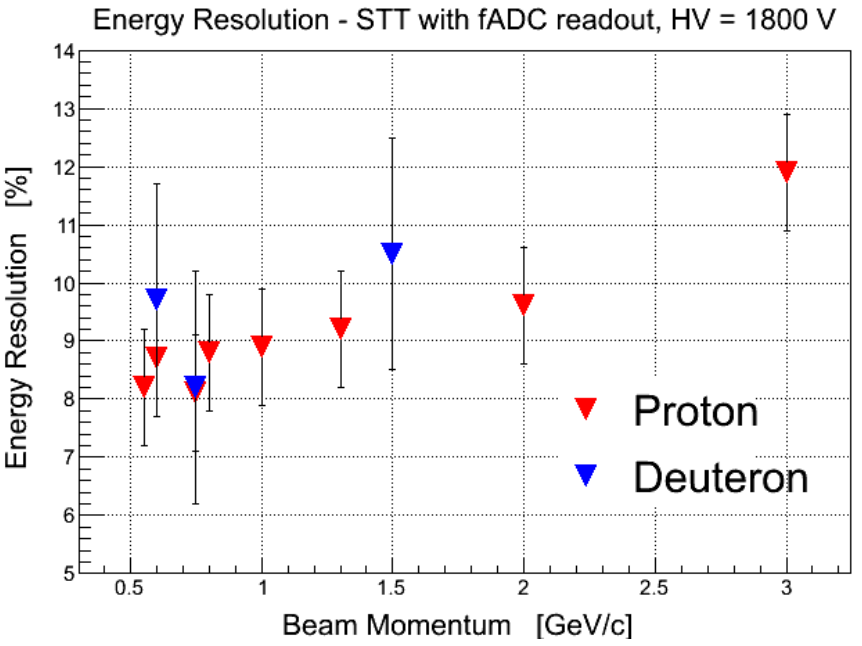
Presented results are only for reconstructed tracks of 16 hits

HV = 1800 V



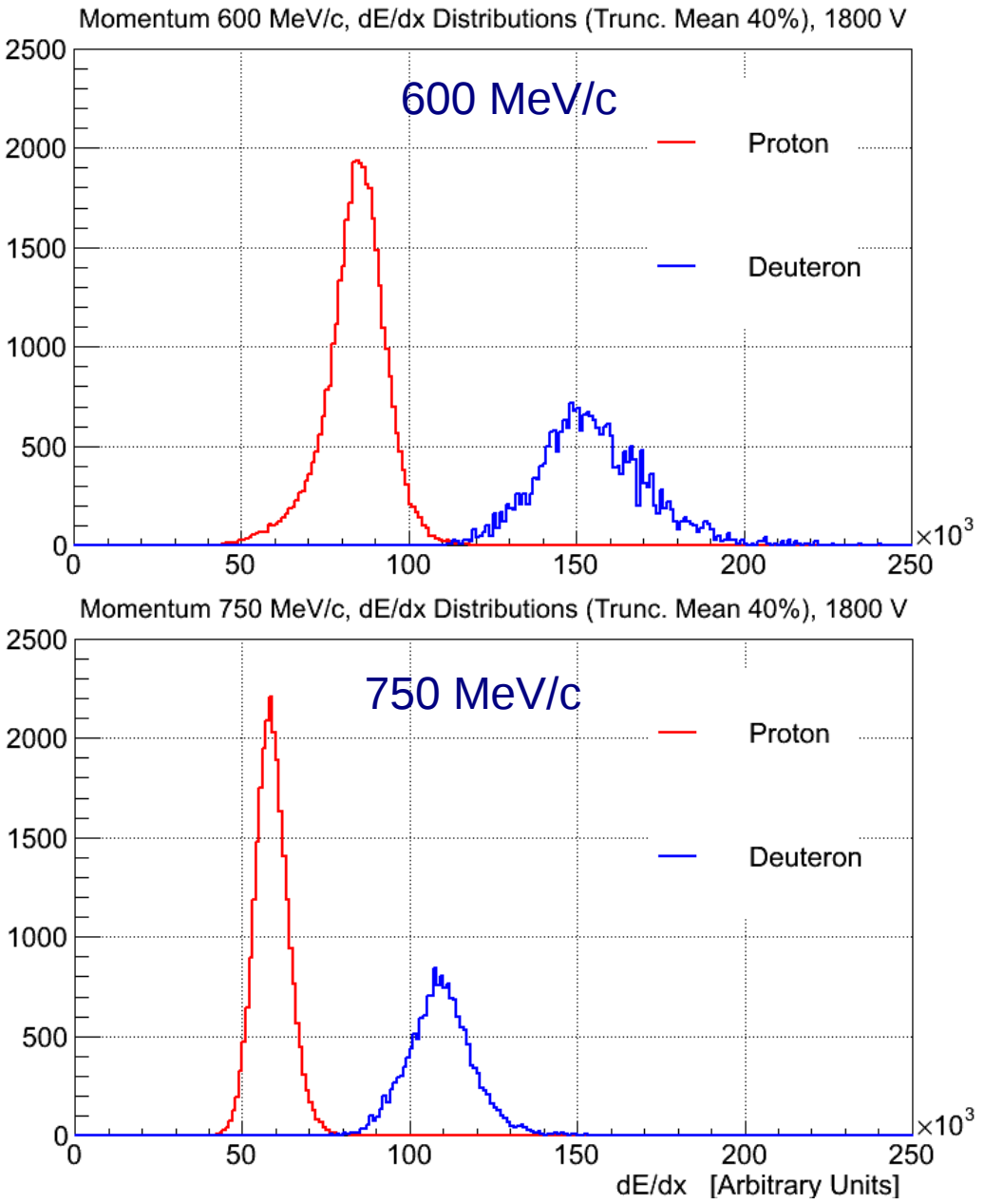

For the energy resolution the Truncation Mean of 40 % applied to initial dE/dx distributions

Results for deuterons are charged with bigger uncertainties



# dE/dx for proton and deuteron

Clear separation between protons and deuterons at 600- and 750 MeV/c



# Manpower – contributing persons

**Susanna Costanza** *(INFN Pavia)*
**Jacek Biernat** *(AGH, UJ Kraków)*
**Andreas Erven** *(Forschungszentrum Jülich, ZEA)*
**Wilhelm Erven** *(Forschungszentrum Jülich, ZEA)*
**Tanja Hahnraths - von der Gracht** *(Forschungszentrum Jülich, IKP)*
**Lioubov Jokhovets** *(Forschungszentrum Jülich, ZEA)*
**Paweł Kulessa** *(IFJ PAN Kraków)*
**Emeline Lesmanne** *(Forschungszentrum Jülich, IKP)*
**Jerzy Mejewski** *(Forschungszentrum Jülich, IKP, Kraków)*
**Marius Mertens** *(Forschungszentrum Jülich, IKP)*
**Robert Nellen** *(Forschungszentrum Jülich, IKP)*
**Henner Ohm** *(Forschungszentrum Jülich, IKP)*
**Timm Preuhs** *(Forschungszentrum Jülich, IKP)*
**Krzysztof Pysz** *(IFJ PAN Kraków)*
**James Ritman** *(Forschungszentrum Jülich, IKP)*
**Thomas Sefzick** *(Forschungszentrum Jülich, IKP)*
**Valery Serdyuk** *(Forschungszentrum Jülich, IKP)*
**Peter Wintz** *(Forschungszentrum Jülich, IKP)*
**Bogusław Włoch** *(IFJ PAN Kraków / AGH Kraków)*
**Peter Wuestner** *(Forschungszentrum Jülich, ZEA)*
**Solmaz Vejdani** *(Forschungszentrum Jülich, IKP, Univ. of Groningen)*

# Manpower – current situation

| | |
|---|---|
| **Susanna Costanza** *(INFN Pavia)* | |
| **Jacek Biernat** *(AGH, UJ Kraków)* | |
| **Andreas Erven** *(Forschungszentrum Jülich, ZEA)* | |
| **Wilhelm Erven** *(Forschungszentrum Jülich, ZEA)* | |
| **Tanja Hahnraths - von der Gracht** *(Forschungszentrum Jülich, IKP)* | |
| **Lioubov Jokhovets** *(Forschungszentrum Jülich, ZEA)* | |
| **Paweł Kulessa** *(IFJ PAN Kraków)* | *20 %* |
| **Emeline Lesmanne** *(Forschungszentrum Jülich, IKP)* | |
| **Jerzy Mejewski** *(Forschungszentrum Jülich, IKP, Kraków)* | |
| **Marius Mertens** *(Forschungszentrum Jülich, IKP)* | |
| **Robert Nellen** *(Forschungszentrum Jülich, IKP)* | |
| **Henner Ohm** *(Forschungszentrum Jülich, IKP)* | |
| **Timm Preuhs** *(Forschungszentrum Jülich, IKP)* | |
| **Krzysztof Pysz** *(IFJ PAN Kraków)* | *20 %* |
| **James Ritman** *(Forschungszentrum Jülich, IKP)* | |
| **Thomas Sefzick** *(Forschungszentrum Jülich, IKP)* | |
| **Valery Serdyuk** *(Forschungszentrum Jülich, IKP)* | |
| **Peter Wintz** *(Forschungszentrum Jülich, IKP)* | |
| **Bogusław Włoch** *(IFJ PAN Kraków / AGH Kraków)* | |
| **Peter Wuestner** *(Forschungszentrum Jülich, ZEA)* | |
| **Solmaz Vejdani** *(Forschungszentrum Jülich, IKP, Univ. of Groningen)* | *PhD student* |

# Summary

- Number of laboratory and beam tests were performed with the use of Front End Electronics Free readout system of PANDA type STT prototype consisting of passive board at the detector housing, 12 m long coaxial signal/HV cable, low noise preamplifier and 240 MHz flashADC.
- Signal shape analysis procedures have been developed and are confirmed.
- Experimentally obtained spatial resolution of <160 μm and energy resolution of about 9 % fulfill the demands defined for PANDA STT detector.
- Feasibility of the readout method based on STT signal sampling with fast ADC and pulse shape analysis oriented for time and energy loss information has been proved.
- Feasibility of the analog readout without active electronics at the detector side but utilizing carefully shielded coaxial signal/HV cables and low noise preamplifier has been proved.
- The general idea of the architecture of the readout and signal processing system for PANDA STT has been defined.

# Summary

- Development of the analog part of the readout (cables, shielding, coupling boards) is ongoing (Electronics Workshop of IKP).
- Development of proper preamplifier and its integration into ADC board is ongoing (ZEA-2 + EW IKP).
- The work on highly integrated multichannel sampling ADC coupled with fast FPGA modules for real time signal shape analysis is ongoing (ZEA-2).
- Manpower has been reduced in recent 2 years.

The success of the project in respect to the prove of its final performance as well as regarding the time limits currently depends on the further progress of the work on digital part of the readout system and available manpower for system integration and test.