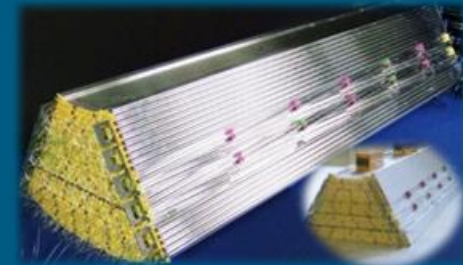


ASIC/TRB Readout Status in Jülich

Peter Wintz (IKP, FZ Jülich)

STT RO WShop, Krakow, Jan-30/31 2016



Outline: ASIC/TRB Readout Status in Jül

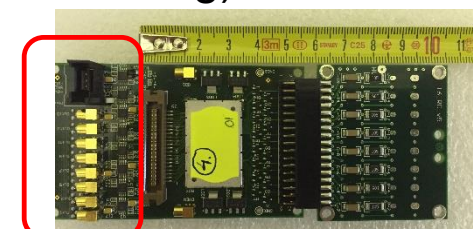
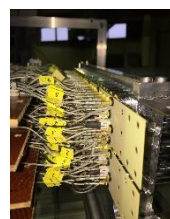
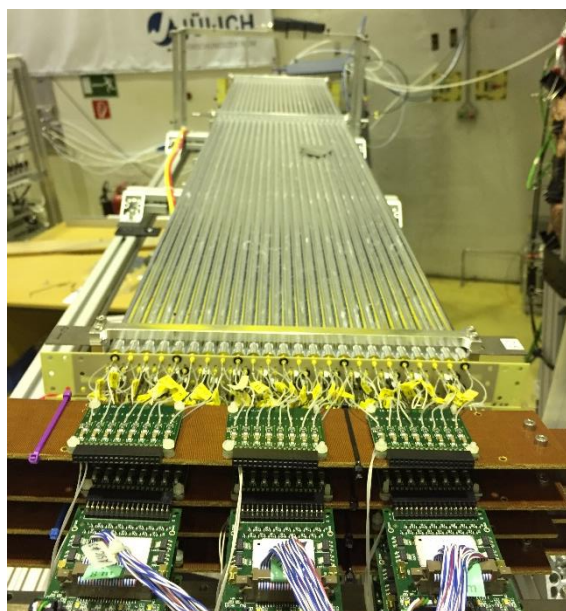
- WPs in Jülich
- System overview
- Production status
- Readout status
- Next steps

WPs with ASIC/TRB System in Jülich

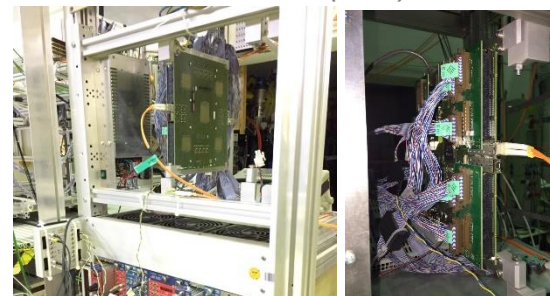
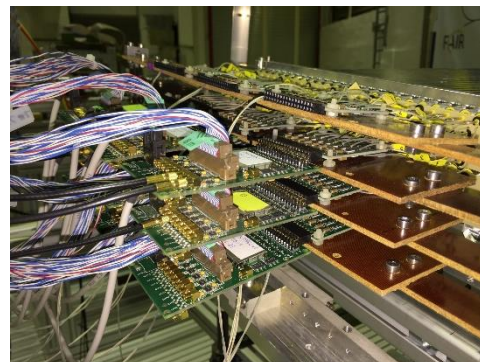
- WP1: straw & readout system for in-beam tests
 - ~ 400ch straw & readout system for in-beam tests
 - High beam intensities (i.p. spikes) and high gas gain can cause aging, straws not for later use in PANDA-STT
 - Readout tests: ASIC props, TRB-DAQ
 - Data analysis, calibration procedures, .. PID methods
 - Mechanical STT design: alignment & precision, position calibration → next: WP2
- WP2: STT “pre-series” system
 - One STT sector with ~700 straws in prototype mechanical frame (by Frascati)
 - Set up readout system with full electronics chain for 700 ch
 - Workout mechanical layout of front-end part (challenging space, cooling)
 - Test mechanical precision of sector with cosmic data, not in-beam
 - Straws and modules can be used later in PANDA-STT, final geometry
- MP: ~ 1.2 FTE (Jül) + Krakow

ASIC/TRB Readout System in Jülich

- Set up readout system with ~700 channels
 - FE-boards with PASTTREC-ASIC (2x8ch), addit. analog out (cut in final layout)
 - LVDS for 16ch out + ASIC ctrl (0.5mm micro TW pair), LV power supply (5V)
 - TRB3 (TDC in FPGA) readout, ~256ch boards, central FPGA for ASIC control
 - DAQ: system (CTS) with online monitoring, online spectra by Go4Analyzer
- System installations done by AGH & JU Krakow (Pawel, Greg)



FE-board with 2xASIC, HV board. Addit. out (box)



Straw test system and front-end electronics.

Connected TRB board in crate.

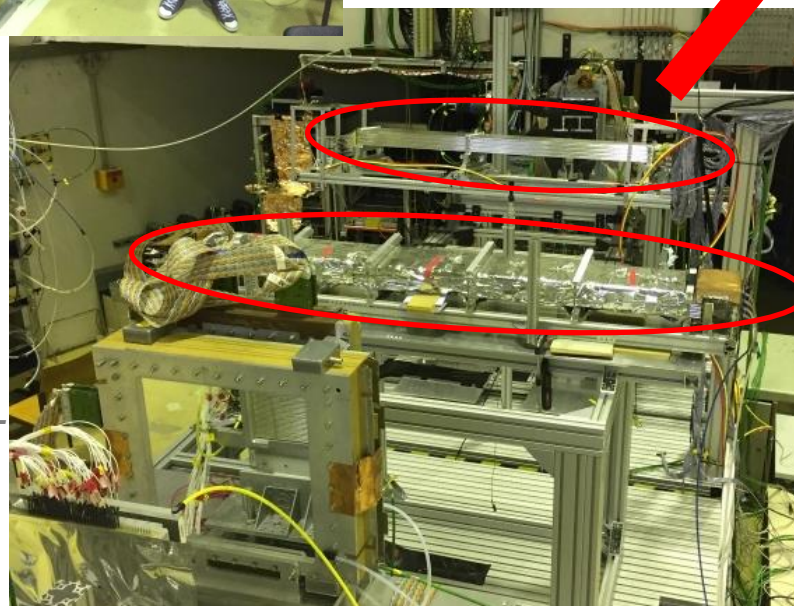
New Beam Area (since 2016)



Test setups in new experimental area (April 2016)



Straw test system for the ASIC/TRB readout. Beam from the right.



2× Straw test systems (red circles) for the ADC-based and ASIC/TRB readout. Beam from the back.

Readout DAQ & Control System

(by AGH & JU Krakow)

- Central trigger system (CTS, GSI) for DAQ, external or channel trigger
- TDC registers, channel count rates monitor (ex. below, 6mV, no HV, 10sec)
- ASIC control (BL, thr., gain, PkT, TC, shaping ..)
- Power cycle (ASIC/TRB on/off) by ethernet powerline
- Remote-scope with monitor channels
- Go4analyzer for online data spectra
- All data files in Root format



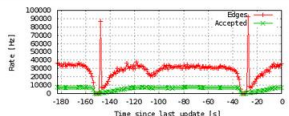
Central Trigger System

- Status overview

Counter	Counts	Rate
Trigger asserted	21776965 cks.	31.19 Kcnt/s
Trigger rising edges	21776965 edges	31.19 KHz
Trigger accepted	28903901 events	7.01 KHz

Last Idle Time: 232340 ns
 Last Dead Time: 3540 ns
 Total Dead Time: 27489893 ns (2.7%)

Throttle: Limit Trigger Rate to 10 KHz
 Full Stop: Ignore all events

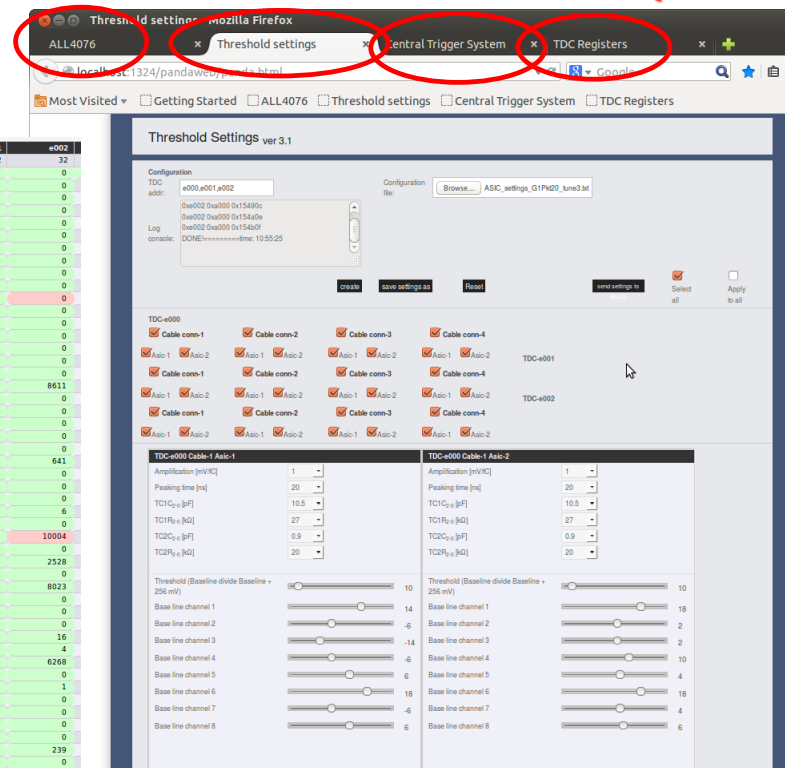


Export CTS Configuration as TrbCmd script or as shell script

- Trigger Channels

#	Enable	Trg. Cond.	Assignment	TrbNet Type	Asserted	Edges
0	<input type="checkbox"/>	R. Edge	Periodical Pulser 0	0x1_physics_trigger	0.00 cnt/s	0.00 Hz
1	<input type="checkbox"/>	R. Edge	Periodical Pulser 1	0x1_physics_trigger	25.00 cnt/s	25.00 MHz
2	<input type="checkbox"/>	R. Edge	Random Pulser 0	0x1_physics_trigger	0.00 cnt/s	0.00 Hz
3	<input type="checkbox"/>	R. Edge	AddOn Multiplexer 0	0x1_physics_trigger	100.00 cnt/s	0.00 Hz
4	<input type="checkbox"/>	R. Edge	AddOn Multiplexer 1	0x1_physics_trigger	438.02 cnt/s	438.02 Hz
5	<input checked="" type="checkbox"/>	R. Edge	AddOn Multiplexer 2	0x1_physics_trigger	99.85 cnt/s	31.17 KHz

Reg	Channel	e#000	e#001	e#002
c#000	0	32	32	32
e#001	1	475	4	0
e#002	2	0	0	0
e#003	3	0	0	0
e#004	4	0	0	0
e#005	5	0	0	0
e#006	6	0	0	0
e#007	7	0	0	0
e#008	8	0	0	0
e#009	9	0	0	0
e#00a	10	0	0	0
e#00b	11	0	0	0
e#00c	12	0	0	0
e#00d	13	0	0	0
e#00e	14	0	0	0
e#00f	15	0	0	0
e#010	16	0	0	0
e#011	17	0	0	0
e#012	18	0	0	8611
e#013	19	0	0	0
e#014	20	0	0	0
e#015	21	0	0	0
e#016	22	0	0	0
e#017	23	0	0	0
e#018	24	0	0	641
e#019	25	0	0	0
e#01a	26	0	0	0
e#01b	27	0	0	0
e#01c	28	0	0	6
e#01d	29	0	0	0
e#01e	30	0	0	10004
e#01f	31	0	0	0
e#020	32	0	0	2528
e#021	33	0	0	0
e#022	34	0	0	8023
e#023	35	0	0	0
e#024	36	0	0	0
e#025	37	0	0	0
e#026	38	0	0	16
e#027	39	67	4	4
e#028	40	0	0	6268
e#029	41	0	0	0
e#02a	42	0	0	0
e#02b	43	0	0	0
e#02c	44	31	0	0
e#02d	45	0	0	0
e#02e	46	0	0	0
e#02f	47	0	67	239
e#030	48	0	5	0



Threshold Settings ver 3.1

Configuration: TDC addr: e#000:e001:e002

Log console: DONE!=====time: 10:55:25

TDC-e000

Cable conn-1	Cable conn-2	Cable conn-3	Cable conn-4
<input checked="" type="checkbox"/> Asc-1	<input checked="" type="checkbox"/> Asc-2	<input checked="" type="checkbox"/> Asc-1	<input checked="" type="checkbox"/> Asc-2
<input checked="" type="checkbox"/> Asc-1	<input checked="" type="checkbox"/> Asc-2	<input checked="" type="checkbox"/> Asc-1	<input checked="" type="checkbox"/> Asc-2
<input checked="" type="checkbox"/> Asc-1	<input checked="" type="checkbox"/> Asc-2	<input checked="" type="checkbox"/> Asc-1	<input checked="" type="checkbox"/> Asc-2

TDC-e001

Cable conn-1	Cable conn-2	Cable conn-3	Cable conn-4
<input checked="" type="checkbox"/> Asc-1	<input checked="" type="checkbox"/> Asc-2	<input checked="" type="checkbox"/> Asc-1	<input checked="" type="checkbox"/> Asc-2
<input checked="" type="checkbox"/> Asc-1	<input checked="" type="checkbox"/> Asc-2	<input checked="" type="checkbox"/> Asc-1	<input checked="" type="checkbox"/> Asc-2
<input checked="" type="checkbox"/> Asc-1	<input checked="" type="checkbox"/> Asc-2	<input checked="" type="checkbox"/> Asc-1	<input checked="" type="checkbox"/> Asc-2

TDC-e002

Cable conn-1	Cable conn-2	Cable conn-3	Cable conn-4
<input checked="" type="checkbox"/> Asc-1	<input checked="" type="checkbox"/> Asc-2	<input checked="" type="checkbox"/> Asc-1	<input checked="" type="checkbox"/> Asc-2
<input checked="" type="checkbox"/> Asc-1	<input checked="" type="checkbox"/> Asc-2	<input checked="" type="checkbox"/> Asc-1	<input checked="" type="checkbox"/> Asc-2
<input checked="" type="checkbox"/> Asc-1	<input checked="" type="checkbox"/> Asc-2	<input checked="" type="checkbox"/> Asc-1	<input checked="" type="checkbox"/> Asc-2

TDC-e#000 Cable-1 Asc-1

Amplification [mV]	Peaking time [ns]	TC1C ₀ [pF]	TC1R ₀ [kΩ]	TC2C ₀ [pF]	TC2R ₀ [kΩ]
1	20	10.5	27	0.9	20

TDC-e#000 Cable-1 Asc-2

Amplification [mV]	Peaking time [ns]	TC1C ₀ [pF]	TC1R ₀ [kΩ]	TC2C ₀ [pF]	TC2R ₀ [kΩ]
1	20	10.5	27	0.9	20

Threshold (Baseline divide Baseline + 256 mV)

Base line channel 1: 10, 14, 2, 2, 10, 4, 18, 6, 4, 18, 4, 6

Production Status

- PASTTRECv1 - ASIC
 - design and tests by AGH, chip production by Fraunhofer (ams techn.)
 - at first manual bonding (AGH), later automatic bonding done by company
 - in total: ~ 150 chips
- FE-boards
 - design by JU / company
 - production by companies
 - 2nd version with slight re-design: volt layer structure, connectors
 - some bad manufacturer quality observed, req. some manual re-bonding (at AGH)
 - in total: ~ 75 boards (soon) available
- TRB3-DAQ system
 - 10x boards available (from GSI), FPGA set up by JU Krakow
- Full production chain executed (~ 1 year)
- Complete costbook for all manufacturing steps existing (at Peter's desk)
 - Manufacturing companies / groups identified, next: re-define QA criteria for them

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 - 10x boards available (from GSI), FPGA set up by JU Krakow
- Full production chain executed (~ 1 year) **in 2015 (remind PANDA situation!)**
- Complete costbook for all manufacturing steps existing (at Peter's desk)
 - Manufacturing companies / groups identified, next: re-define QA criteria for them

Readout Operation Status

- TRB3-DAQ
 - In running or standby mode since Apr-2016 beam time, cosmic runs in 2017
 - ASIC ctrl by FPGA reliable (but slow), TDC calibration procedure defined
 - Stable operation in 2 weeks beam time (trigger limit necess.)
 - Low & stable min. thresh. ~10mV since > 6months, NL ~ 5mV for 144+ ch system
- PASTTRECv1-ASIC
 - Robust operation, low NL, no ringing (compare ASD8, Carioca)
 - ASIC parameters seems ok (range of gain, pkt, BL, TC, shaping, ..)
 - No saturation seen for deuteron beam @ 600 MeV/c and dE/dx ~ 50 keV/cm
 - No indication for 2nd thresh necessity from data results for resolution (low+high thr)
 - **At current: I see no need for an ASIC re-design (v2)**
- FE-boards
 - Some re-design for final version (space optimisation), HV boards now 2-sided
 - No EM shielding needed (was prepared), RF-pickup thru HV line identified & cured

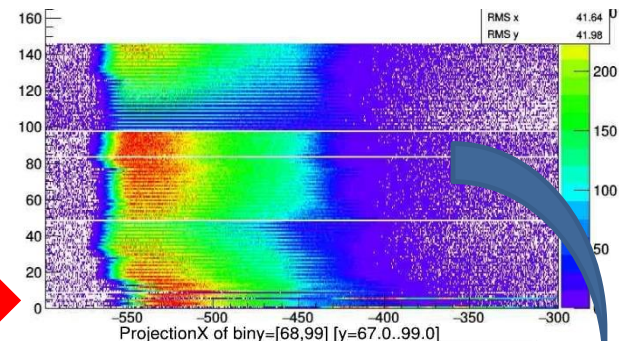
ASIC/TRB – Readout Status

(Raw Spectra from April 2016 Beam Time)

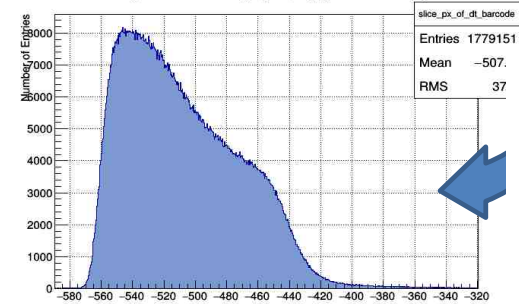


In-beam position of straw setup with FE-ASIC boards (beam from the right)

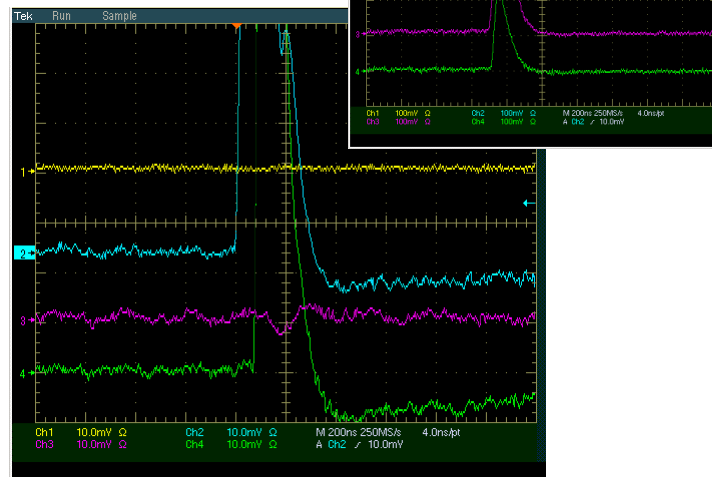
FEB replaced later (ch1-16)



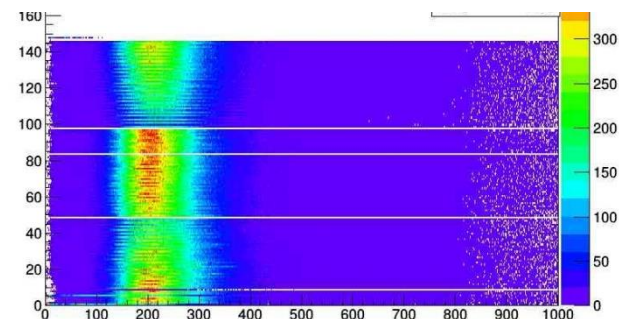
beam spot area



ASIC analog output signals (in-beam), NL <5mV (stable), min. thresh. at 10mV

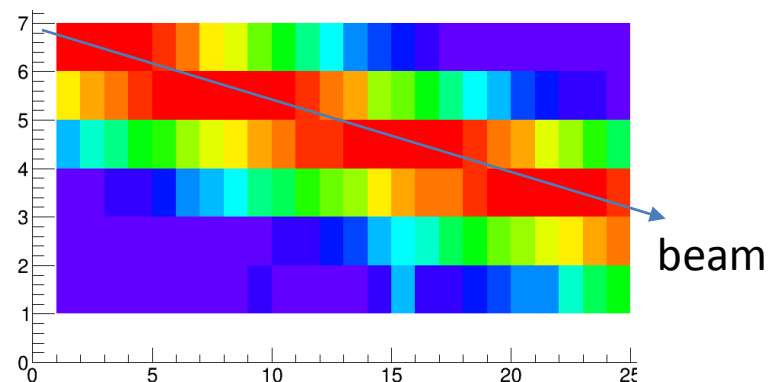
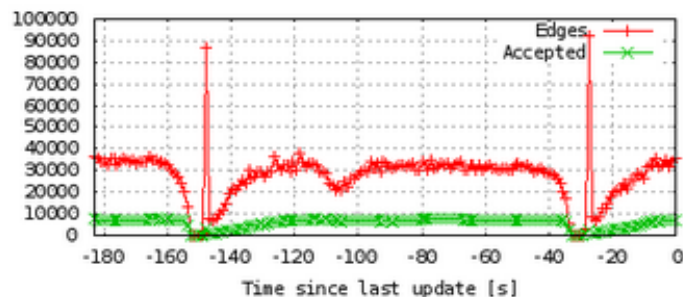


TDC time (top) and time-over-threshold (below) vs channel

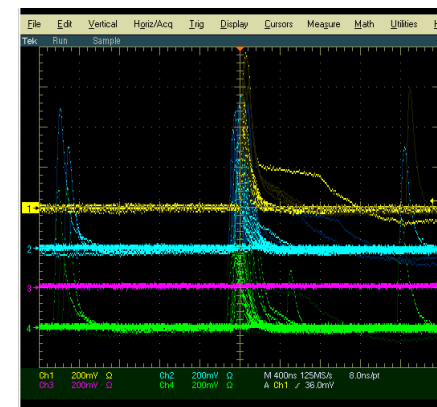
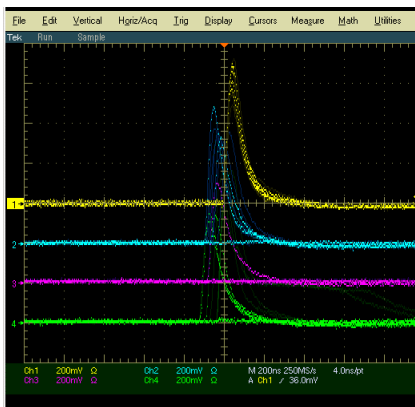


Status Beamtime Dec 2016

- TRB3-DAQ, cts rate for 1.5 GeV/c beam, trigger (red), readout rate (green)
- COSY beam extraction cycle 2min (spike intensities on detectors)
- Hitmap (6x24 straws), $\sim 2 \times 2 \text{ cm}^2$ spot

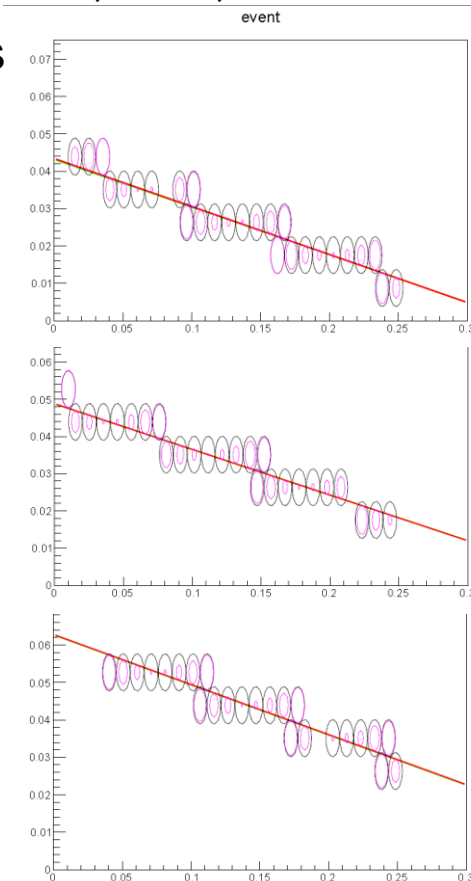


- 600 MeV/c deuteron beam
- $dE/dx > 8 \times \text{MIPS}$, $\sim 50 \text{ keV/cm}$
- FE-ASIC analog outs on scope

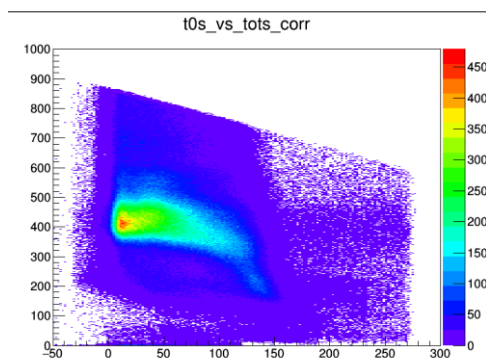


2016' Beam Test Data

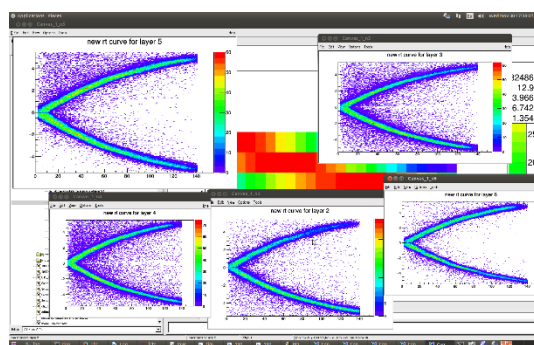
- 2x1 weeks, proton @ 3, 1, 0.75, 0.55 GeV/c, deuteron @ 1.5, 0.75, 0.6 GeV/c
- Test of signal dynamical range by 600 MeV/c deuterons
 - dE/dx ~ 50 keV/cm, consider as our dE/dx range limit
 - dE/dx-range: ~ 1-10x mips @ 2bar
 - MScatt: $\theta_0 \sim O(1\text{mrad}/\text{straw}) \sim 10\mu\text{m}/\text{straw}$
 - Spatial resolution spoiled by MS. (\propto no. hits/track)
- No saturation effects seen for ASIC (amp, TC, ..)
- Analysis ongoing (snapshots for 600 MeV/c deuterons)



Reconstructed tracks.
Some cuts applied
(50% min. eff., time cuts ..)



ToT vs time (ns) for 600 MeV/c deuterons. No saturation seen



Isochrone $r(t)$ curves for 5 layers in beam spot

Status and Next Steps (HW)

- DAQ operation:
 - Readout system with clean and stable operation: > 6 months, 144 ch
 - Leave in running mode, further cosmic runs in 2017
 - Add more straw channels (~ 300 ch)
 - Study (current) trigger limit for DAQ operation (TRB3 design: ~ 300 kHz)
- Front-end:
 - No ASIC design iteration necessary (based on current test data)
 - Workout of STT front-end layout ongoing (space, cooling reqmts)
 - FE board slight re-designs for final version (space, cut analog out)
- TRB-system
 - TRB3-DAQ bandwidth sufficient for PANDA starting phase (lower lumi)
 - New TRB design necess. for full lumi (TRB general PANDA/GSI project)

Status and Next Steps (SW)

- Data analysis (in-beam tests)
 - Analysis of beam test data ongoing in 2017 (lacking man power)
 - Prelim. resolutions (time, space, ToT) spoiled, corrections poss.& ongoing
 - ToT methods ongoing, dE/dx separation by ToT/dx, ToT_{corr}
 - ToT - dE (charge) calibration study (wishful for simulation)
 - ..
 - Absolute straw timing and pattern recognition studies
- Very important: readout is used for overall STT system test (urgently needed)
 - Measured possible straw (mis)alignment, tube-wire displacement (“2-leg”)
 - Method developed to check straw positions by data & re-align straws
 - Found: robust & efficient operation of straws in-beam even if misaligned
- Reminder: general failure tests required for all system components

Thank you

for your

attention

WPs: ASIC/TRB Readout System

- Readout of drift time and dE/dx for PID by time-over-threshold
- Pre-series system ready: PASTTRECv1-ASIC, FEB & TRB3 readout
- Preps done for beam test, few ASIC sets def. (progr. combs: 16x, PkT-G , 4100x TC)
- Option: 2nd ASIC version with 2-threshs for better ToT by end 2016
- TRB3 – PANDA DAQ integration ongoing (BW limit, Buffsize), for low lumi ok
- TRB new HW required (?) for full lumi (1.5 GB/s data rate per TRB)
- ToDo: cooling concept (~120 W)

ASIC design by AGH

PASTTREC: A new 8 channels ASIC for STT & FT

Layout – 1.95 × 2.6 mm²

Improvements

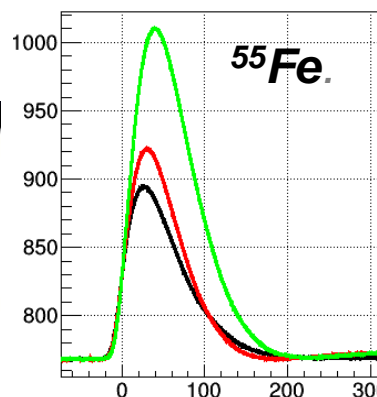
- New faster amplifiers
- Redesigned BLH circuit: Baseline dispersion below 35 mV_{p-p}
- 5 bit DACs added to trimm baseline (2 mV accuracy)

Performance

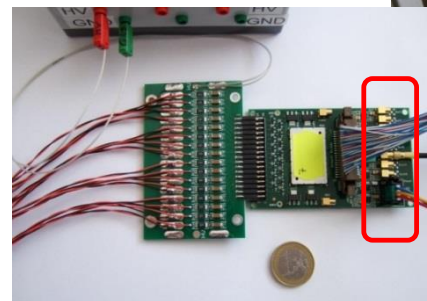
- Total power 34.2 mW/ch
- Gain in range of 1 to 7 mV/fC
- T_{peak} of ~17, ~23, ~39 and ~64 ns
- ENC below 3000 e⁻ for highest gain and 25 pF of C_{in}

Dominik Przyborowski PASTTREC: A New 8-channel ASIC for STT & FT

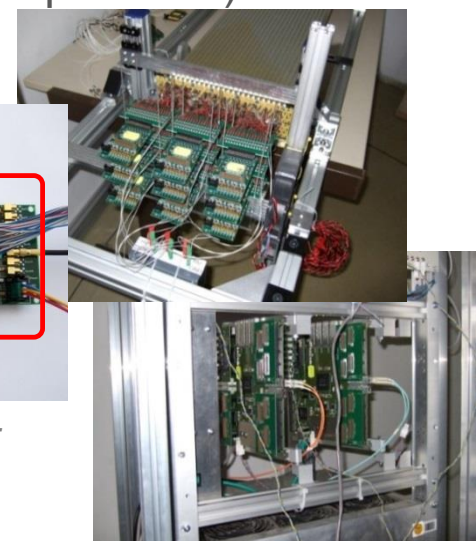
PASTTREC parameters



Straw signals (mV) for diff. ASIC sets.



HV coupling and FE-board with 2x ASIC.



FEBs at test system (top) and TRB3 readout (lower)

dE/dx (Charge) – ToT Calibration

- ASIC/TRB prototype data (red dots, left y-axis)
 - Time-over-threshold \leftrightarrow charge calibration (by ^{55}Fe here, later with proton beam)
 - Only 12 hits/track \rightarrow 10% truncation only
 - FADC prototype data (blue dots & axis)
 - 16 hits/track, up to 40% truncation best
 - Clear dE/dx sensitivity seen for both
 - Reminder: dE/dx min \sim 5 keV/cm
- @ 2bar Ar/CO₂(10%)

