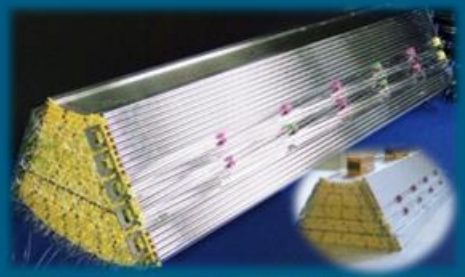
ASIC/TRB Readout Status in Jülich

Peter Wintz (IKP, FZ Jülich)

STT RO WShop, Krakow, Jan-30/31 2016



Outline: ASIC/TRB Readout Status in Jül

- WPs in Jülich
- System overview
- Production status
- Readout status
- Next steps

WPs with ASIC/TRB System in Jülich

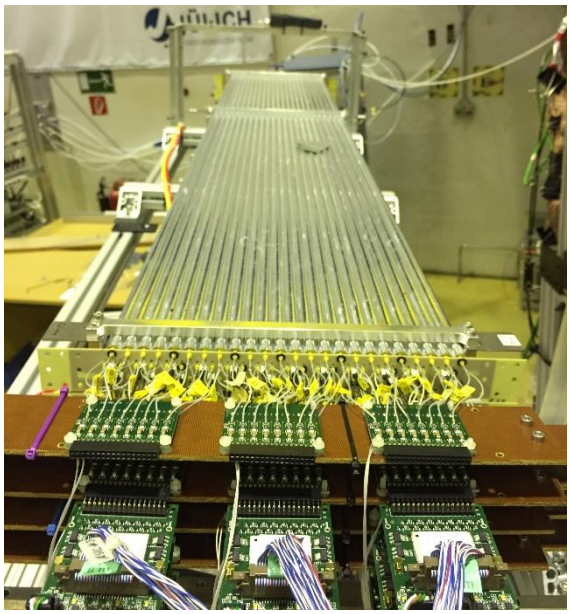
- WP1: straw & readout system for in-beam tests
  - ~ 400ch straw & readout system for in-beam tests
  - High beam intensities (i.p. spikes) and high gas gain can cause aging, straws not for later use in PANDA-STT
  - Readout tests: ASIC props, TRB-DAQ
  - Data analysis, calibration procedures, .. PID methods
  - Mechanical STT design: alignment & precision, position calibration → next: WP2

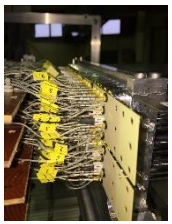
- WP2: STT “pre-series” system
  - One STT sector with ~700 straws in prototype mechanical frame (by Frascati)
  - Set up readout system with full electronics chain for 700 ch
  - Workout mechanical layout of front-end part (challenging space, cooling)
  - Test mechanical precision of sector with cosmic data, not in-beam
  - Straws and modules can be used later in PANDA-STT, final geometry

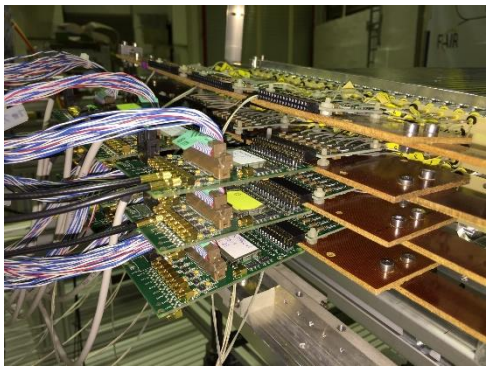
- MP: ~ 1.2 FTE (Jül) + Krakow

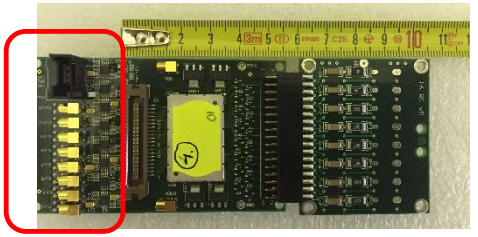
ASIC/TRB Readout System in Jülich

- Set up readout system with ~700 channels
  - FE-boards with PASTTREC-ASIC (2x8ch), addit. analog out (cut in final layout)
    - LVDS for 16ch out + ASIC ctrl (0.5mm micro TW pair), LV power supply (5V)
  - TRB3 (TDC in FPGA) readout, ~256ch boards, central FPGA for ASIC control
  - DAQ: system (CTS) with online monitoring, online spectra by Go4Analyzer
- System installations done by AGH & JU Krakow (Pawel, Greg)









FE-board with 2xASIC, HV board. Addit. out (box)

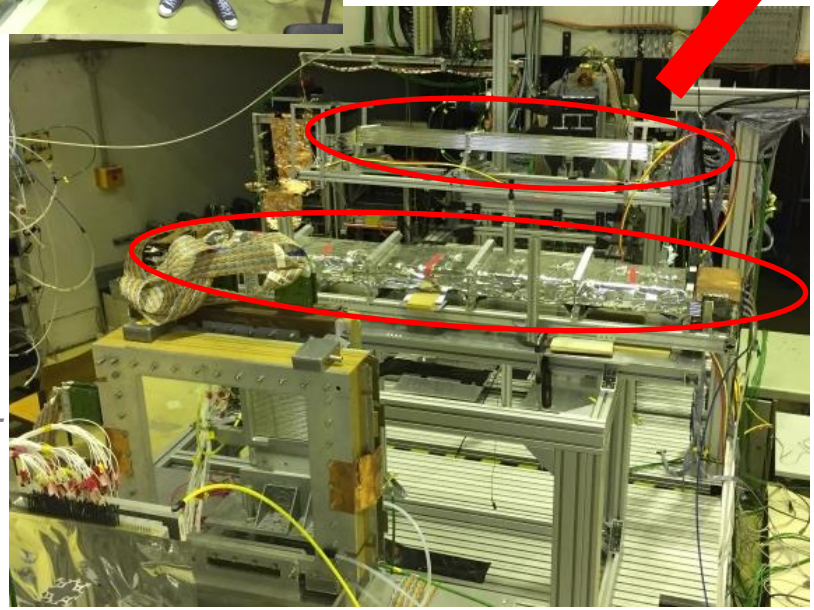
Straw test system and front-end electronics.

Connected TRB board in crate.

New Beam Area (since 2016)

Test setups in new experimental area (April 2016)

Straw test system for the ASIC/TRB readout. Beam from the right.



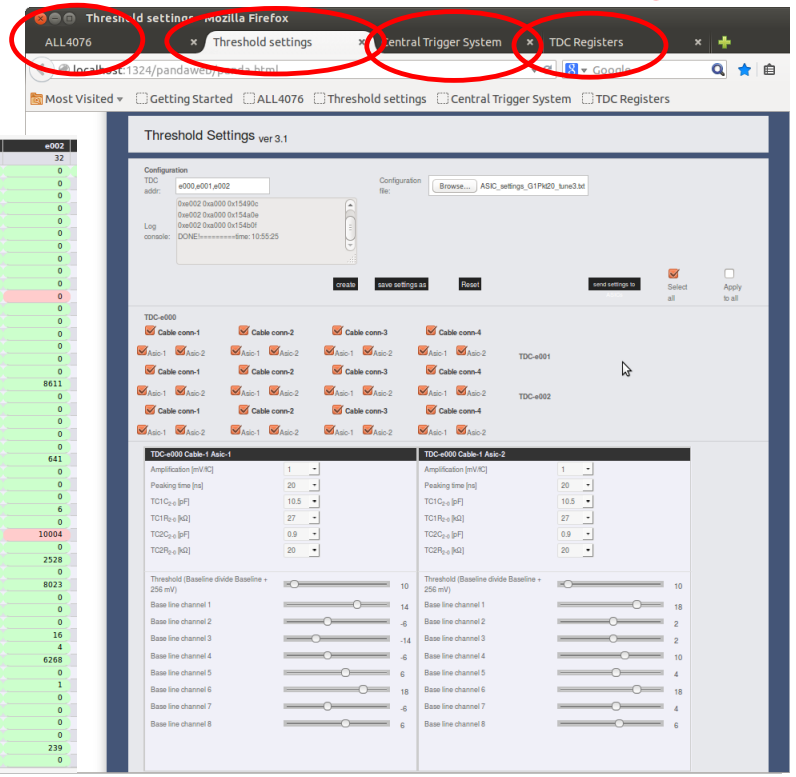
2× Straw test systems (red circles) for the ADC-based and ASIC/TRB readout. Beam from the back.

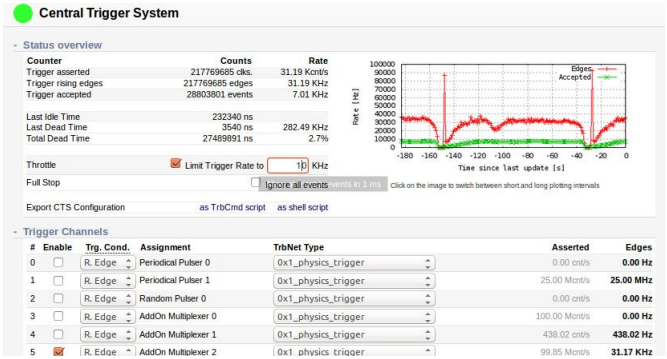
Readout DAQ & Control System

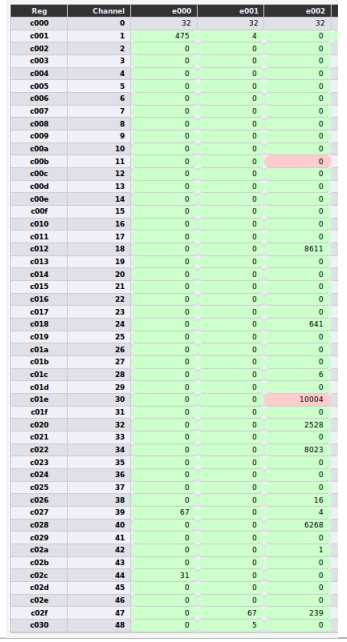
(by AGH & JU Krakow)

- Central trigger system (CTS, GSI) for DAQ, external or channel trigger
- TDC registers, channel count rates monitor (ex. below, 6mV, no HV, 10sec)
- ASIC control (BL, thr., gain, PkT, TC, shaping ..)
- Power cycle (ASIC/TRB on/off) by ethernet powerline
- Remote-scope with monitor channels
- Go4analyzer for online data spectra
- All data files in Root format

htm scripts







Production Status

- PASTTRECv1 - ASIC
  - design and tests by AGH, chip production by Fraunhofer (ams techn.)
  - at first manual bonding (AGH), later automatic bonding done by company
  - in total: ~ 150 chips
- FE-boards
  - design by JU / company
  - production by companies
  - 2nd version with slight re-design: volt layer structure, connectors
  - some bad manufacturer quality observed, req. some manual re-bonding (at AGH)
  - in total: ~ 75 boards (soon) available
- TRB3-DAQ system
  - 10x boards available (from GSI), FPGA set up by JU Krakow

- Full production chain executed (~ 1 year)
- Complete costbook for all manufacturing steps existing (at Peter's desk)
  - Manufacturing companies / groups identified, next: re-define QA criteria for them

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- Full production chain executed (~ 1 year) **in 2015 (remind PANDA situation!)**
- Complete costbook for all manufacturing steps existing (at Peter's desk)
  - Manufacturing companies / groups identified, next: re-define QA criteria for them

Readout Operation Status

- TRB3-DAQ
  - In running or standby mode since Apr-2016 beam time, cosmic runs in 2017
  - ASIC ctrl by FPGA reliable (but slow), TDC calibration procedure defined
  - Stable operation in 2 weeks beam time (trigger limit necess.)
  - Low & stable min. thresh. ~10mV since > 6months, NL ~ 5mV for 144+ ch system

- PASTTRECv1-ASIC
  - Robust operation, low NL, no ringing (compare ASD8, Carioca)
  - ASIC parameters seems ok (range of gain, pkt, BL, TC, shaping, ..)
  - No saturation seen for deuteron beam @ 600 MeV/c and dE/dx ~ 50 keV/cm
  - No indication for 2nd thresh necessity from data results for resolution (low+high thr)
  - **At current: I see no need for an ASIC re-design (v2)**

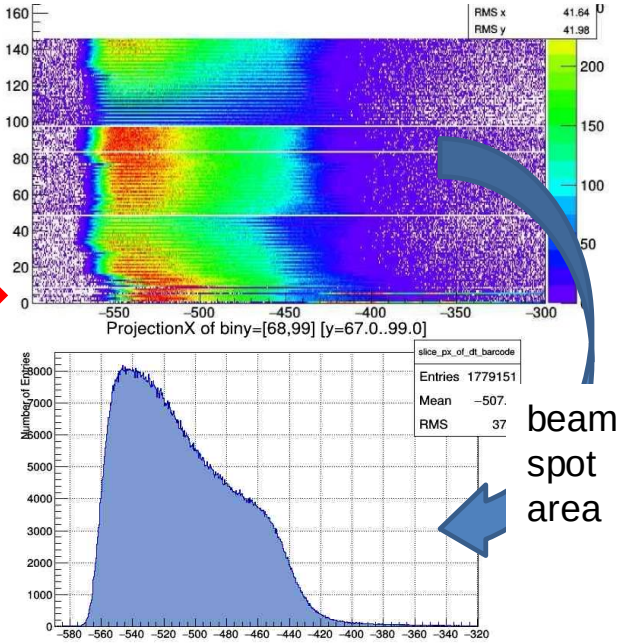
- FE-boards
  - Some re-design for final version (space optimisation), HV boards now 2-sided
- No EM shielding needed (was prepared), RF-pickup thru HV line identified & cured

ASIC/TRB – Readout Status

(Raw Spectra from April 2016 Beam Time)

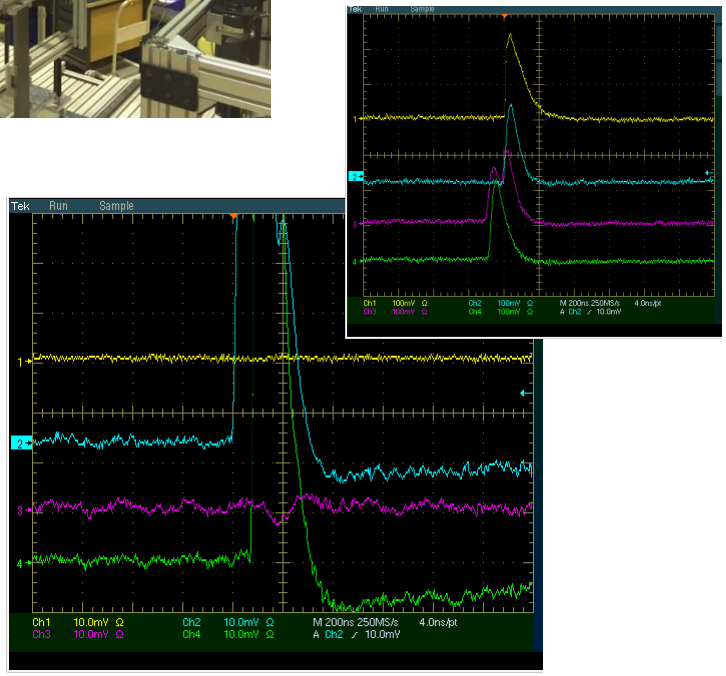
In-beam position of straw setup with FE-ASIC boards (beam from the right)

FEB replaced later (ch1-16)

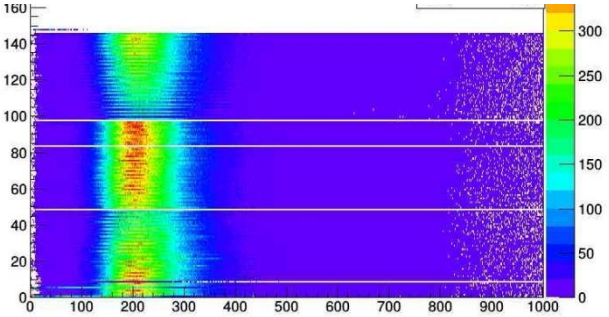


beam spot area

ASIC analog output signals (in-beam), NL <5mV (stable), min. thresh. at 10mV

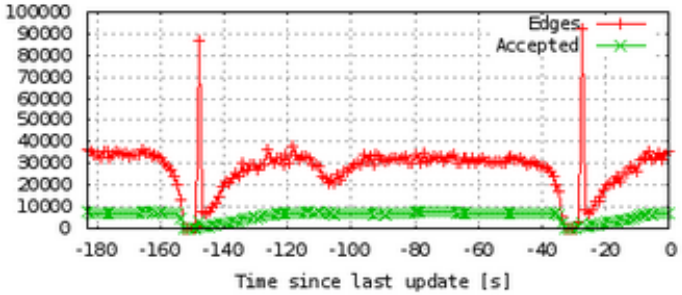


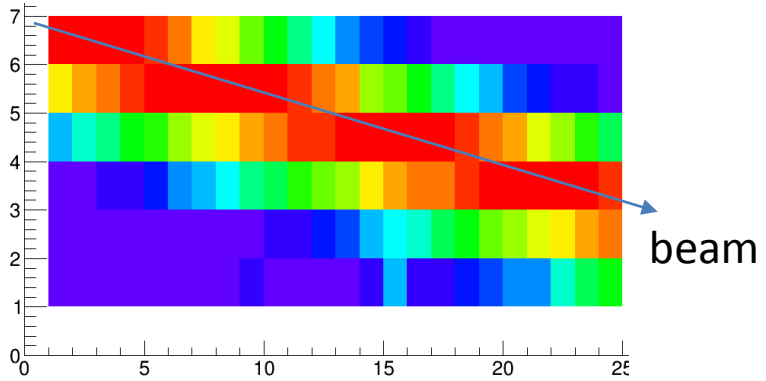
TDC time (top) and time-over-threshold (below) vs channel



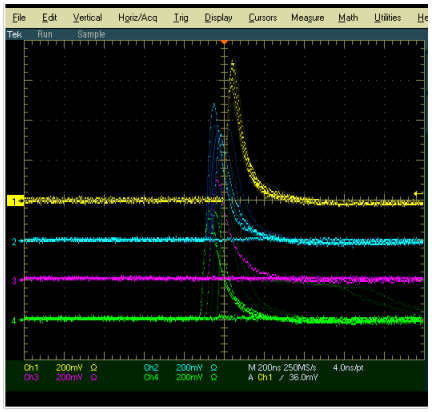
Status Beamtime Dec 2016

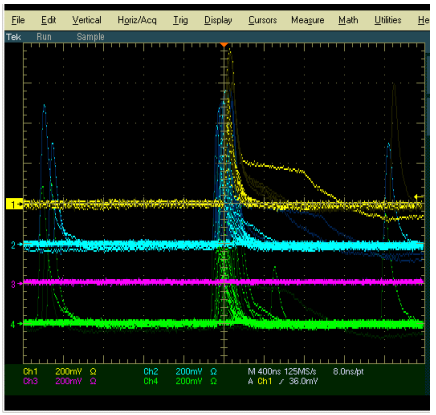
- TRB3-DAQ, cts rate for 1.5 GeV/c beam, trigger (red), readout rate (green)
- COSY beam extraction cycle 2min (spike intensities on detectors)
- Hitmap (6x24 straws), ~ 2x2 cm^2 spot





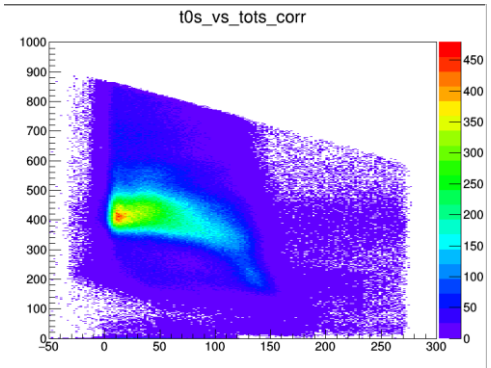
- 600 MeV/c deuteron beam
- dE/dx > 8x MIPS, ~ 50 keV/cm
- FE-ASIC analog outs on scope



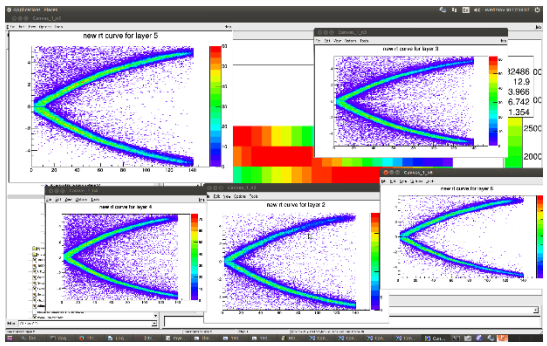


2016´ Beam Test Data

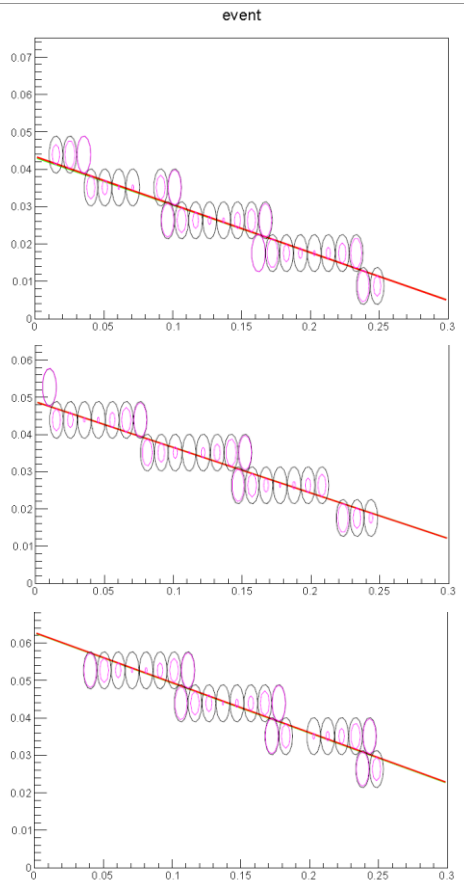
- 2x1 weeks, proton@ 3, 1, 0.75, 0.55 GeV/c, deuteron@ 1.5, 0.75,0.6 GeV/c
- Test of signal dynamical range by 600 MeV/c deuterons
  - dE/dx ~ 50 keV/cm, consider as our dE/dx range limit
  - dE/dx-range: ~ 1-10x mips @ 2bar
  - MScatt: θ_0 ~ O(1mrad/straw) ~ 10µm/straw
  - Spatial resolution spoiled by MS. ($\propto$ no. hits/track)
- No saturation effects seen for ASIC (amp, TC, ..)
- Analysis ongoing (snapshots for 600 MeV/c deuterons)



ToT vs time (ns) for 600 MeV/c deuterons. No saturation seen



Isochrone r(t) curves for 5 layers in beam spot



Reconstructed tracks. Some cuts applied (50% min. eff., time cuts ..)

Status and Next Steps (HW)

- DAQ operation:
  - Readout system with clean and stable operation: > 6 months, 144 ch
  - Leave in running mode, further cosmic runs in 2017
  - Add more straw channels (~ 300 ch)
  - Study (current) trigger limit for DAQ operation (TRB3 design: ~ 300 kHz)

- Front-end:
  - No ASIC design iteration necessary (based on current test data)
  - Workout of STT front-end layout ongoing (space, cooling reqmts)
  - FE board slight re-designs for final version (space, cut analog out)

- TRB-system
  - TRB3-DAQ bandwidth sufficient for PANDA starting phase (lower lumi
  - New TRB design necess. for full lumi (TRB general PANDA/GSI project)

Status and Next Steps (SW)

- Data analysis (in-beam tests)
  - Analysis of beam test data ongoing in 2017 (lacking man power)
  - Prelim. resolutions (time, space, ToT) spoiled, corrections poss.& ongoing
  - ToT methods ongoing, dE/dx separation by ToT/dx, ToT_{corr}
  - ToT - dE (charge) calibration study (wishful for simulation)
  - ..
  - Absolute straw timing and pattern recognition studies
- Very important: readout is used for overall STT system test (urgently needed)
  - Measured possible straw (mis)alignment, tube-wire displacement (“2-leg”)
  - Method developed to check straw positions by data & re-align straws
  - Found: robust & efficient operation of straws in-beam even if misaligned
- Reminder: general failure tests required for all system components

Thank you

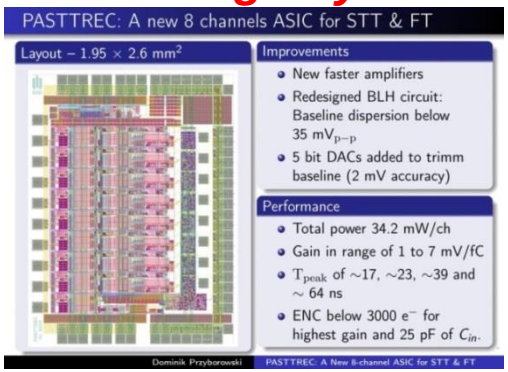
for your

attention

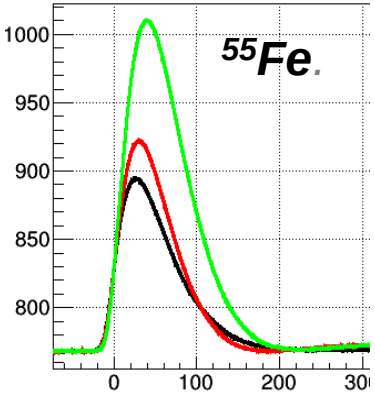
WPs: ASIC/TRB Readout System

- Readout of drift time and dE/dx for PID by time-over-threshold
- Pre-series system ready: PASTTRECv1-ASIC, FEB & TRB3 readout
- Preps done for beam test, few ASIC sets def. (progr. combs: 16×, PkT-G , 4100× TC)
- Option: 2nd ASIC version with 2-threshs for better ToT by end 2016
- TRB3 – PANDA DAQ integration ongoing (BW limit, Buffsize), for low lumi ok
- TRB new HW required **(?)** for full lumi (1.5 GB/s data rate per TRB)
- ToDo: cooling concept (~120 W)

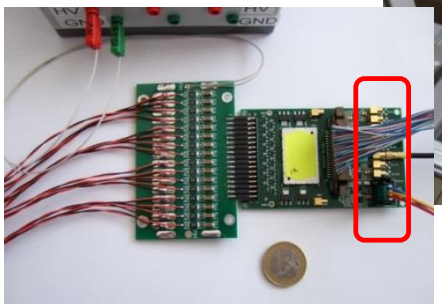
ASIC design by AGH



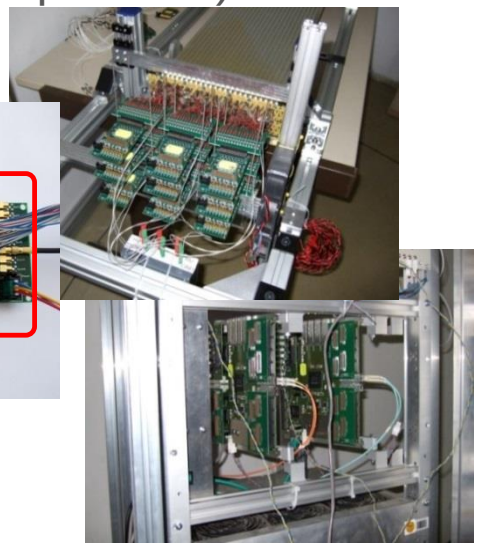
PASTTREC parameters



Straw signals (mV) for diff. ASIC sets.



HV coupling and FE-board with 2× ASIC.



FEBs at test system (top) and TRB3 readout (lower)

dE/dx (Charge) – ToT Calibration

- ASIC/TRB prototype data (red dots, left y-axis)
  - Time-over-threshold ↔ charge calibration (by ^{55}Fe here, later with proton beam)
  - Only 12 hits/track → 10% truncation only
- FADC prototype data (blue dots & axis)
  - 16 hits/track, up to 40% truncation best
- Clear dE/dx sensitivity seen for both
- Reminder: dE/dx min ~ 5 keV/cm

  @ 2bar Ar/CO_2(10%)