PASTTREC Status and Plans

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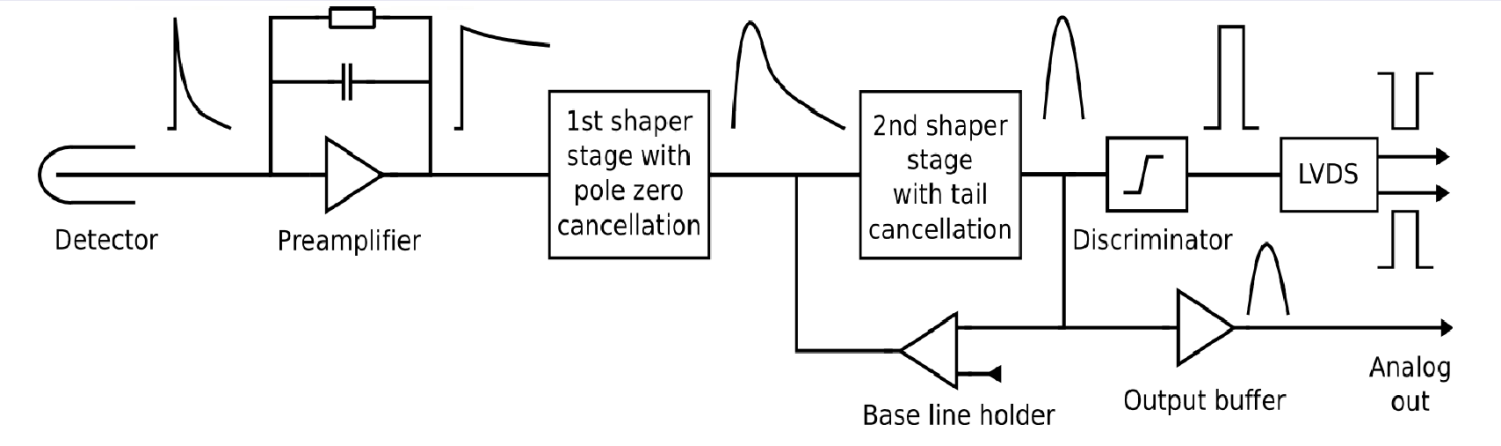
Outline

PASTTREC ASIC for straw tubes

Channel functionality



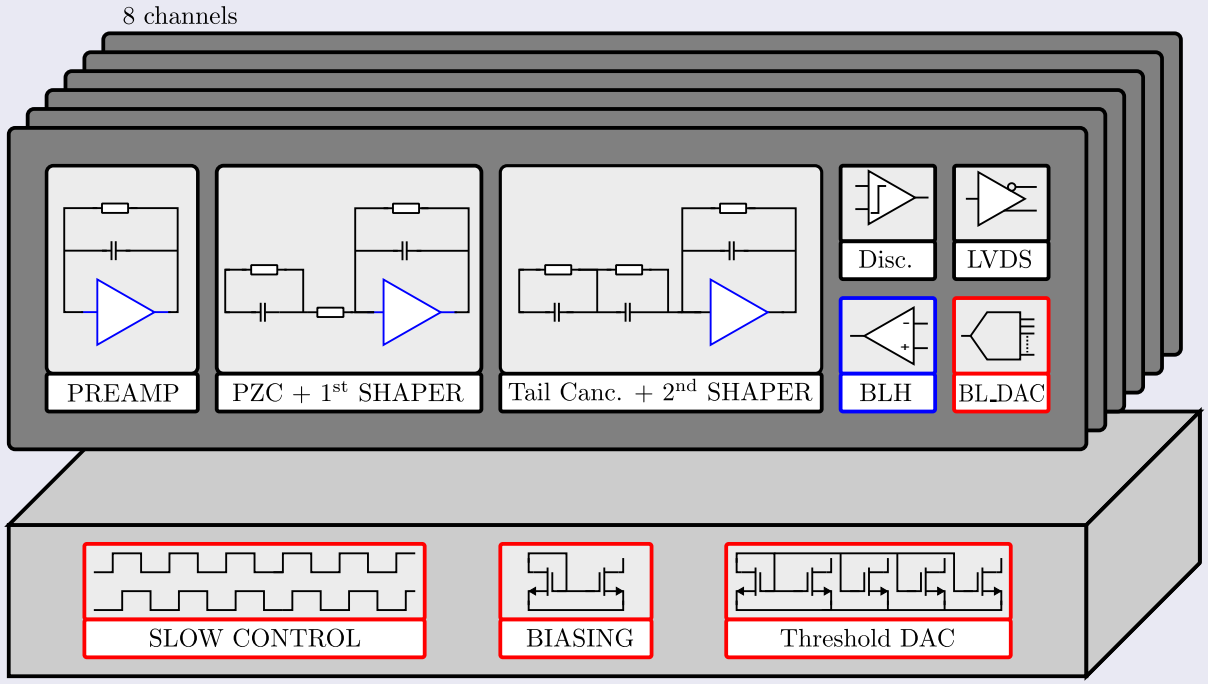
Features

- CSA with variable gain and time constant
- CR–RC^2 shaper with variable peaking time
- Ion tail cancellation circuit with trimming
- Baseline stabilized by BLH circuit
- Leading edge discriminator for time and ToT measurements
- Fast LVDS output
- Buffered analog output

PASTTREC ASIC for straw tubes

8-channel chip

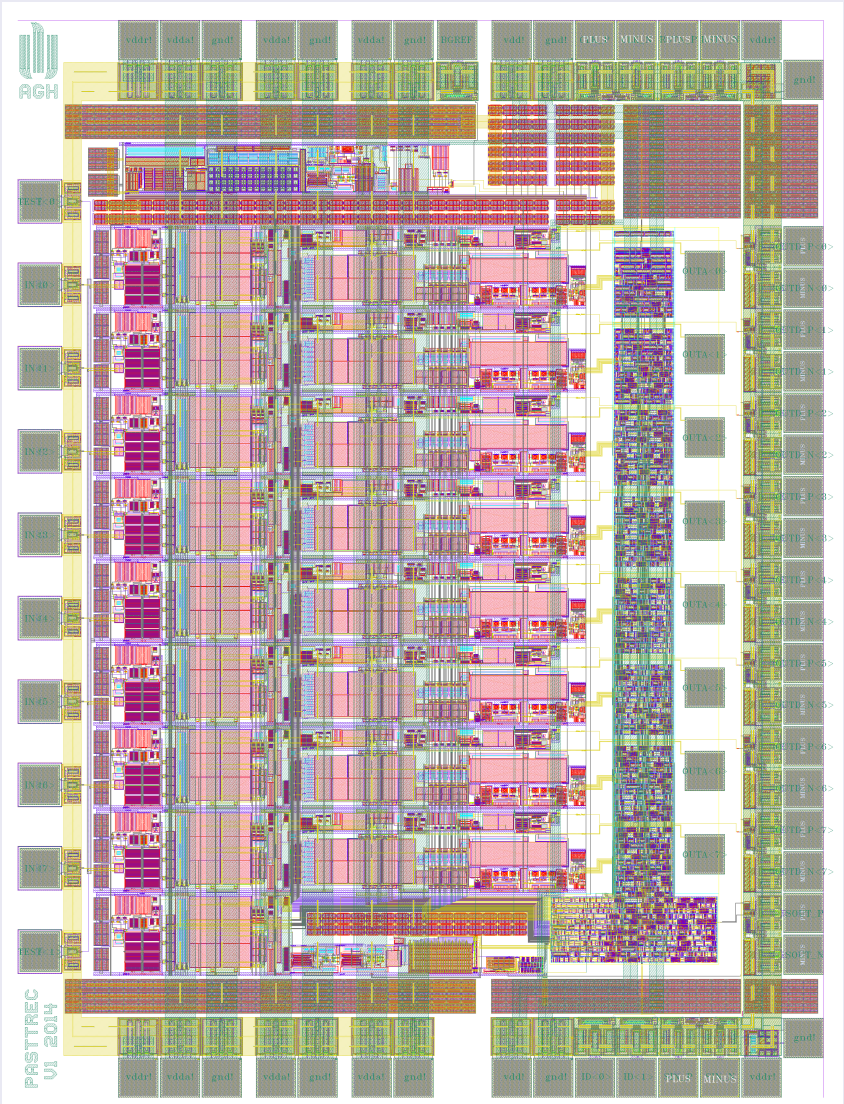
Block diagram



- Features:
  - Global DAC for threshold
  - Trimming DACs for each ch.
  - Slow control responsible for communication and settings
- AMS 0.35 μm CMOS
- 8 channels
- Fabricated in Oct 2014
- Used at UJ and Juelich

PASTTREC ASIC for straw tubes

Layout – 1.95 × 2.6 mm^2



Performance

- Total power 34.2 mW/ch
- Gain in range of 1 to 7 mV/fC
- T_{peak} of ∼17, ∼23, ∼39 and ∼ 64 ns
- ENC below 3000 e^- for highest gain and 25 pF of C_{in}
- Baseline dispersion below 35 mV_{p-p}
- 5 bit DACs to trimm the baseline (2 mV accuracy)

Next step - production of 50 readout boards

Technical info

Cost estimation

- Submission of 100 ASICs ranges between 4250-5500 Euro + VAT
- Production of 50 boards (SOFTCOM) 1100 Euro + VAT
- Packaging through EUROPRACTICE > 80 Euro/chip (rather expensive...)
- Components and Assembly to be added

Summary and Plans

- Where do we are with PASTTREC ?
  - Prototype straw tube setups with PASTTREC readout were built at UJ and Juelich
  - A lot of test-beam data was taken
  - We hope to arrive to some conclusions today-tomorrow...
- What next ?