GSI Event-driven TDC with 4 Channels

GET4

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Agenda

- **Requirements for CBM ToF**
- Testchip DANTE
- First TDC Prototype GET4

Requirements for the CBM ToF

- Very high time resolution < 25ps
- Double hit resolution < 5ns
- Event rate up to 50 kHz per channel
- Capability to measure time over threshold
- Low power consumption with less than 30 mW per channel
- Number of Channels: ~ 65.000
- Triggerless operation:
  - Each event combined with a timestamp
  - Epoche event on timestamp counter overflow
- Timestamp counter of all chips has to run synchronously

Agenda

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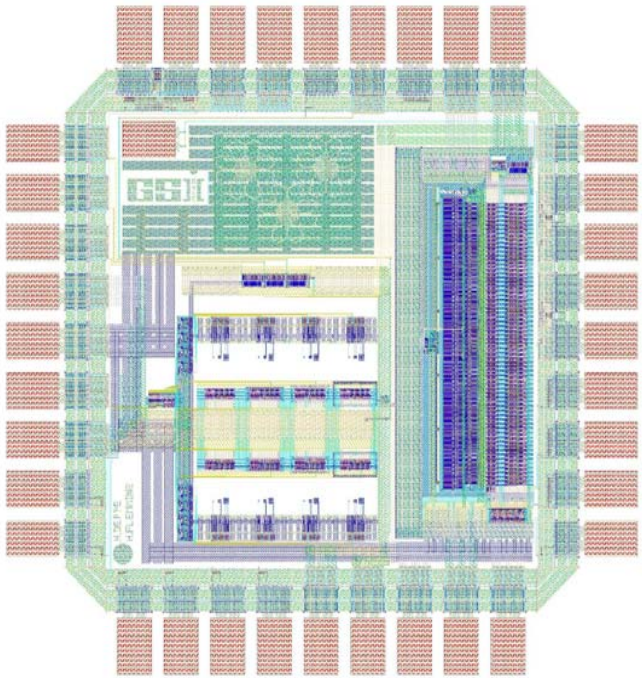
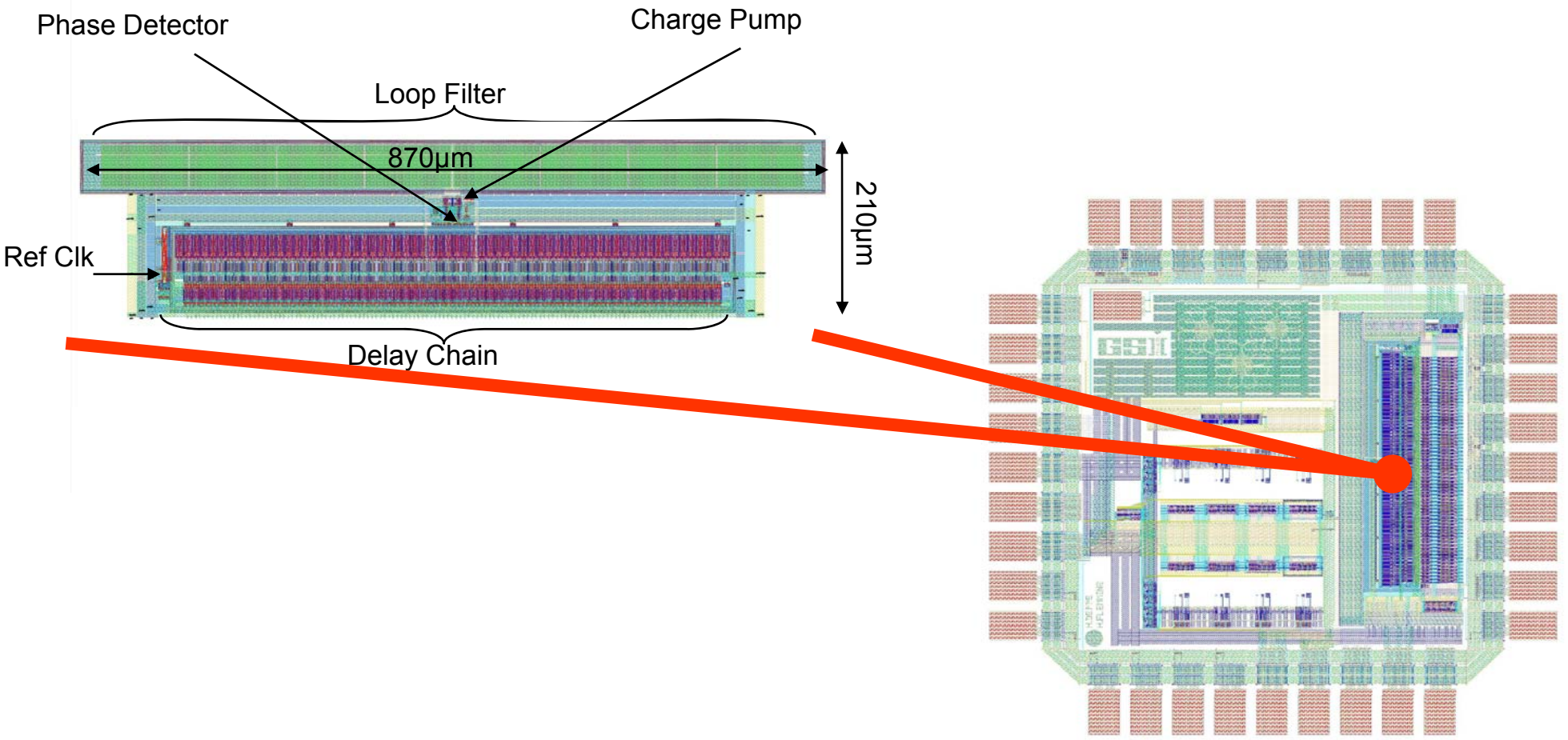
Testchip for a DLL Based Time Core

- Closed regulation loop
- Self calibration to compensate temperature and process variations
- Intrinsic resolution is determined by the delay of a basic cell :
- $T_{Bin} = T_{Clk} / N$

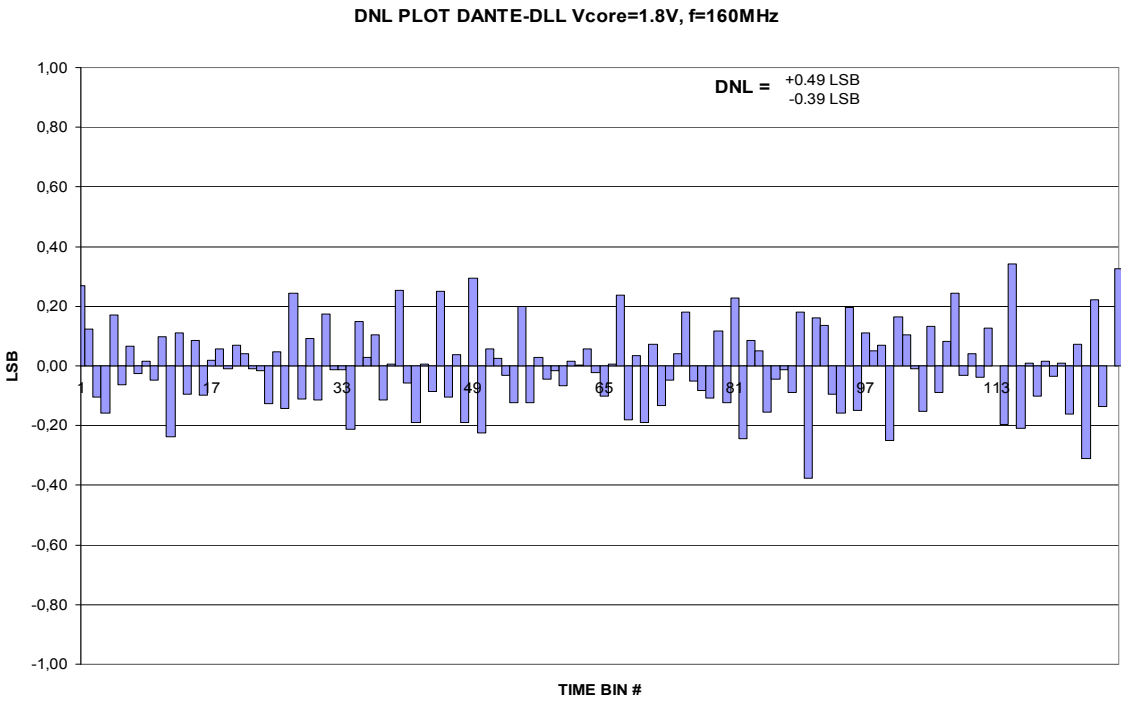


Testchip for a DLL Based Time Core



Measurements and Results DANTE

- Results :
  - Lock: 135MHz – 164MHz
  - Linearity: DNL: +/- 0.4 LSB
    INL: +/- 0.5 LSB
  - Resolution @ 160MHz Clk
  - σ_{uc} = **20.34ps ± 0.19ps**



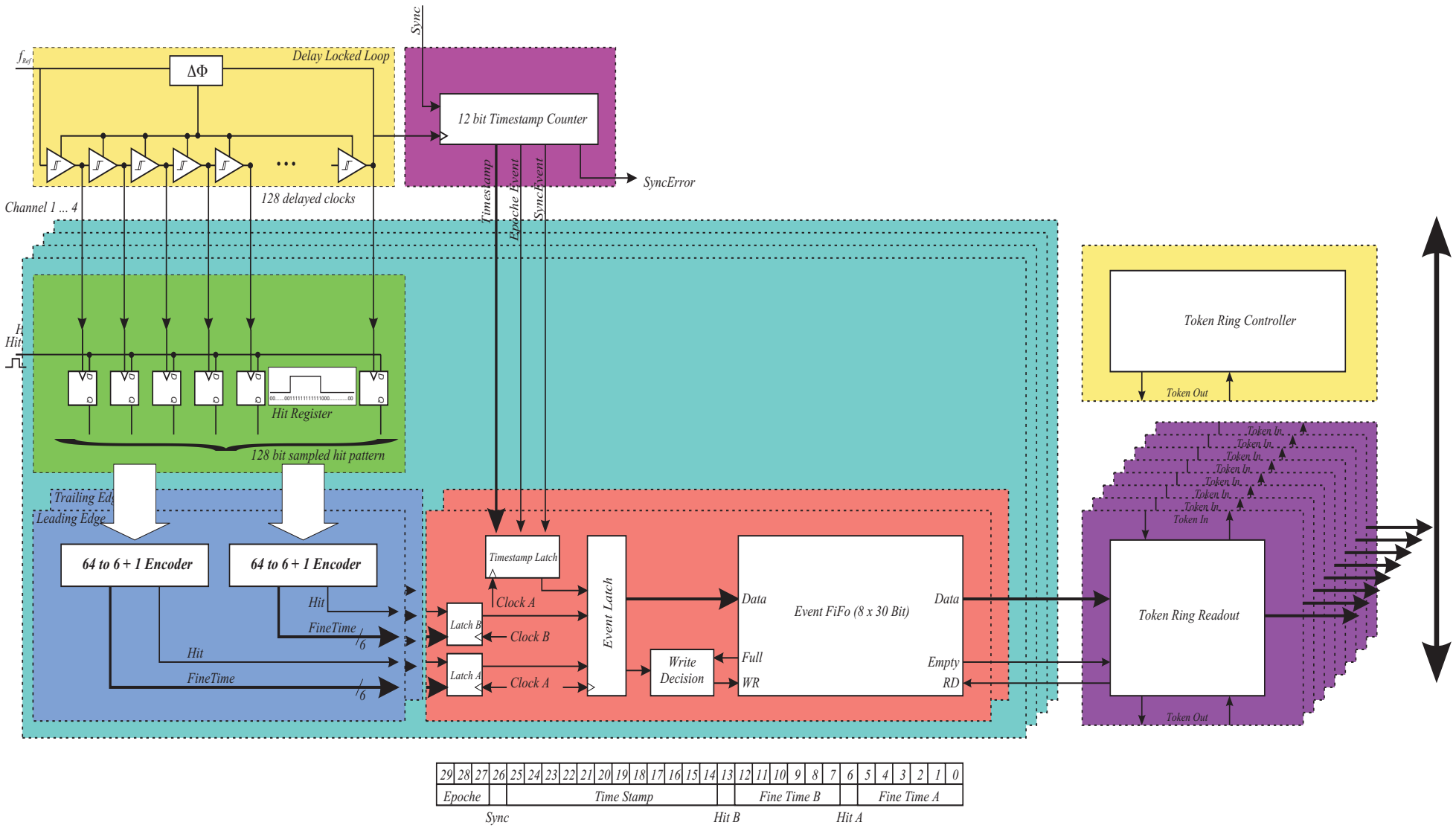
Agenda

- Requirements for CBM ToF
- Testchip DANTE
- **First TDC Prototype GET4**

GET4 Prototype

- Full size prototype with 4 channels
- UMC 180nm process
- 1P6M layer
- 3200µm x 3200µm, 64 Bondpads
- Submitted in Oct. 2008

Schematic Overview of GET4 Prototype



29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Epoche			Time Stamp														Fine Time B							Fine Time A						

Sync Hit B Hit A

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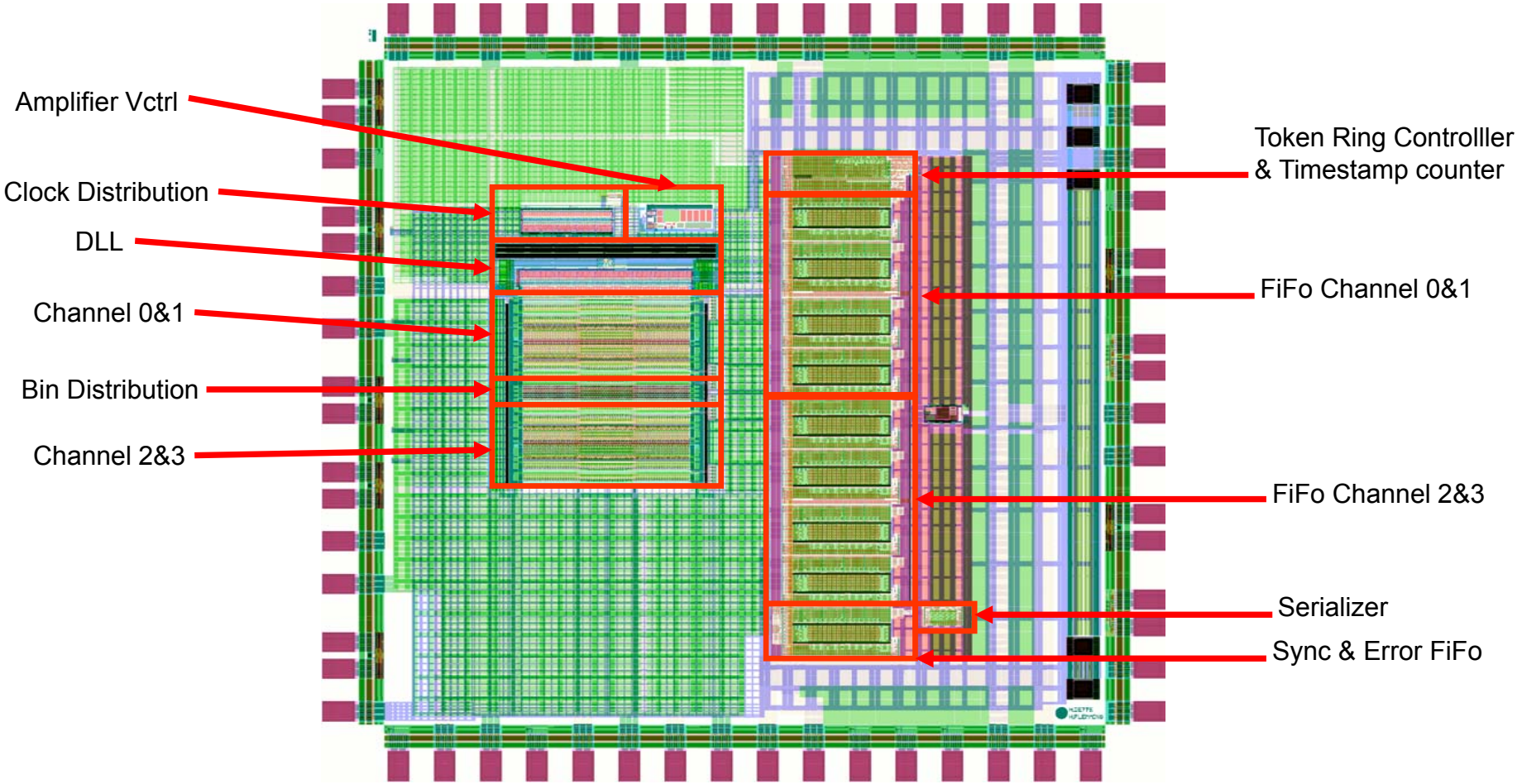
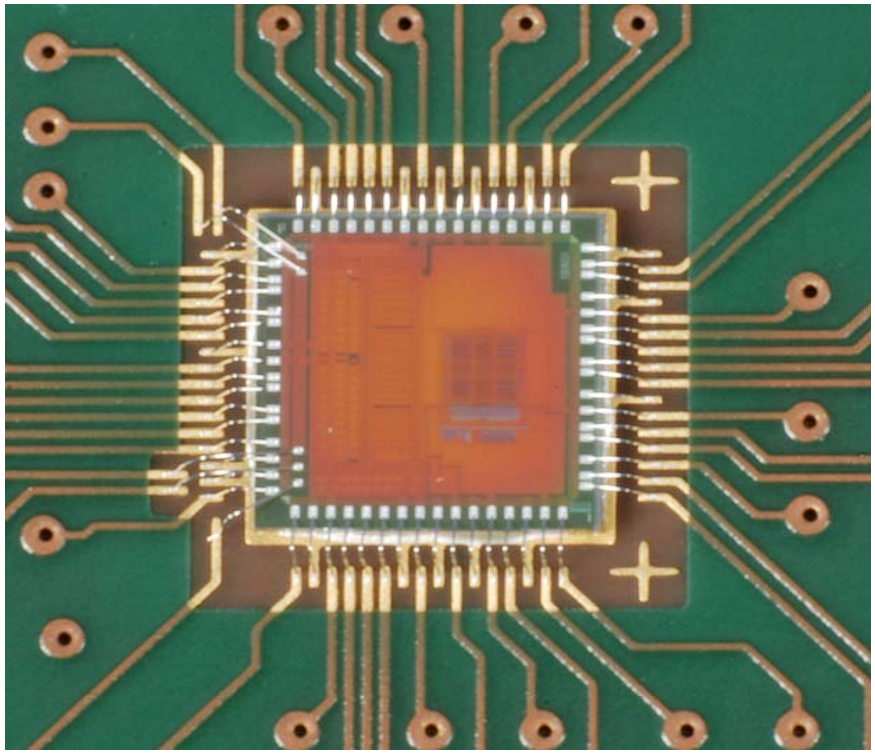
GET4 Layout

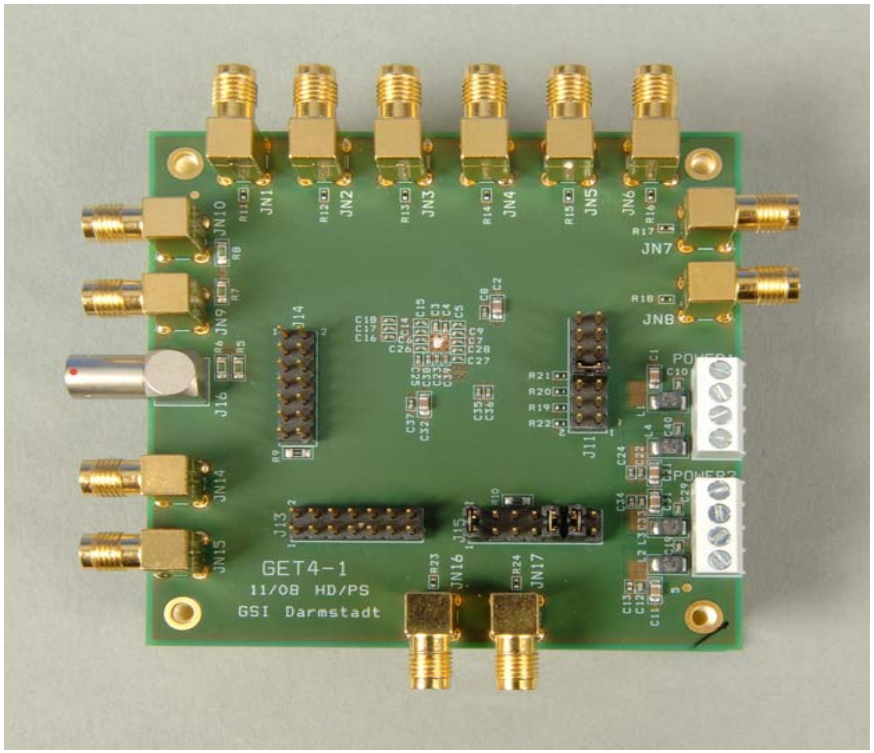

Amplifier Vctrl
Clock Distribution
DLL
Channel 0&1
Bin Distribution
Channel 2&3
Token Ring Controlller
& Timestamp counter
FiFo Channel 0&1
FiFo Channel 2&3
Serializer
Sync & Error FiFo

GET4 Prototype PCB

Bottom side view



Top side view



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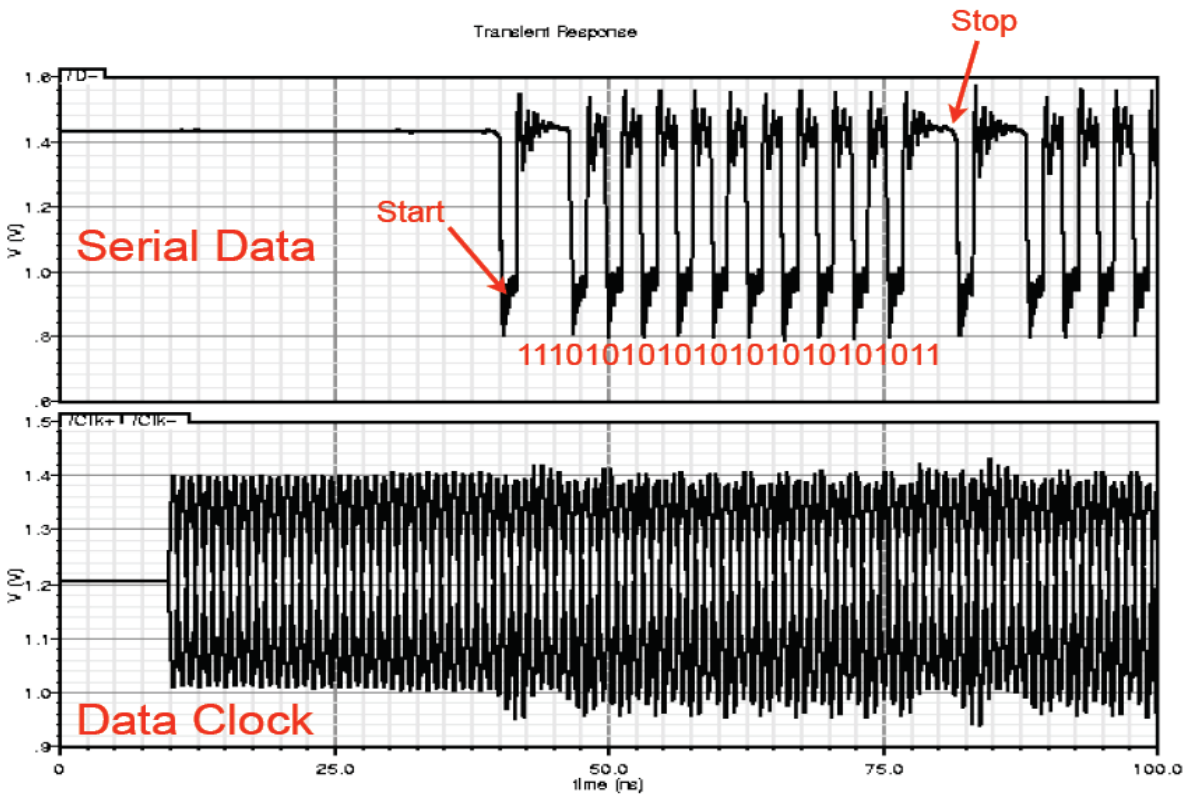
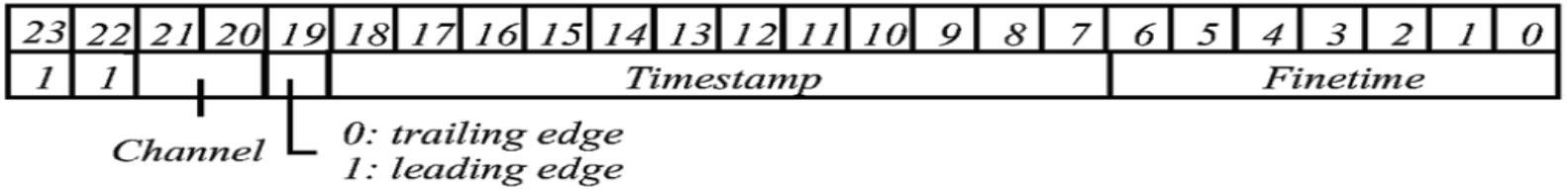
Serial Data Transmission

- External Data Clock
  - For 50 kHz/Ch event rate
  - => Min. Data Rate 10.5 MBit/s
  - Maximum Data Rate 312 MBit/s
- Asynchronous Data format
  - 1 Start Bit (Low)
  - 24 Data Bits
  - 1 Stop Bit (High)
  - no Parity
- LVDS Clock input
- LVDS Serial Data Output

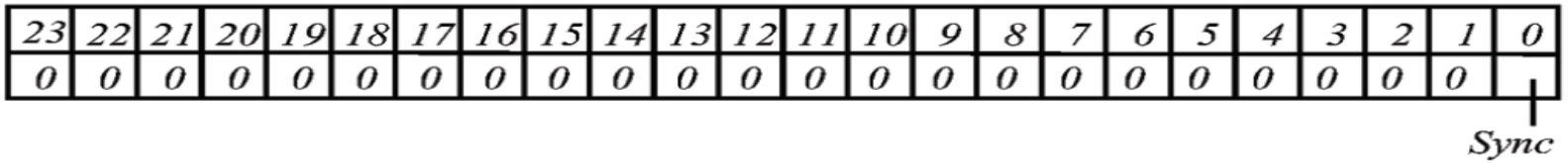


Event Format

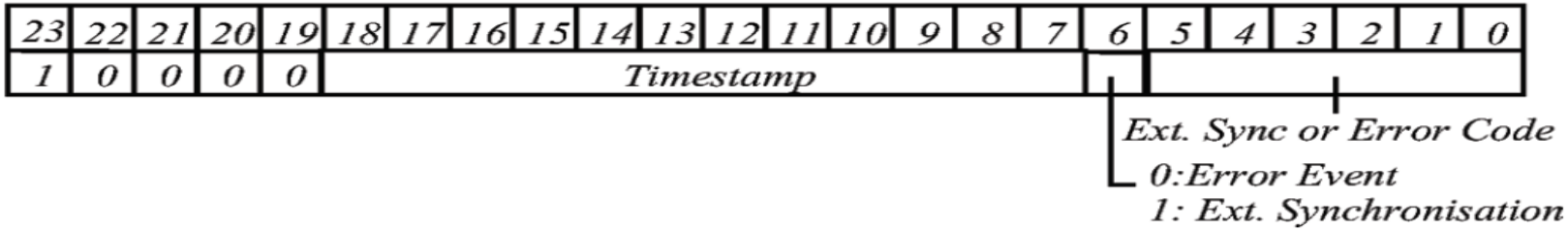
Data Events



Epoche Event

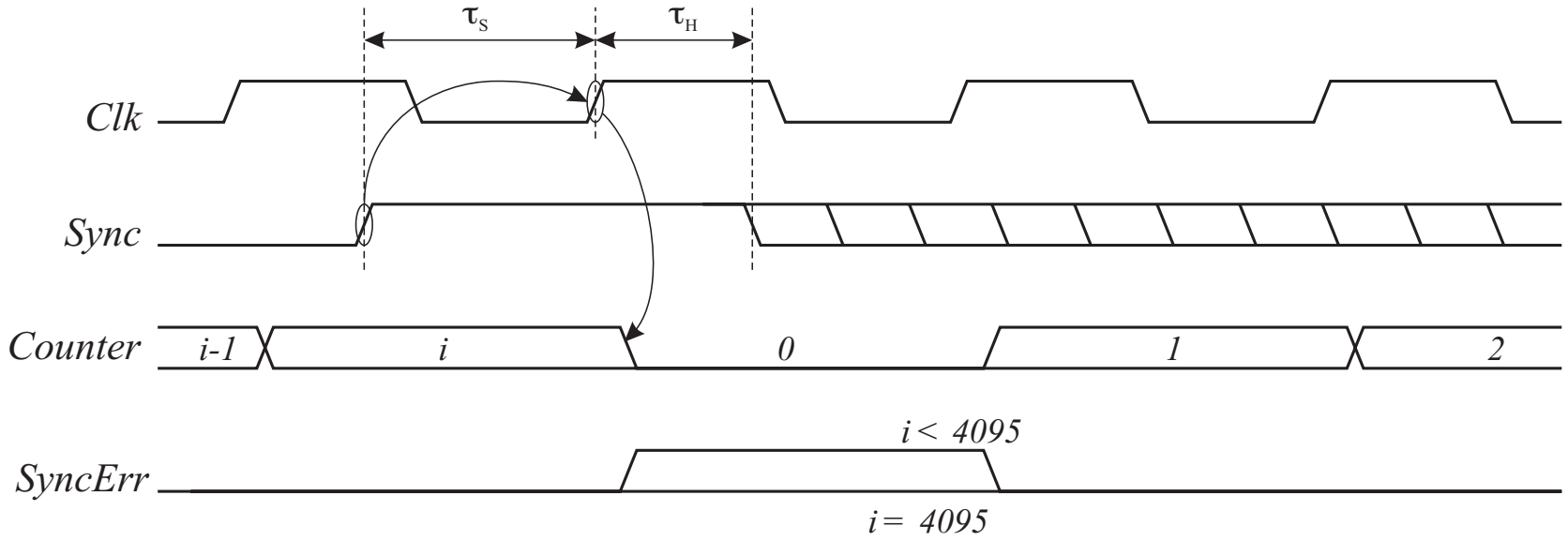


Ext. Sync and Error Event



Timestamp Synchronization

- External Sync signal
- Synchronization on next leading edge of clock after leading edge of Sync signal
- Flagging of Epoche and Sync events

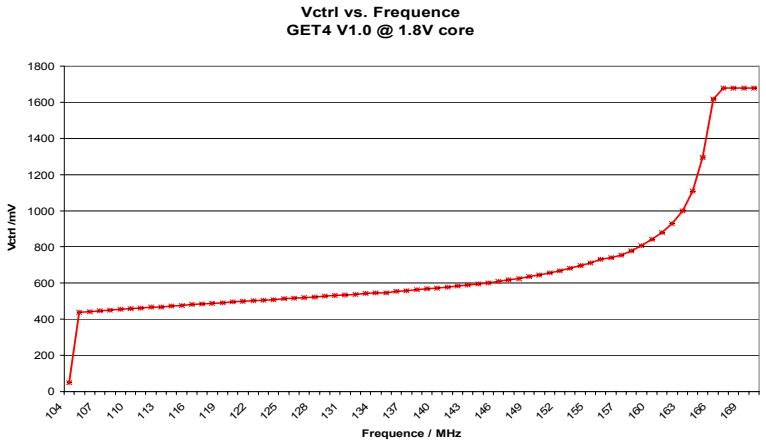


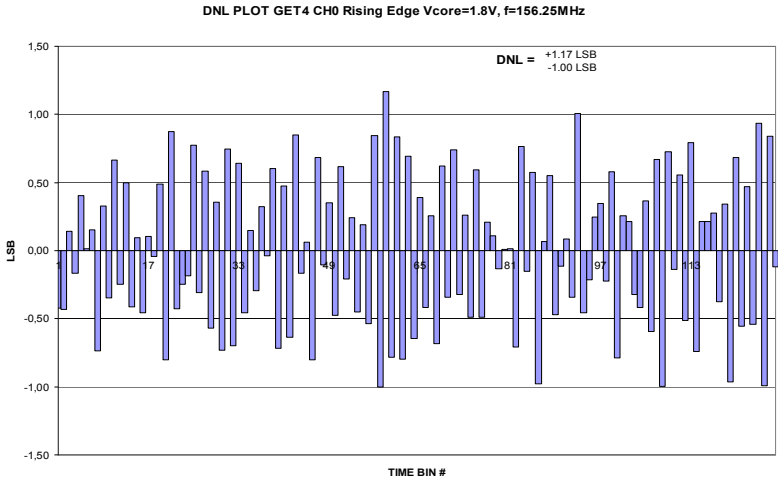
Measurements and Results GET4

- Clock 156.25MHz
- Lock Range 110MHz – 165MHz
- Linearity:
  - DNL > +/- 1.2 LSB
  - INL > +/- 1.5 LSB

- Resolution: $\sigma_{uc} \approx$ 23ps ± 1ps

- Power consumption:
  - 27mW/Chan @ 150kHz event rate





Next Steps

- Upgrading of Linearity
  => Improve the Resolution
- Slow control, etc.

Thanks.....

- ..... **for your attention**