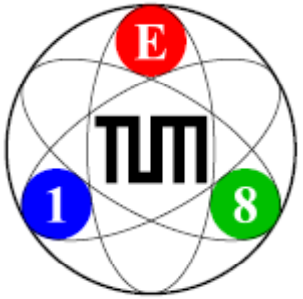


TDC for PANDA

I.Konorov

Motivation

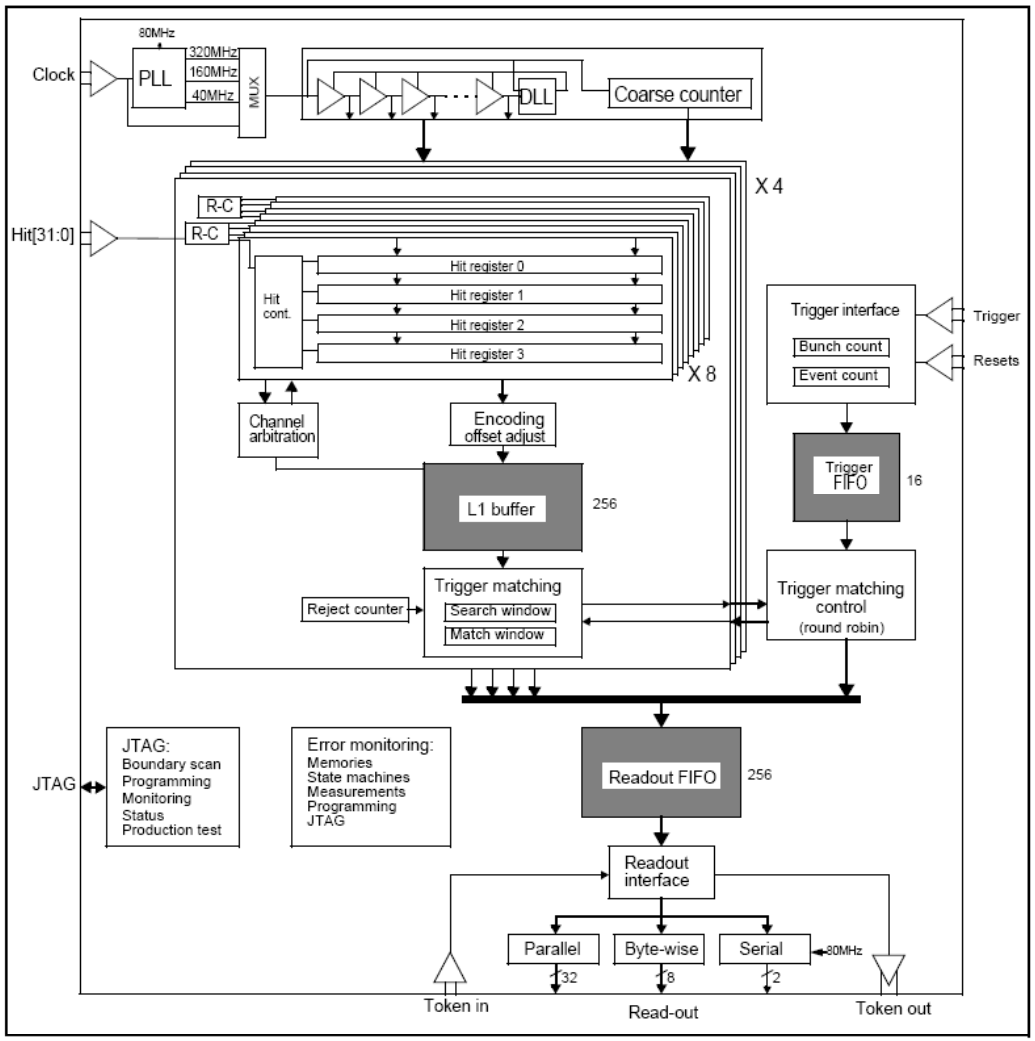
- CERN has 2200 HPTDC chips status from January 2008
- Agreement with CERN to get TDC chips for PANDA
- Decision to be taken now

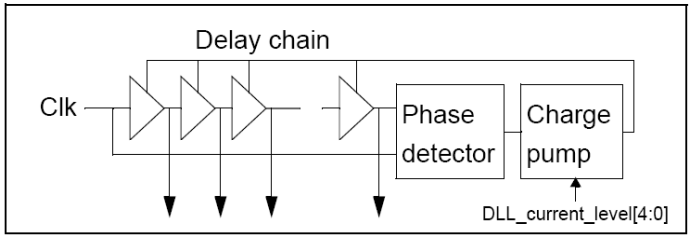
Detectors require TDC readout

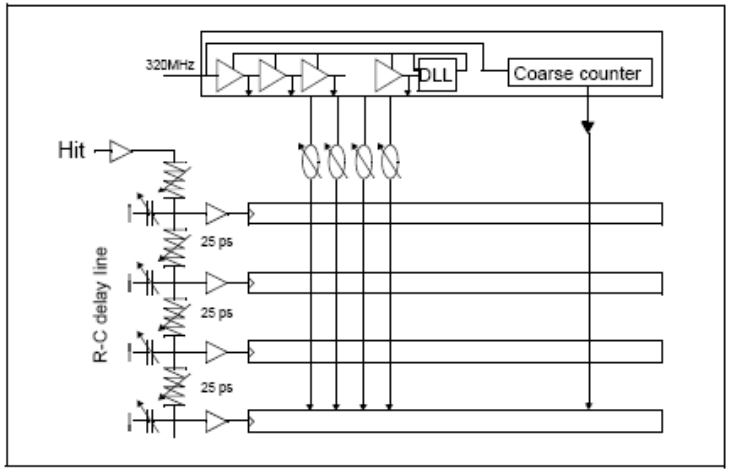
- Straws, MDC(straw), MuonChamber
  - 20k channels
  - Amplitude Time over Thr
  - Radiation tolerant
  - time resolution < 1ns
  - hit rate 7kHz/channel

- **Endcap DIRC**
- **Barrel DIRC**
- TOF - ?

HPTDC architecture

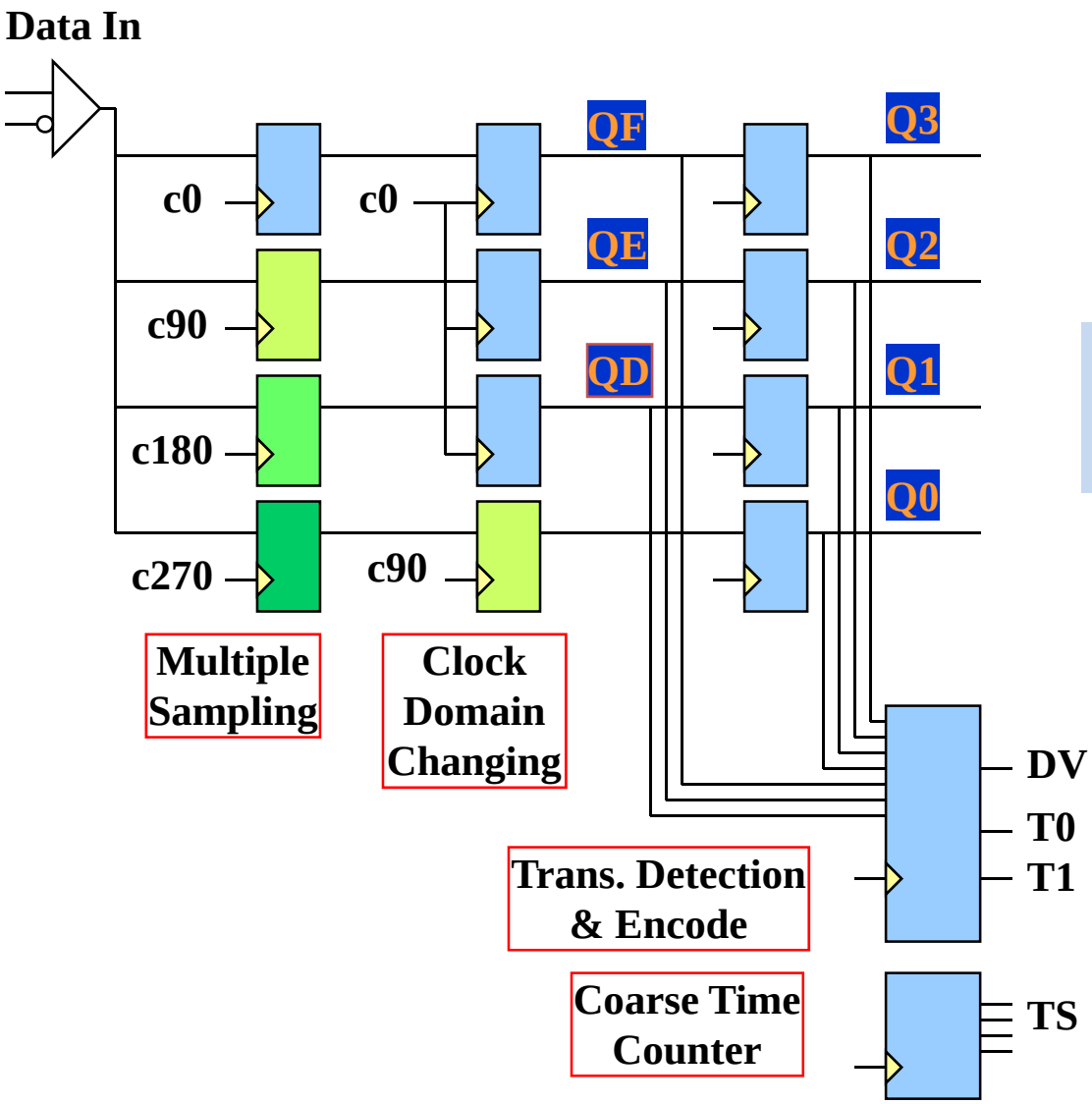






- Trigger driven
- Bin size 100/25ps
- Resolution 25ps
- 32channels/chip
- Cost: 100 Euro/chip
- 0.25u technology - radiation tolerant

FPGA based TDC1

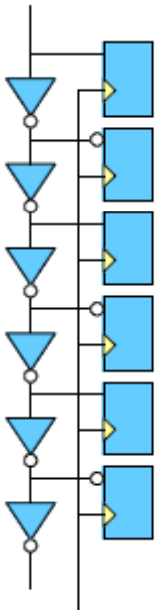


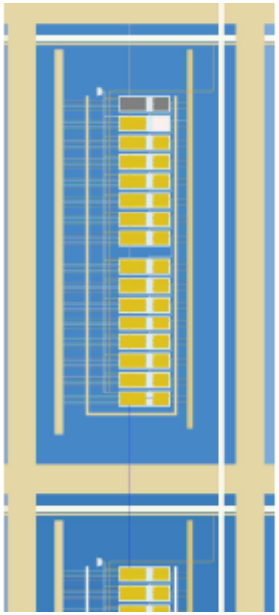
4x Sampling:
250 MHz: 1ns(LSB), 288ps(RMS)
400 MHz: 625ps(LSB), 180ps(RMS)

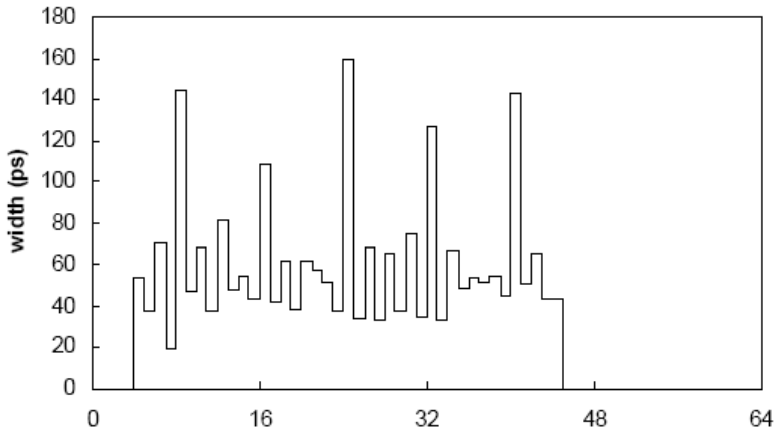
FPGA based TDC, next step

Jinyuan Wu and Zonghan Shi
Fermilab

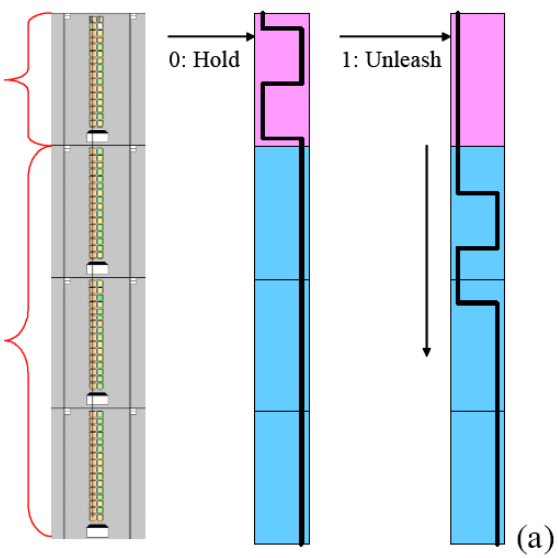
ALTERA Cyclone II EP2C8T144C6
Tap delay: 60 ps
Ultra-wide bin: 165 ps
Main clock : 400 MHz



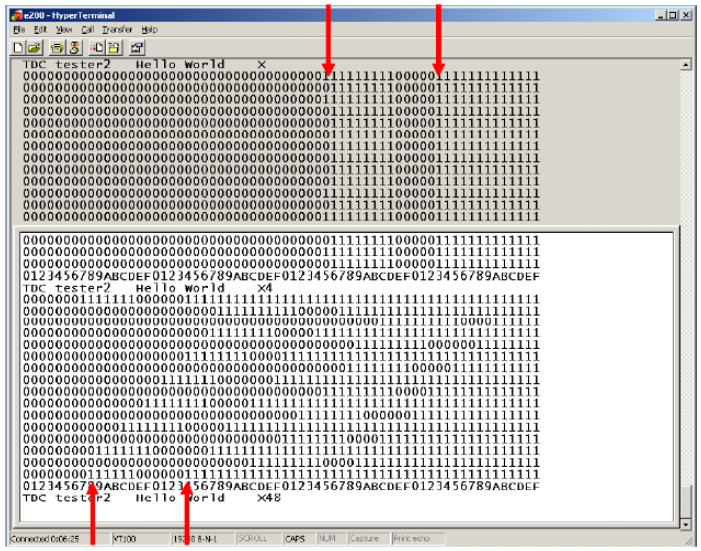




FPGA based TDC next step



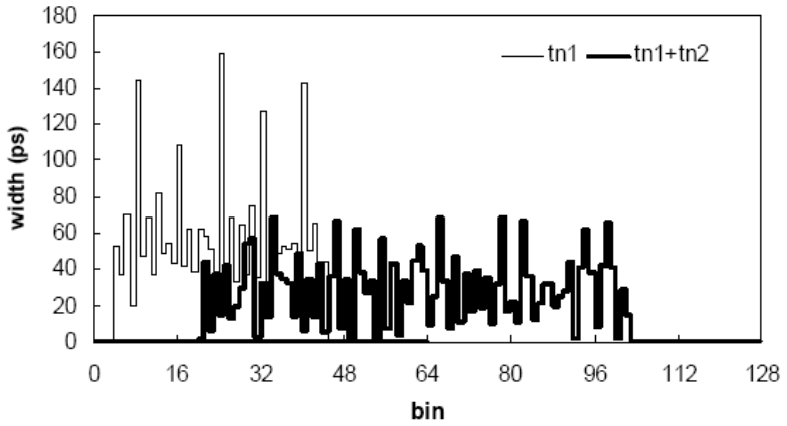
(a)



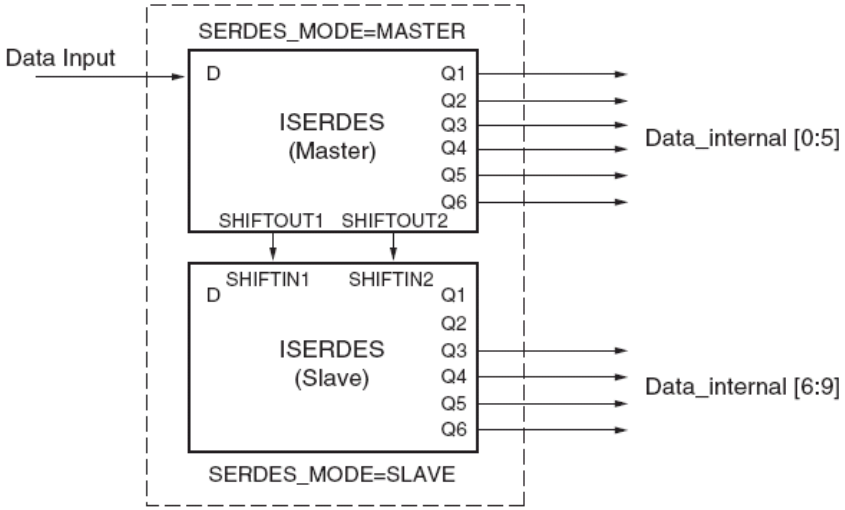
(b)

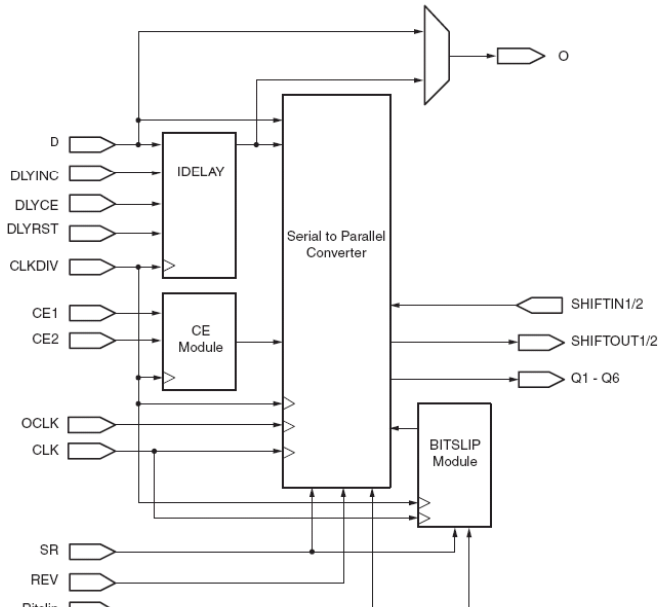
Wavelet launcher:

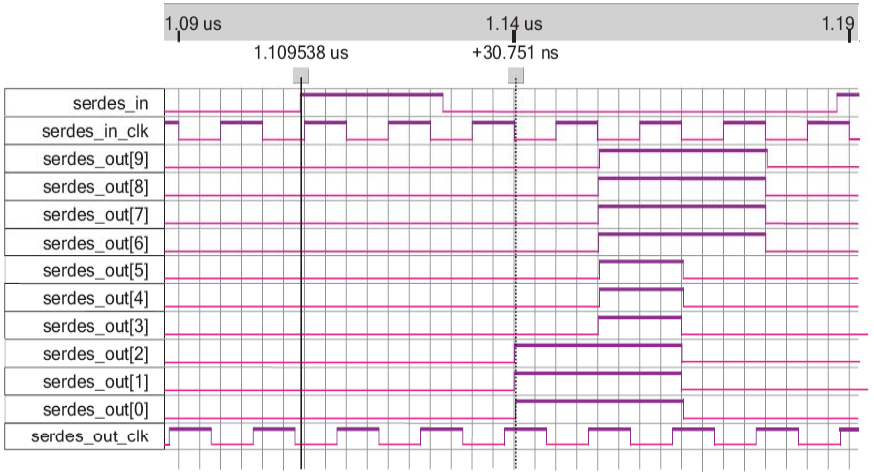
- Input pulse unleash bit pattern
- Multiple measurement



DeSerializer as TDC







Features:

- LVDS input
- 64 taps for delay adjusting, one tap 75ps
- Controlled delay by Reference Clock