1st FAIR FEE Workshop

Wednesday 12 October 2005

Plenary (09:00-10:45)

time	[id] title	presenter
09:00	[10] General Purpose Charge Readout Chip	MUSA, Luciano
09:35	[11] Studies on Programmable Charge Amplifier	TRAMPISCH, Gerd
09:55	[12] Building Blocks for FAIR FEE - goals and first results	TIELERT, Reinhard
10:20	[13] Low Power Pipeline ADCs	MUTHERS, David

Plenary (11:15-12:40)

time	[id] title	presenter
11:15	[14] FEE for Nuclear Spectroscopy at FAIR	LAZARUS, Ian
11:50	[15] Towards a Concept: NUSTAR Slow Control	WÖRTCHE, Heinrich
12:15	[16] Progress in RPC-FEE development	CIOBANU, Mircea

Plenary (14:00-16:00)

time	[id] title	presenter
14:00	[17] Time Distribution System	KONOROV, Igor
14:30	[18] A Campus-Wide Time Synchronization System - „BuTiS“	MORITZ, Peter
15:00	[19] Time measurement with differential ring oscillators	FISCHER, Peter
15:30	[20] A Multi Gigabit Clock and Data Recovery Testchip fabricated in 0.18µm CMOS	TONTISIRIN, Sitt

Plenary (16:30-18:00)

time	[id] title	presenter
16:30	[21] Symbiosis of DAQ, Accelerator Settings, Diagnostics and Slow Controls at Experimental Storage Rings	KOZHUHAROV, Christophor
17:00	[22] MUST II: large solid angle light charged particle telescope for studies with radioactive beams	POLLACCO, Emanuel
17:30	[23] The VLSI/ASIC based readout technology for the spectroscopic signal processing of the UHV compatible Si multi detector system (CHICSi)	GOLUBEV, Pavel