Low Power Pipeline ADCs

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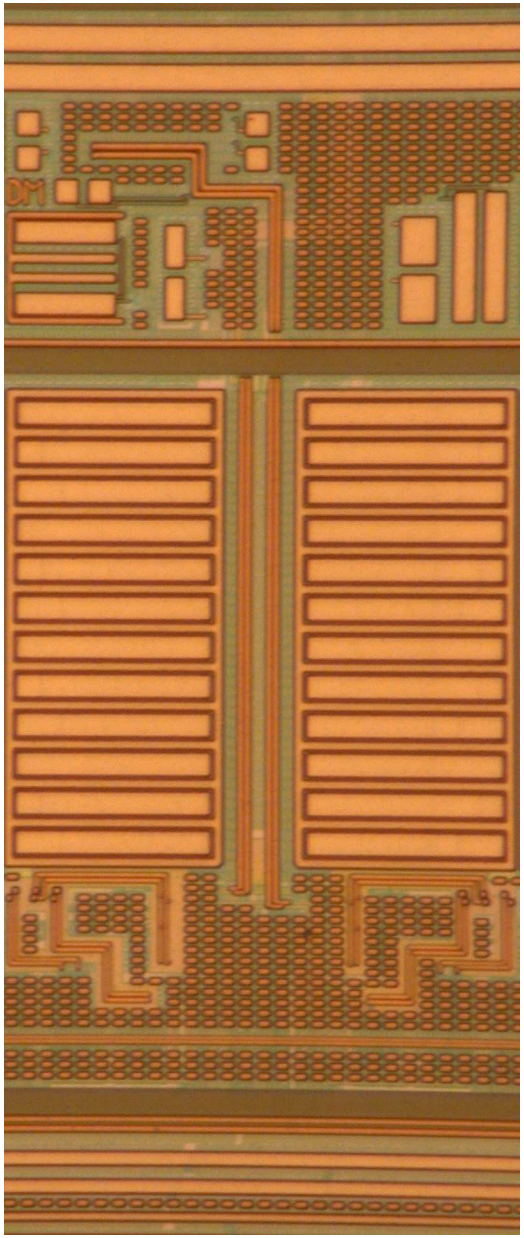
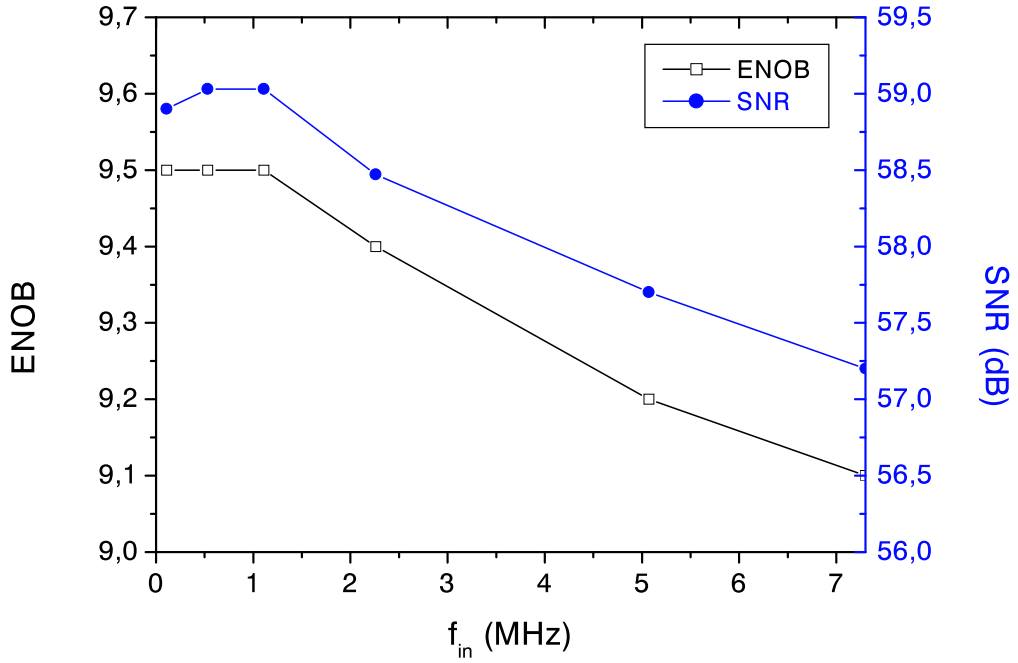
TRAP-ADC for the ALICE-TRD





Samplingrate	10MS/s
Resolution	10bit
Power	12mW
Area	0.11mm^2
ENOB @1MHz	9.5bit
SNR @1MHz	59.2dB

ADC for future projects:

High flexibility!

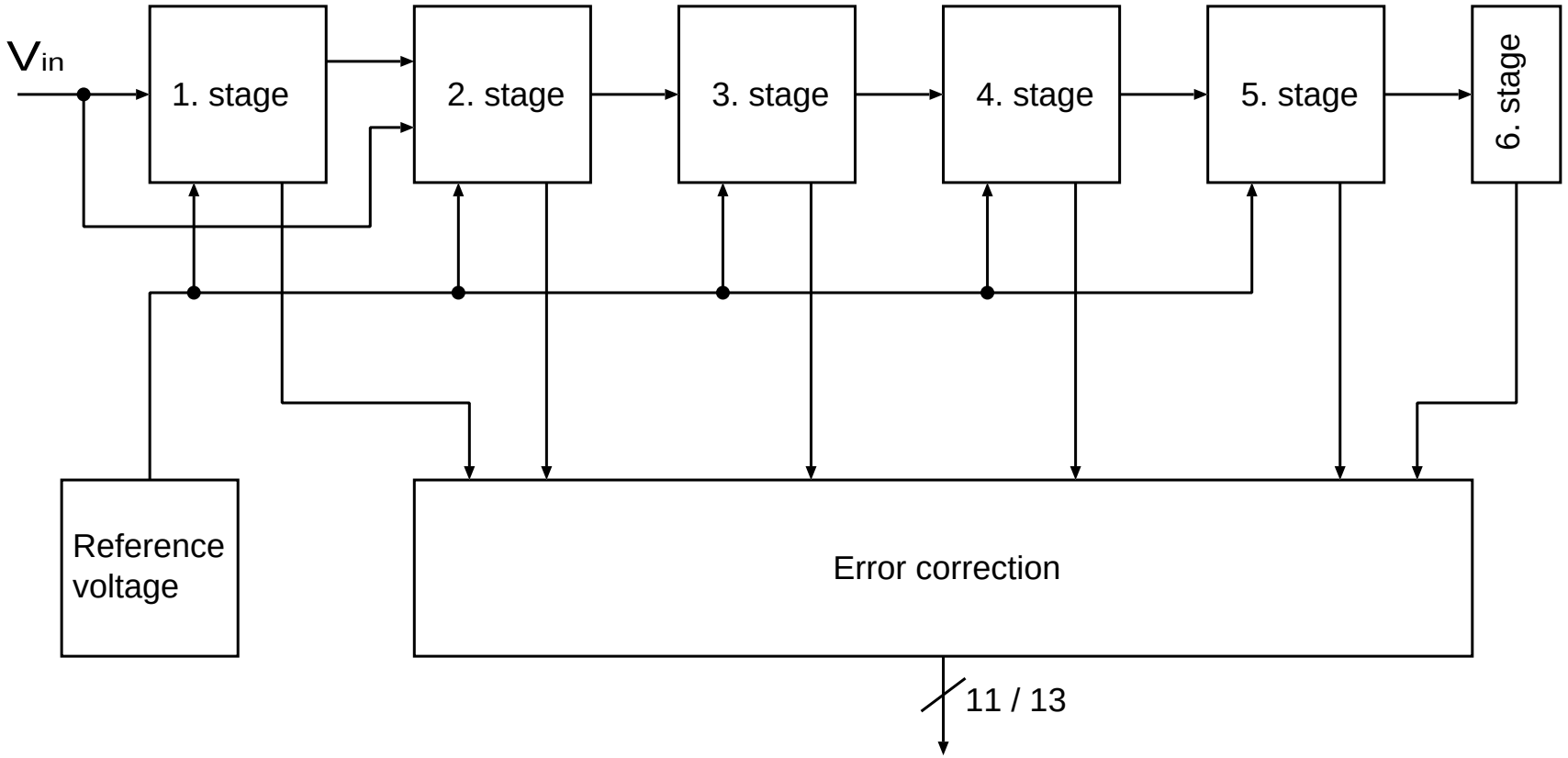
- *Configurable Resolution* 10bit / 12bit, Power accordingly

- Useful for wide range of f_{sample}, *Power ~ f_{sample}*

- Low Power: Promised *20mW @50MS/s, 10bit*
  35mW @50MS/s, 12bit

- Suited for mixed-signal implementations

Pipeline-ADC: Flexible 10(11) / 12(13)bit ADC



First testchip implemented
Samplerate up to 75MS/s currently

Various low-power techniques

- Pingpong sampling: Full-length sample interval

- Pseudodifferential circuitry: Saves CM-regulation

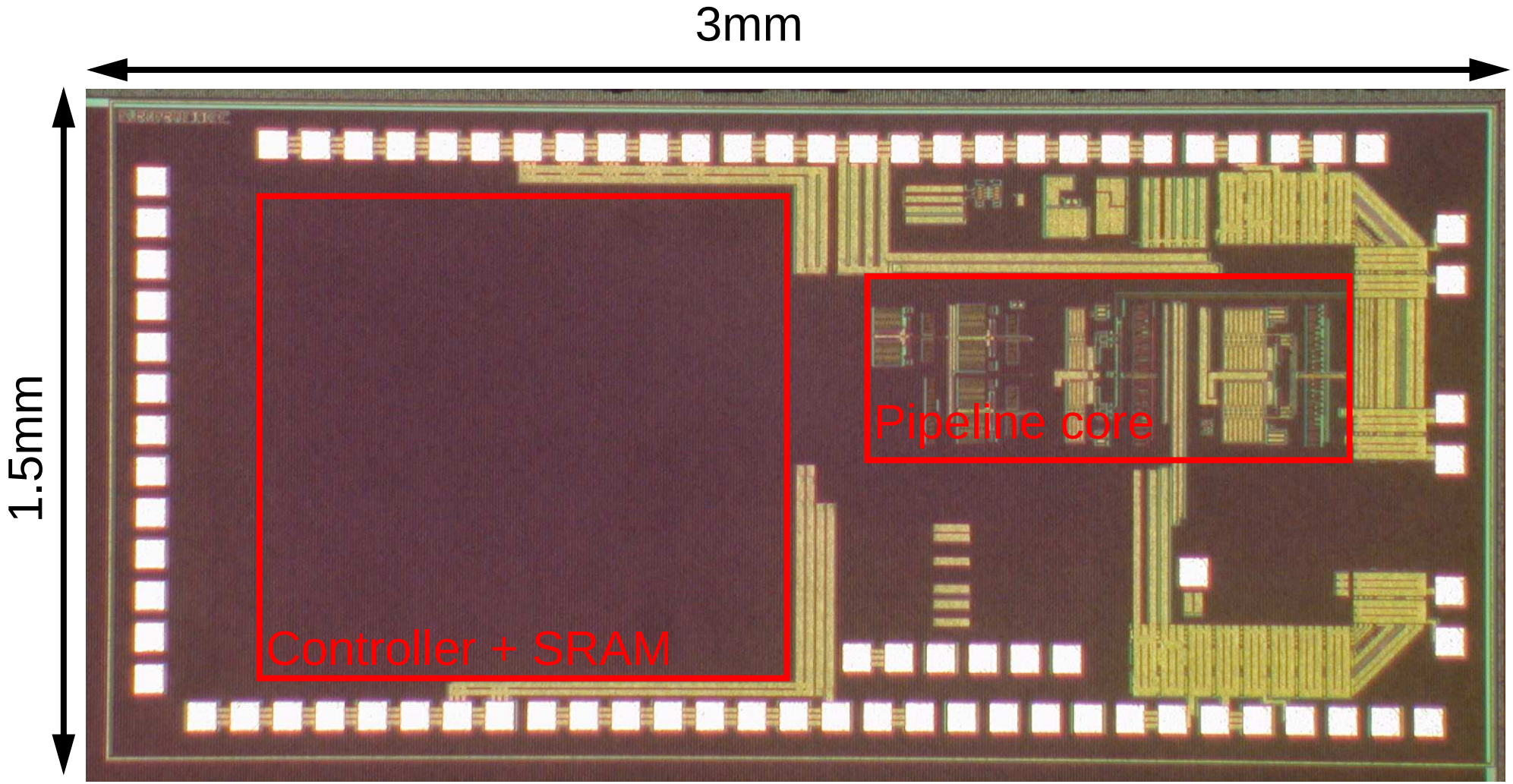
- No explicite S&H: Use implicite sampling of SC-circuits

- 100% Switched Capacitor: Power ~ f_{sample}

- optimized resolution per stage

- aggressive capacitor sizing: benefit of TRAP-ADC design

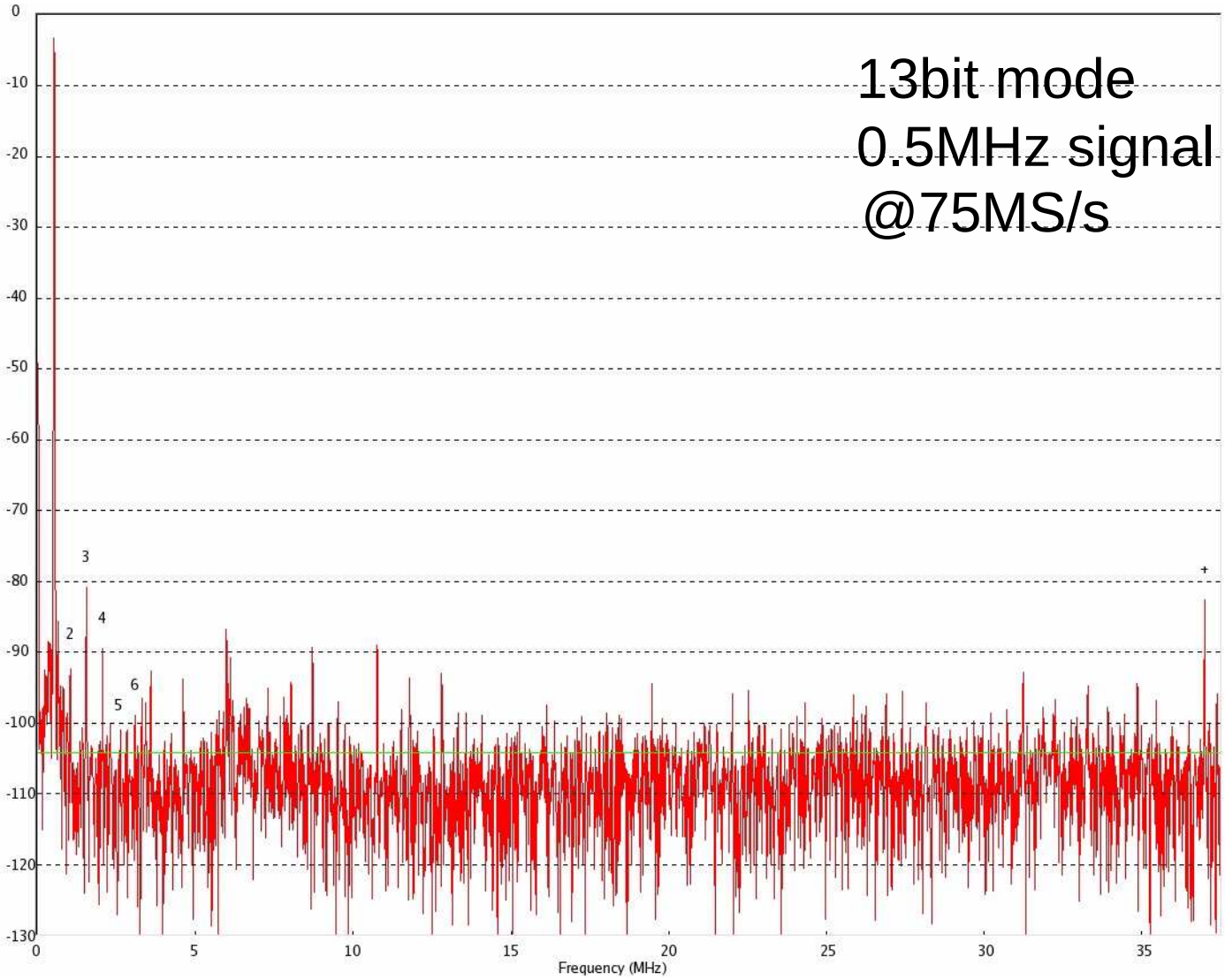
Implementation Results



UMC 0.18µm CMOS
Pipeline core: 0.4mm^2

Power @75MS/s, 13bit mode: 53mW

Power @75MS/s, 11bit mode: 30mW

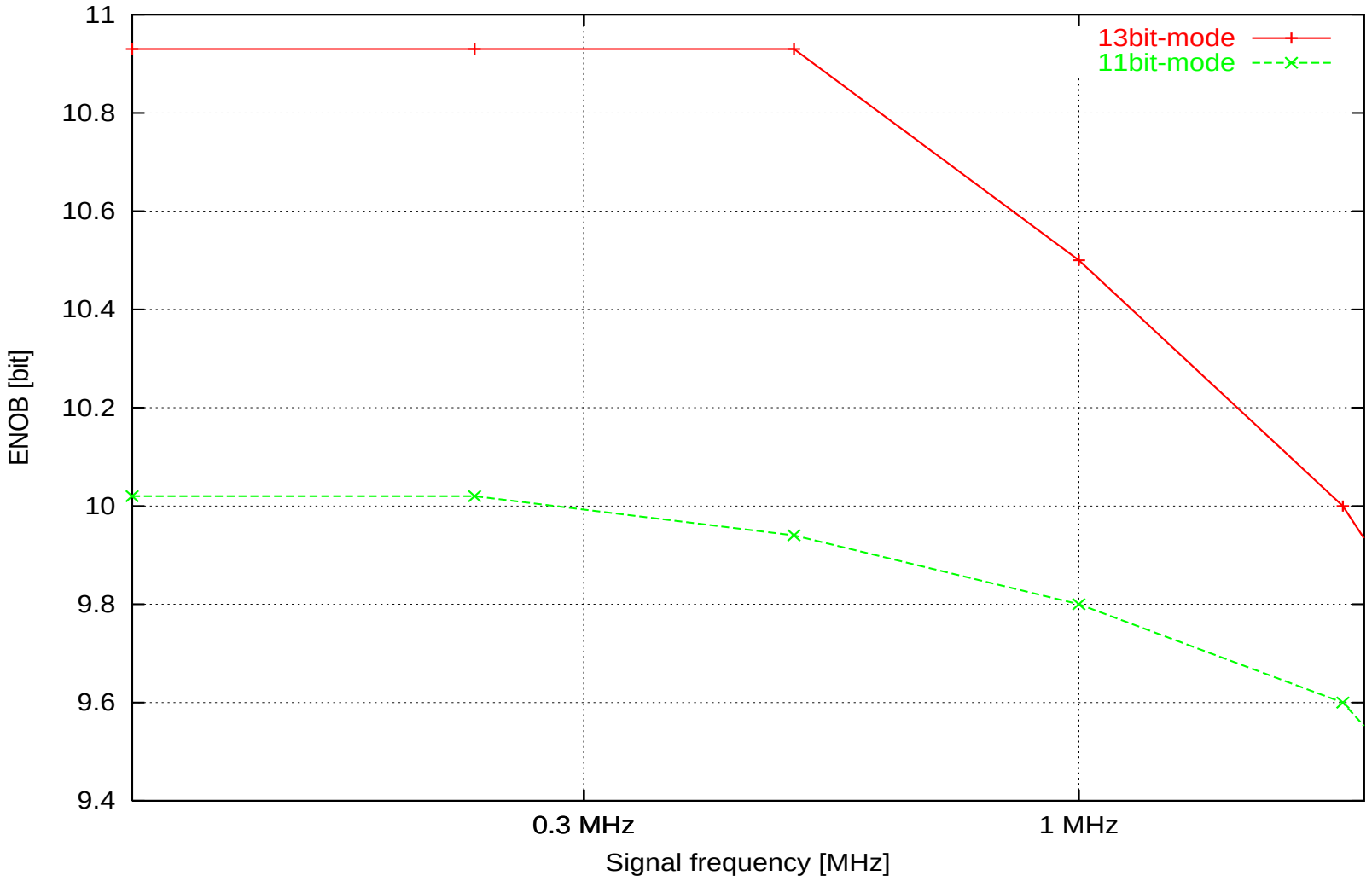


SINAD	67.4dB
SNR	68.0dB
THD	-76.6dB
ENOB	10.9bit

Higher Signal frequencies

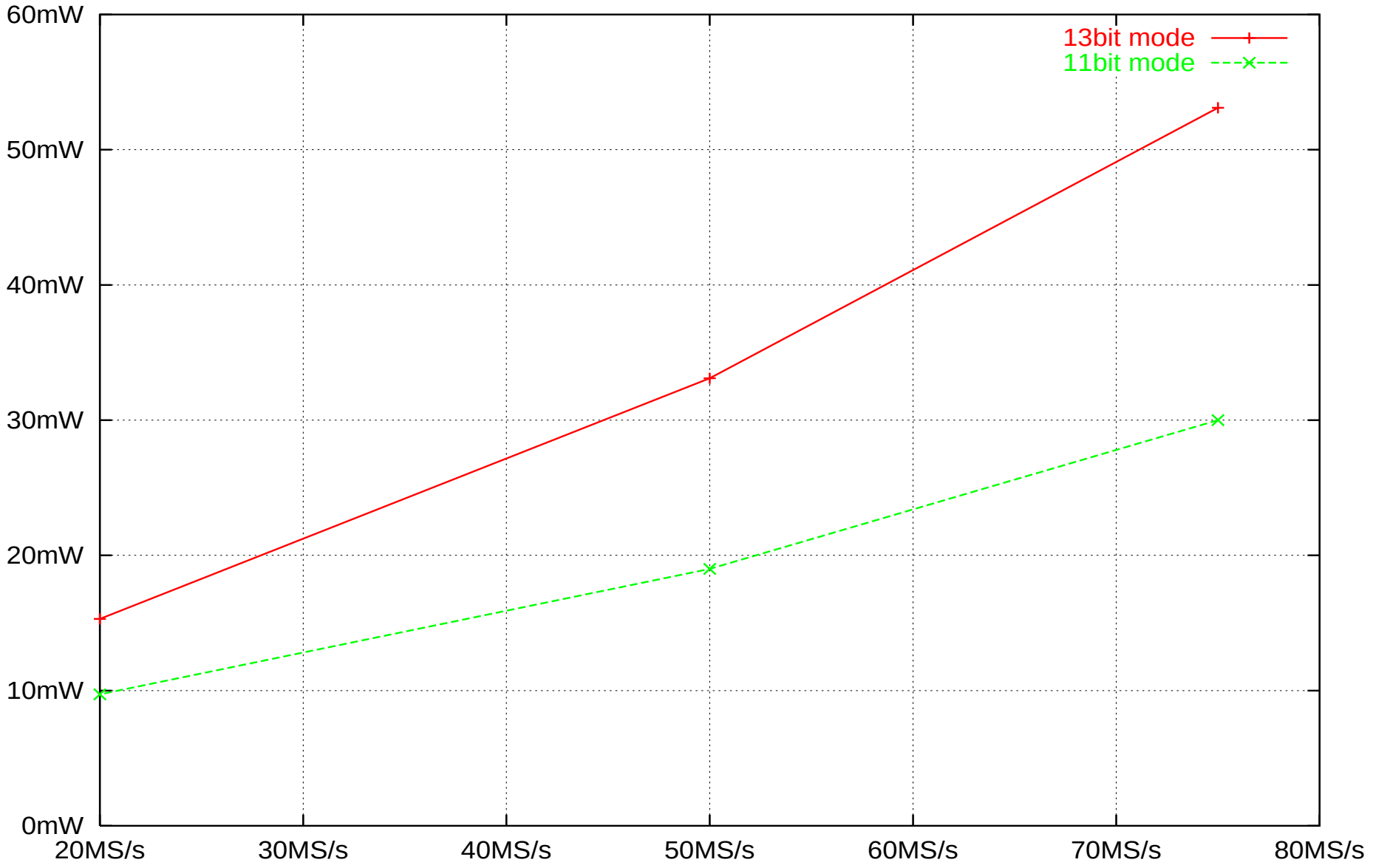
ENOB
vs. f_{signal}

@75MS/s



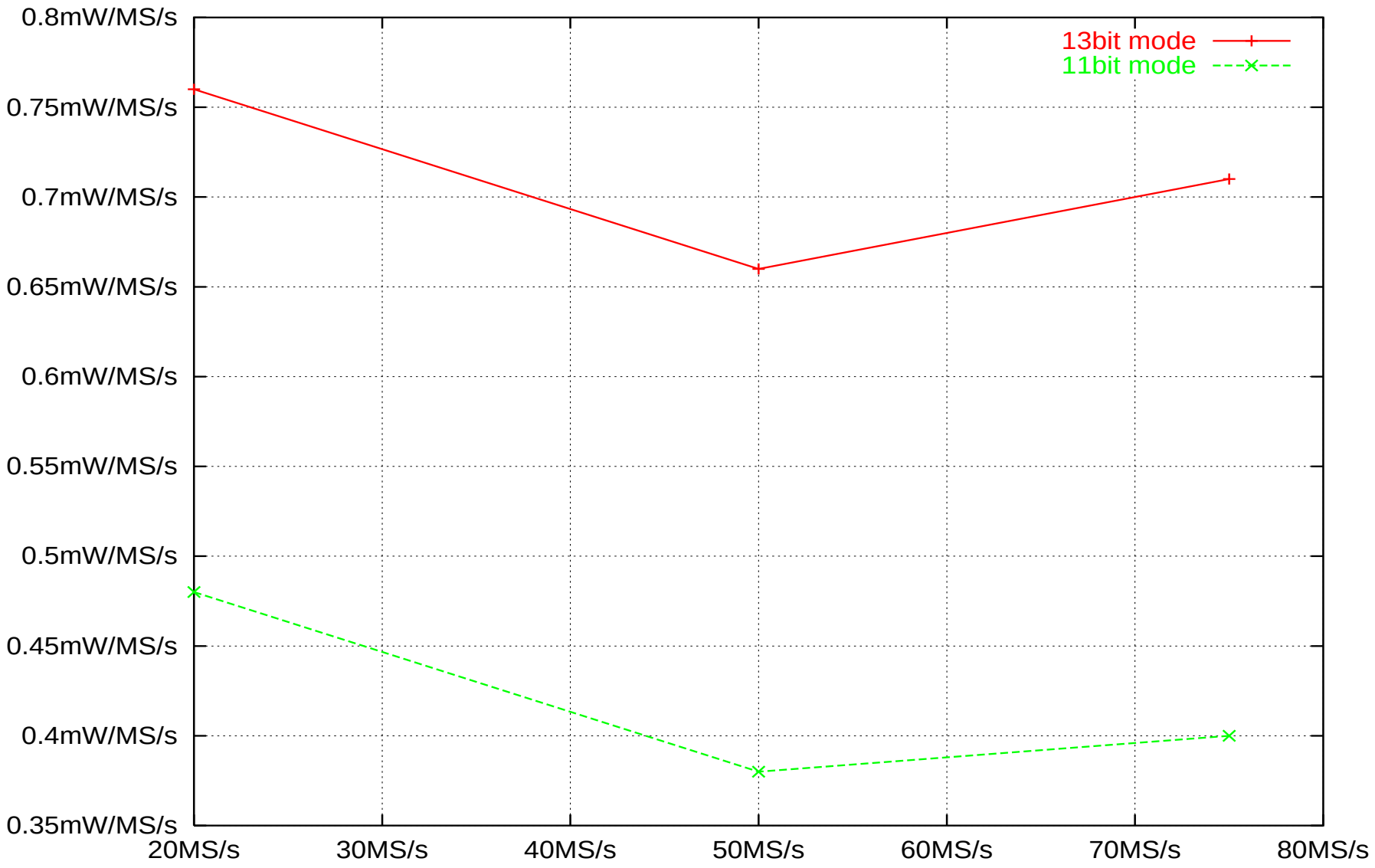
Jitter-problem: ~60ps RMS !
due to timing problem, requiring an unintended clocking of the testchip

Power vs. Sample frequency



Condition: const. ENOB

Power / MS/s versus Sample frequency



Suited for a wide range of applications
through highly scalable analog circuitry

ADS5273

12bit 70MS/s ADC, 8 channel, Serializer

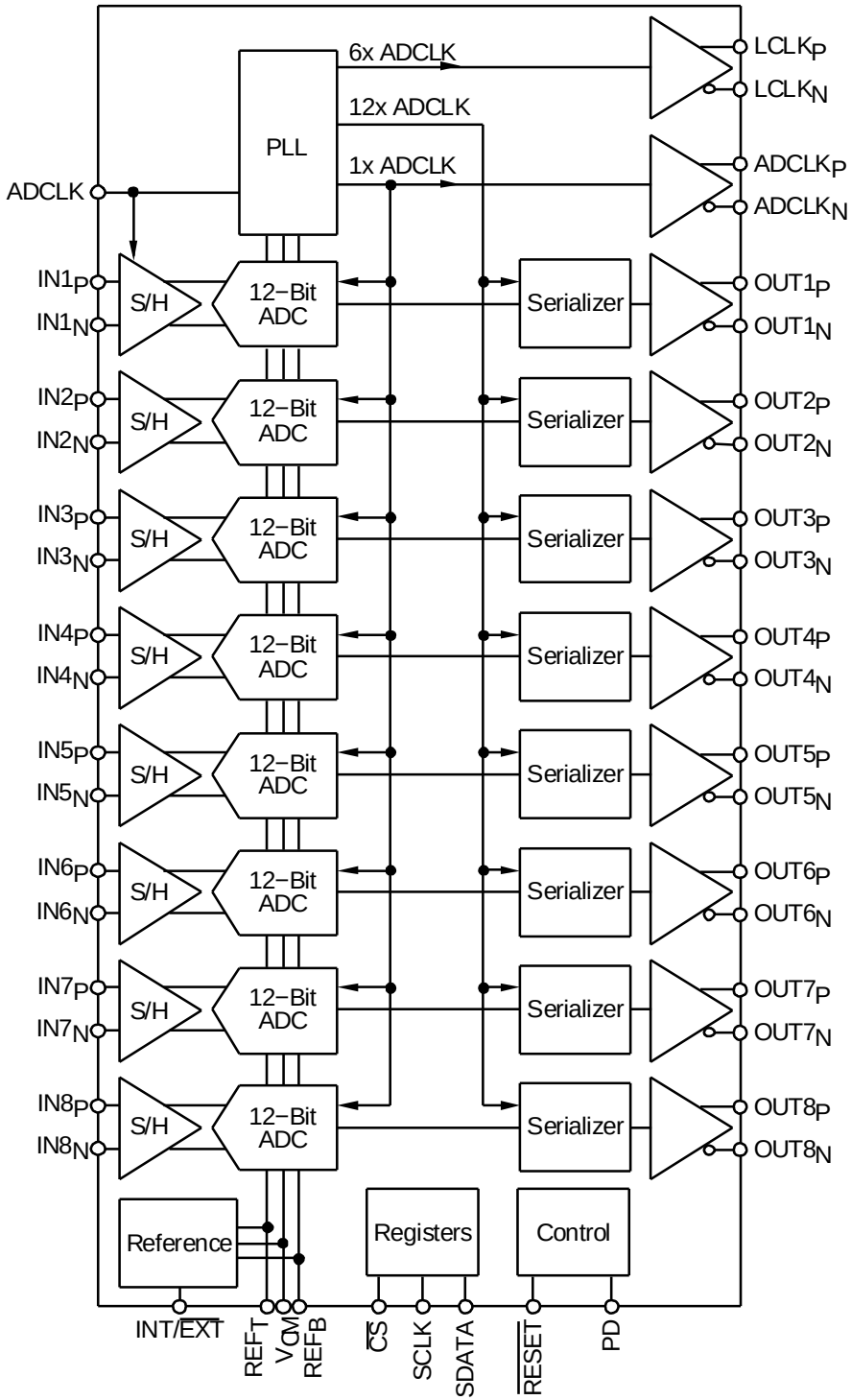
Single ADC channel:100mW (analog)

Proposed ADC:

Single ADC: 53mW

8 channels: possible

Serializer: possible



Conclusion

	13bit-mode	11bit-mode
POWER @ 50MS/s	33mW	19mW
POWER @75MS/s	53mW	30mW
ENOB (low f_{signal})	10.9bit	10.0bit
Input range	+/- 1V	+/- 1V
Supply voltage	1.8V	1.8V

To do:

- Remove timing problem (jitter !) for useful high frequency behavior
- Extend Sample frequency range up to 100MS/s
- Increase 13bit-mode-resolution