

# **TDC readout prototype: test from measurements**

Authors:

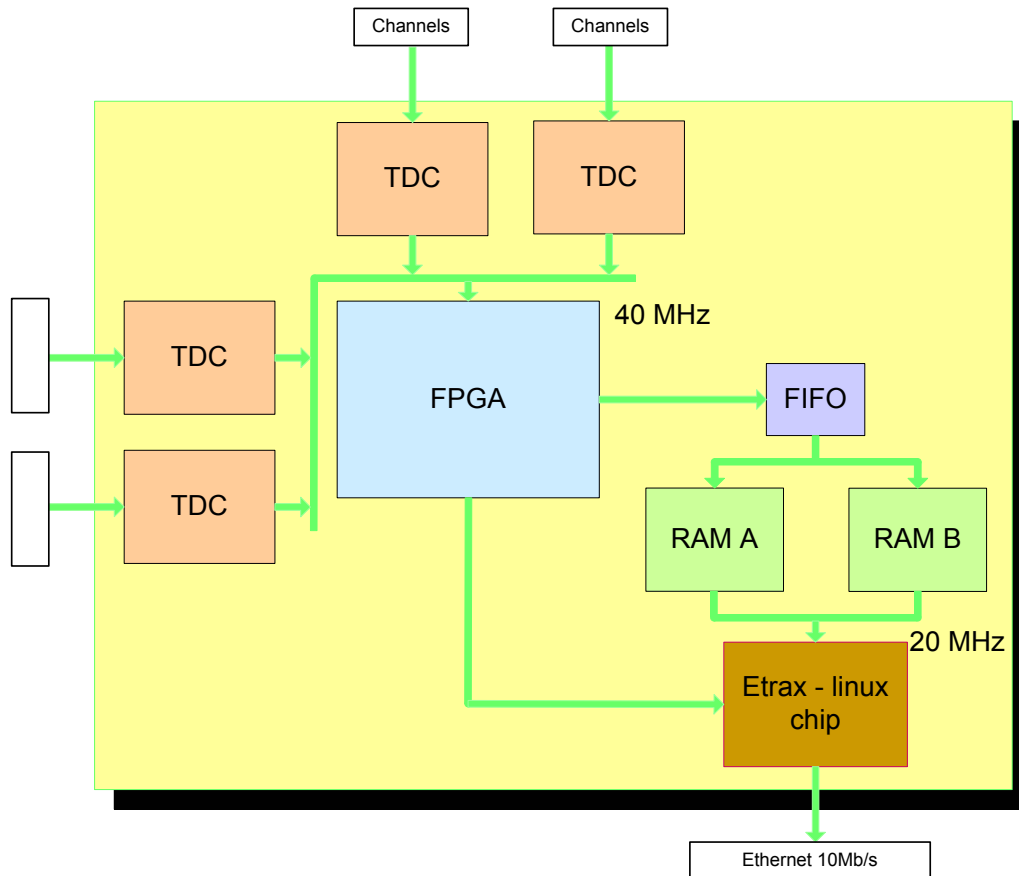
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# TDC readout prototype: test from measurements

- Description of TDC board:



- Board destination:

- HADES – RPC detector (EU FP6 construction contract nr 515876).

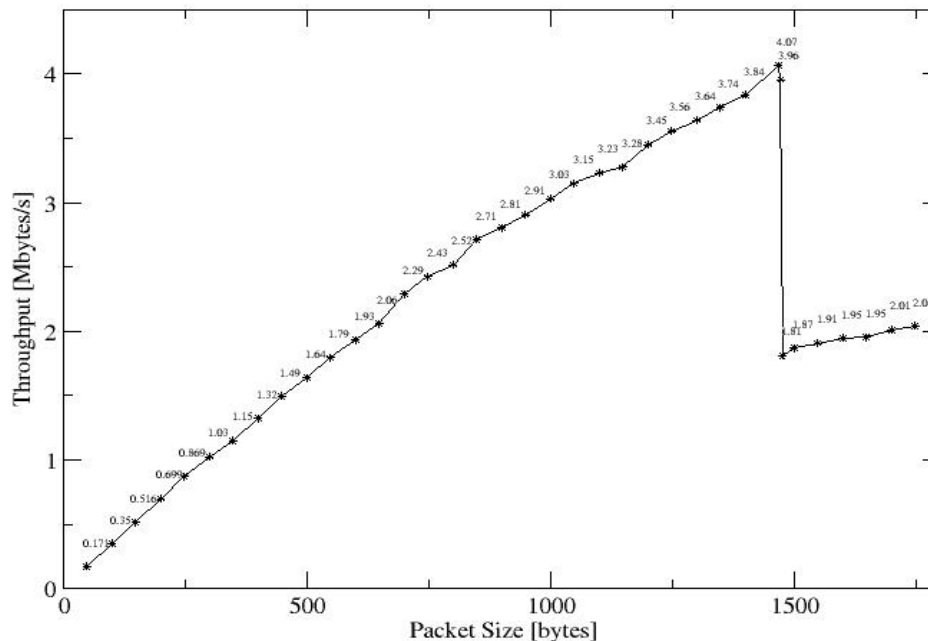
- Main parts of board

- TDC,
- FPGA,
- ETRAX,
- RAM's and FIFO,
- Etrax.

# TDC readout prototype: test from measurements

- Speed measurements:

Performance of Axis Etrax Chip in UDP transfer

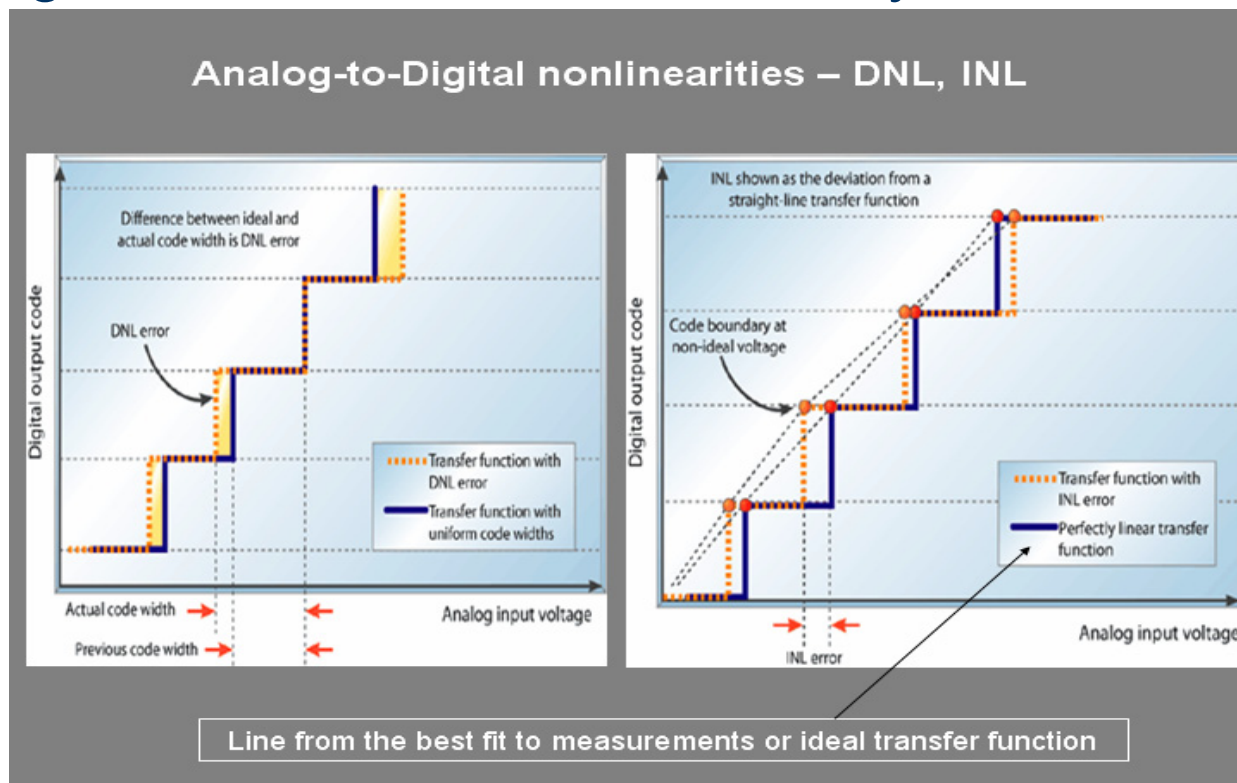


Maximum speed transfer through ethernet: 4,07 MB/s

Maximum FPGA frequency estimated by Synplify Pro: 87,8 MHz

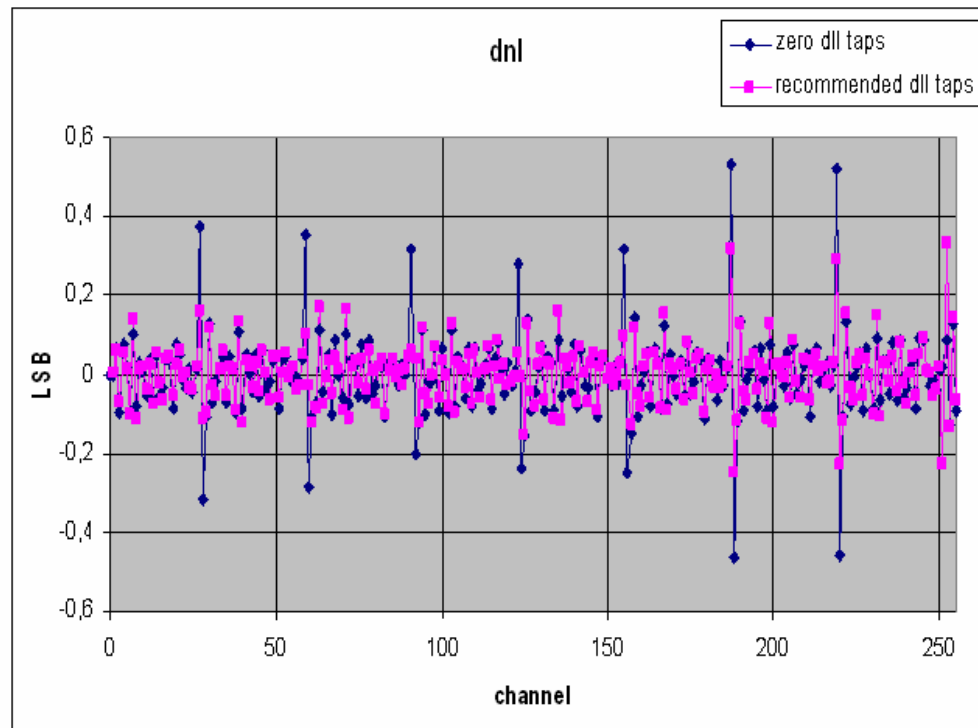
# TDC readout prototype: test from measurements

- Integral and differential nonlinearity



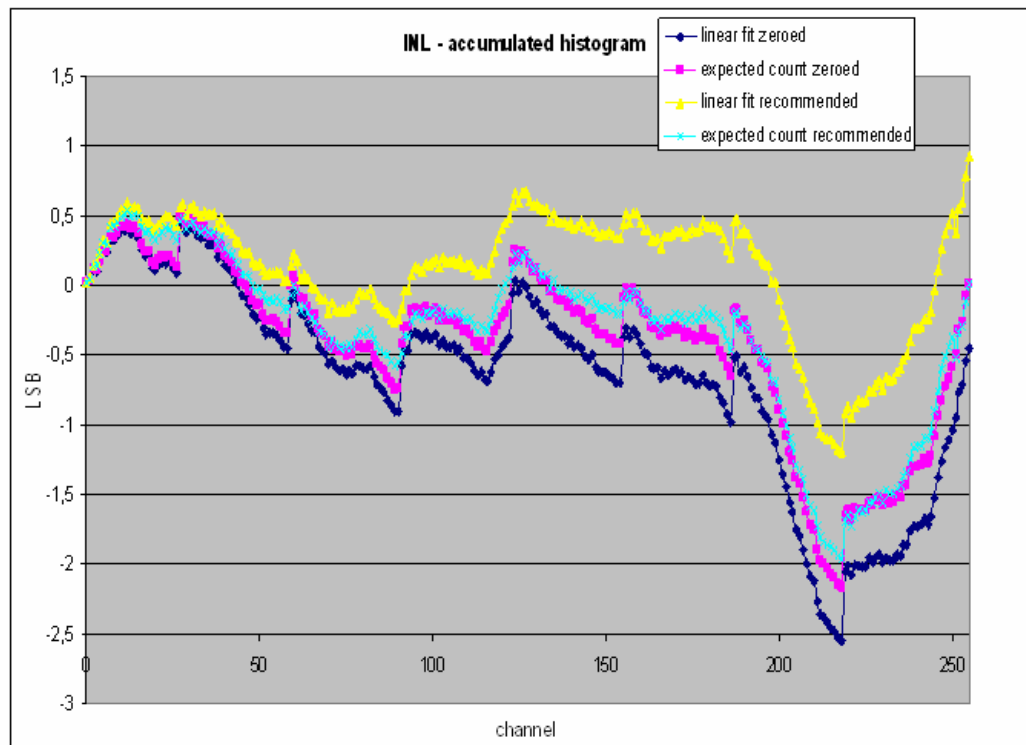
# TDC readout prototype: test from measurements

- Integral and differential nonlinearity



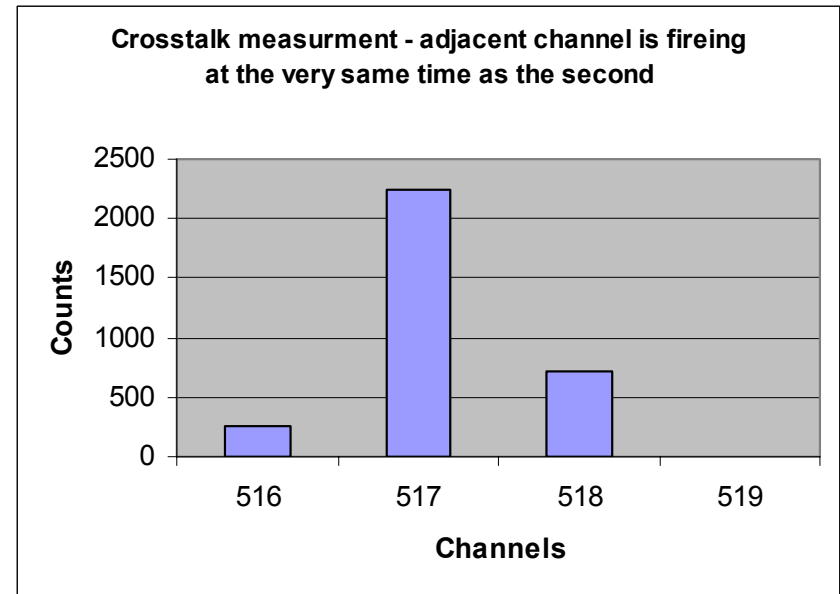
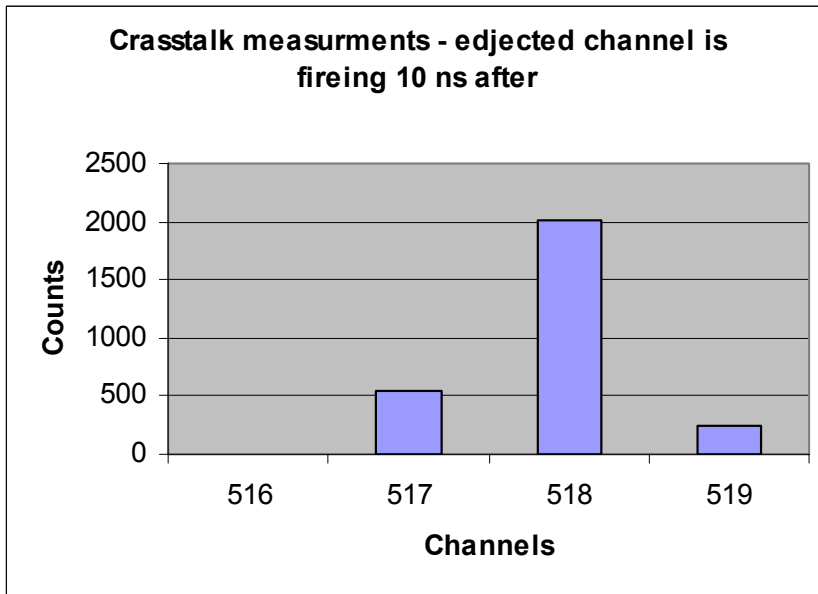
# TDC readout prototype: test from measurements

- Integral and differential nonlinearity



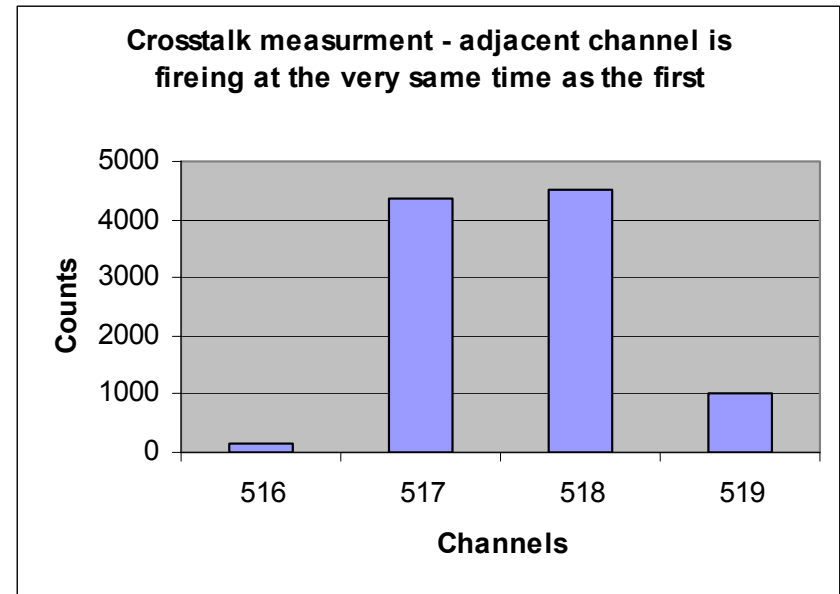
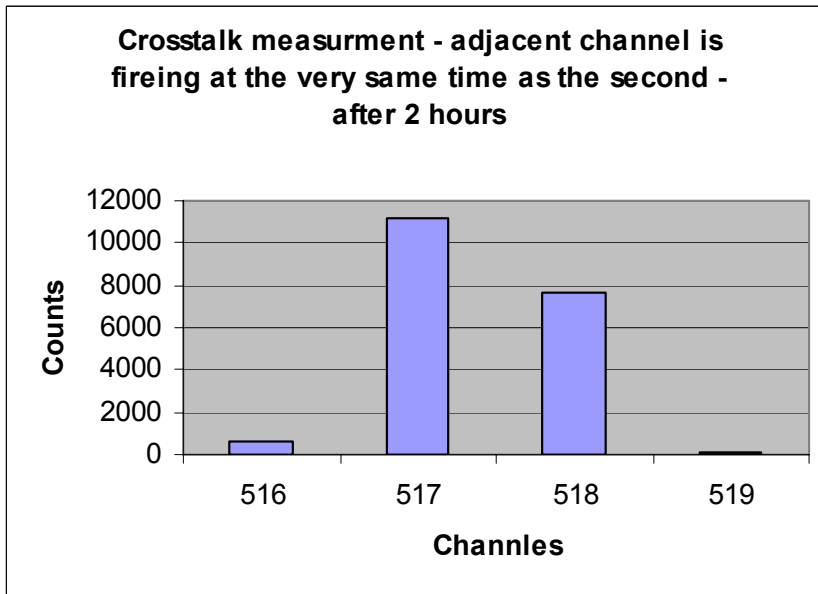
# TDC readout prototype: test from measurements

- Crosstalk



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# TDC readout prototype: test from measurements

- Summation
  - System is during tests now and it is operating,
  - In November there will be RPC detector test and our board,
  - Designed board is flexible.