Time measurements with the TDCs board

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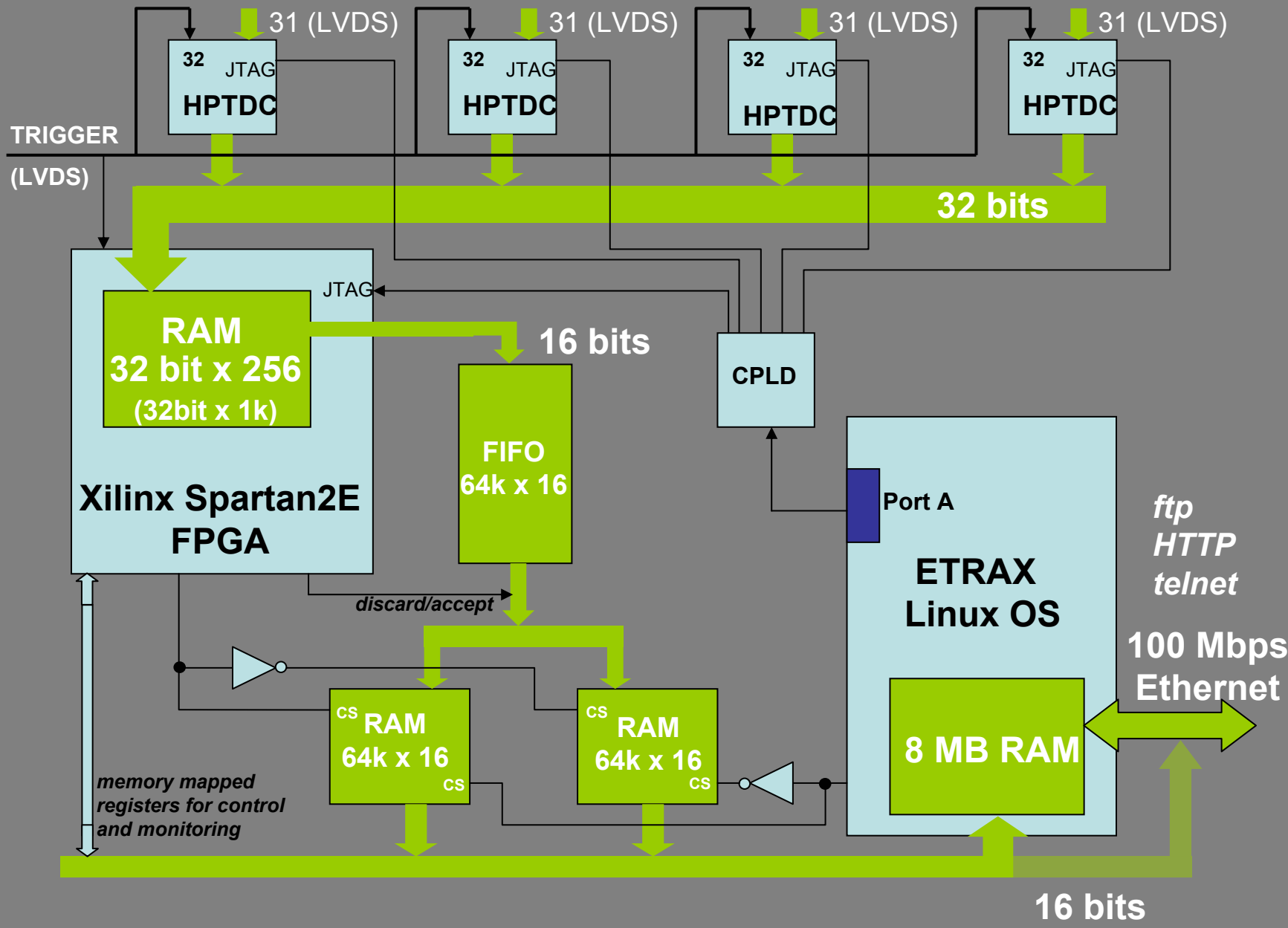
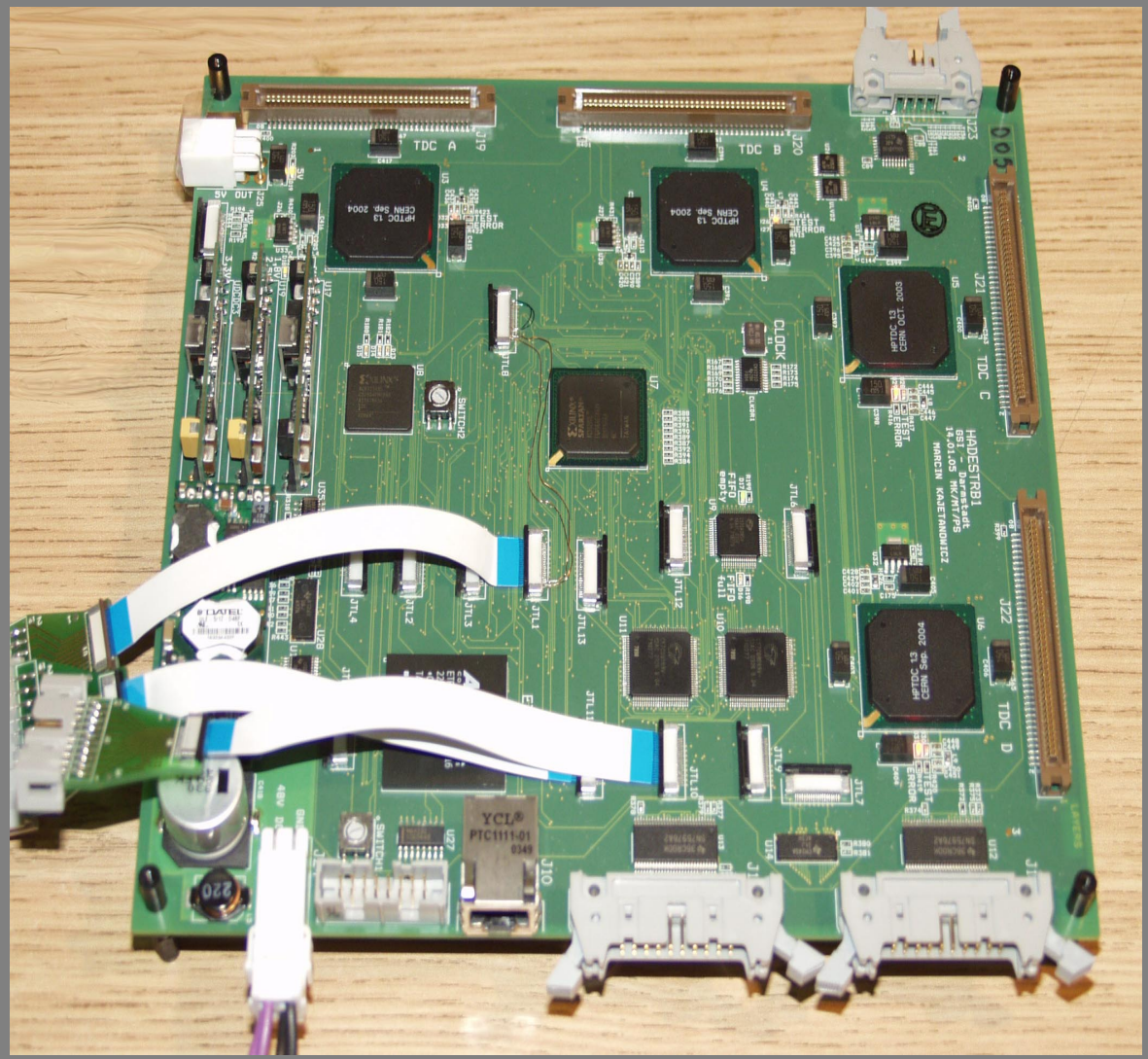
Data flow from the TDCs to the external world



Prototype board



Architecture of HPTDC

2. Architecture

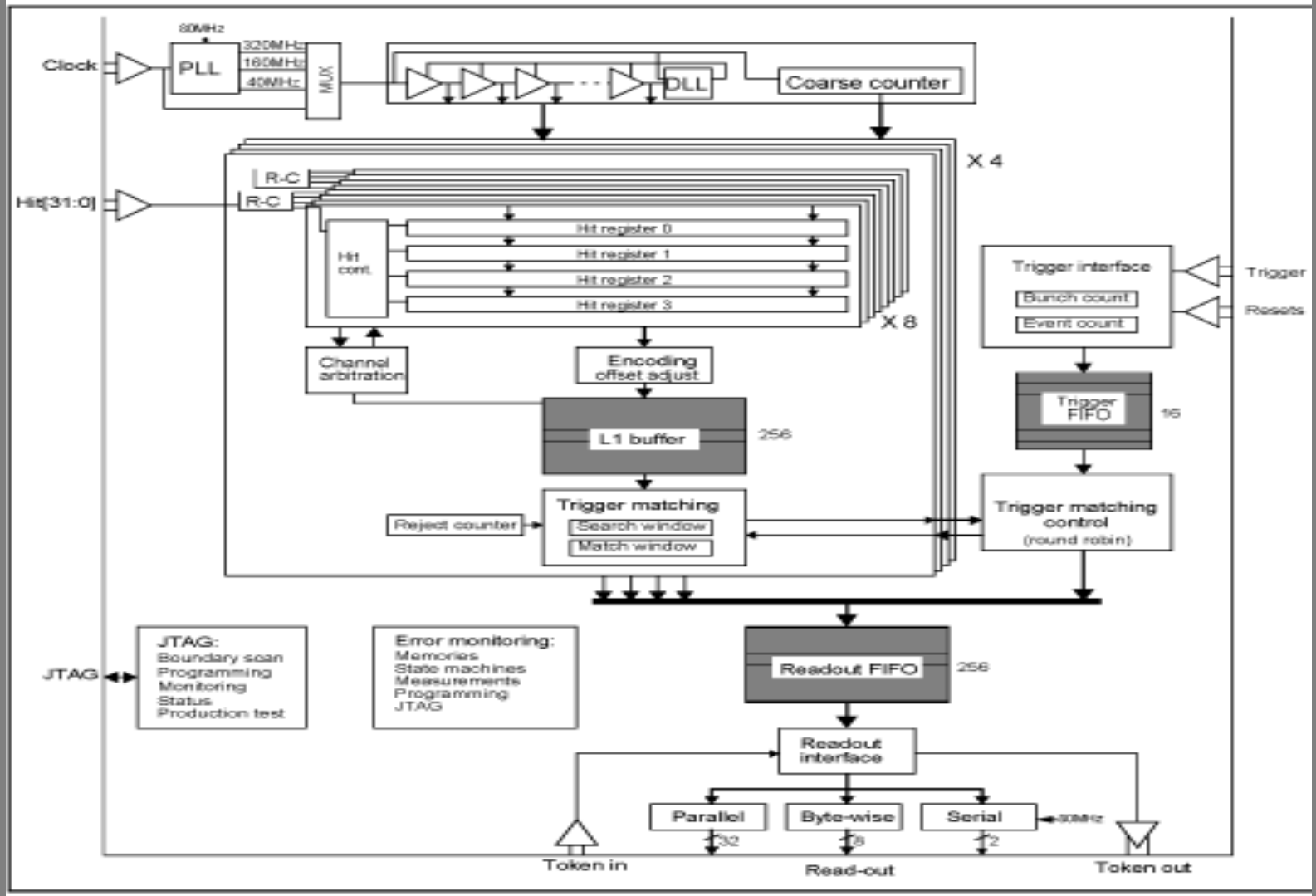
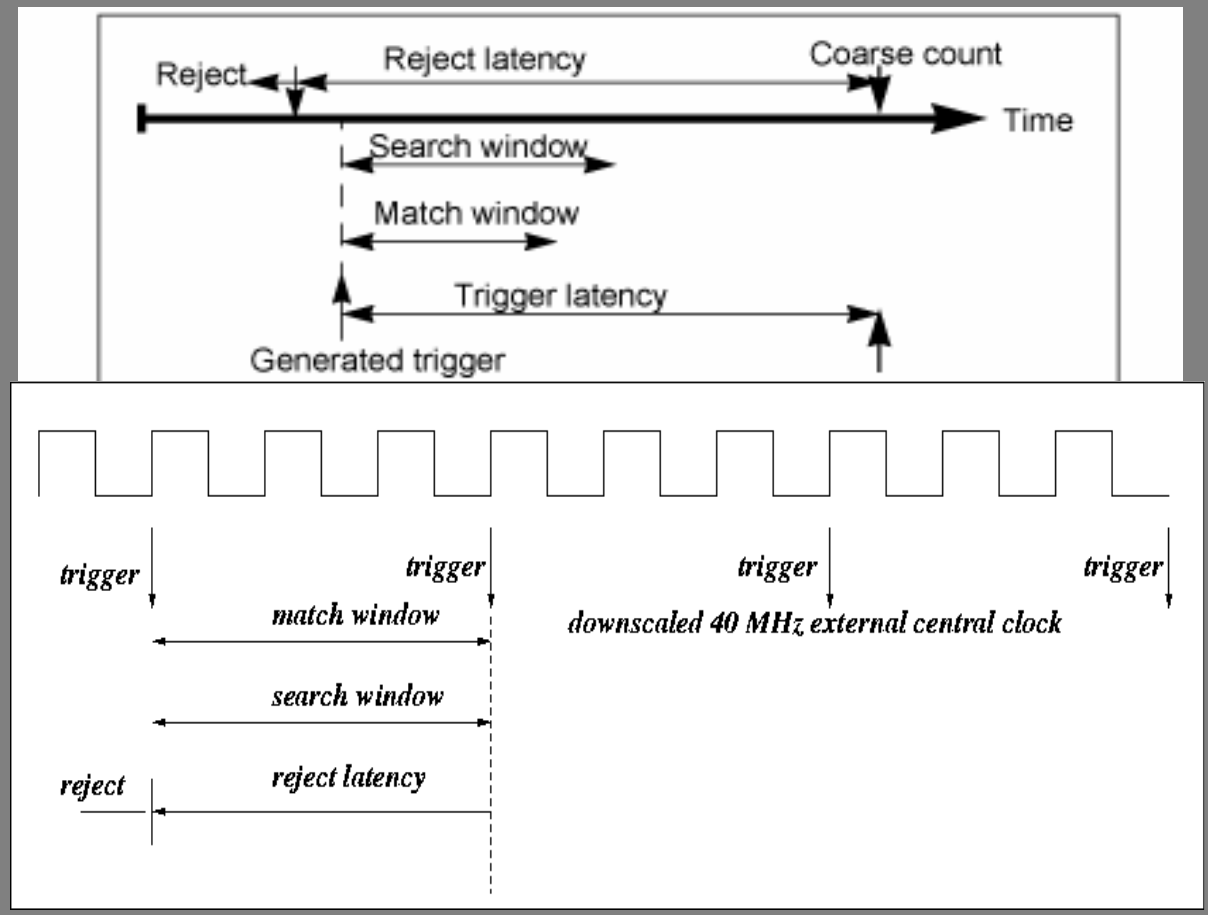
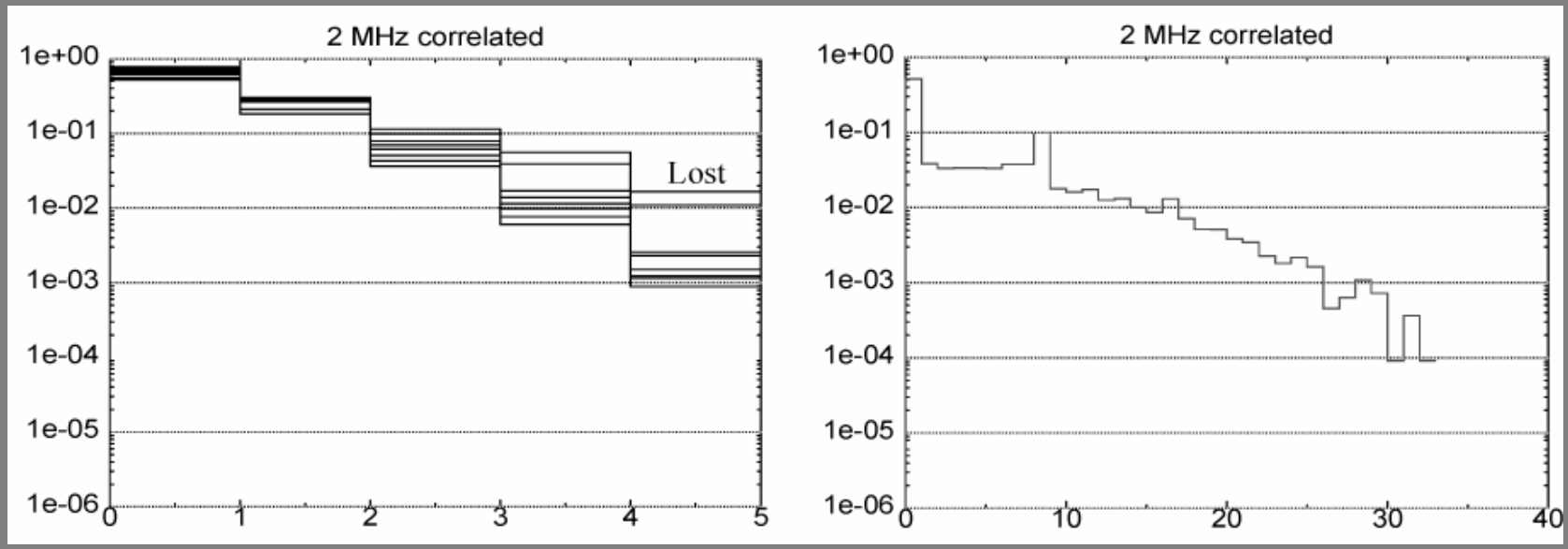


Fig. 1 Architecture of HPTDC.

Trigger matching of HPTDC



High speed operation of HPTDC



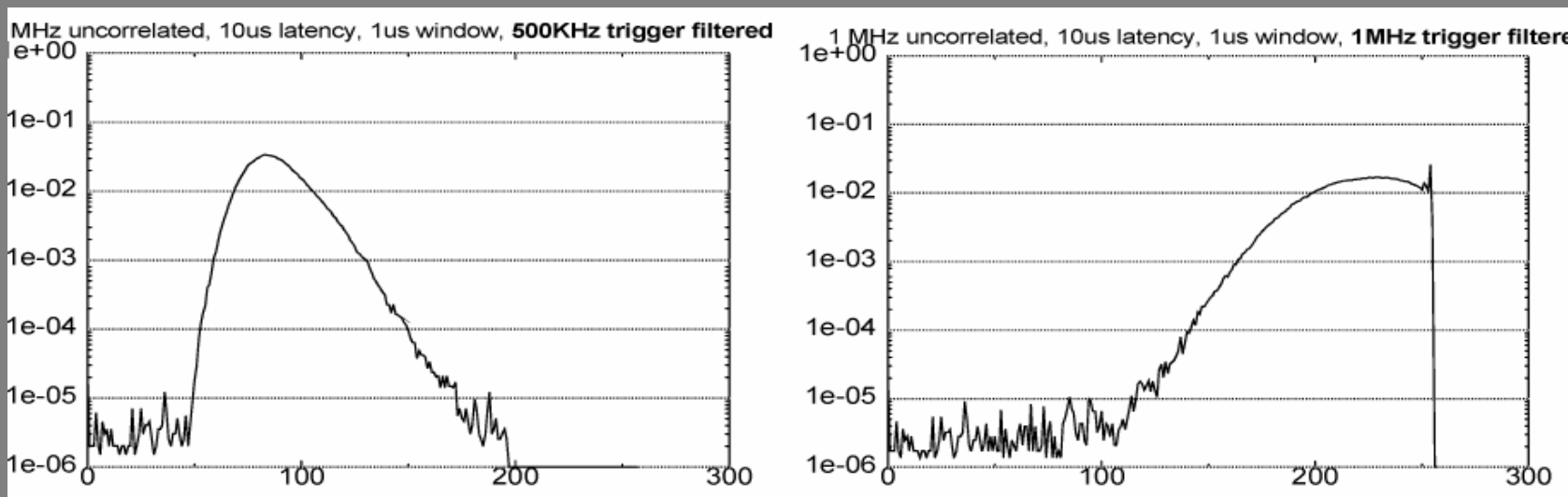
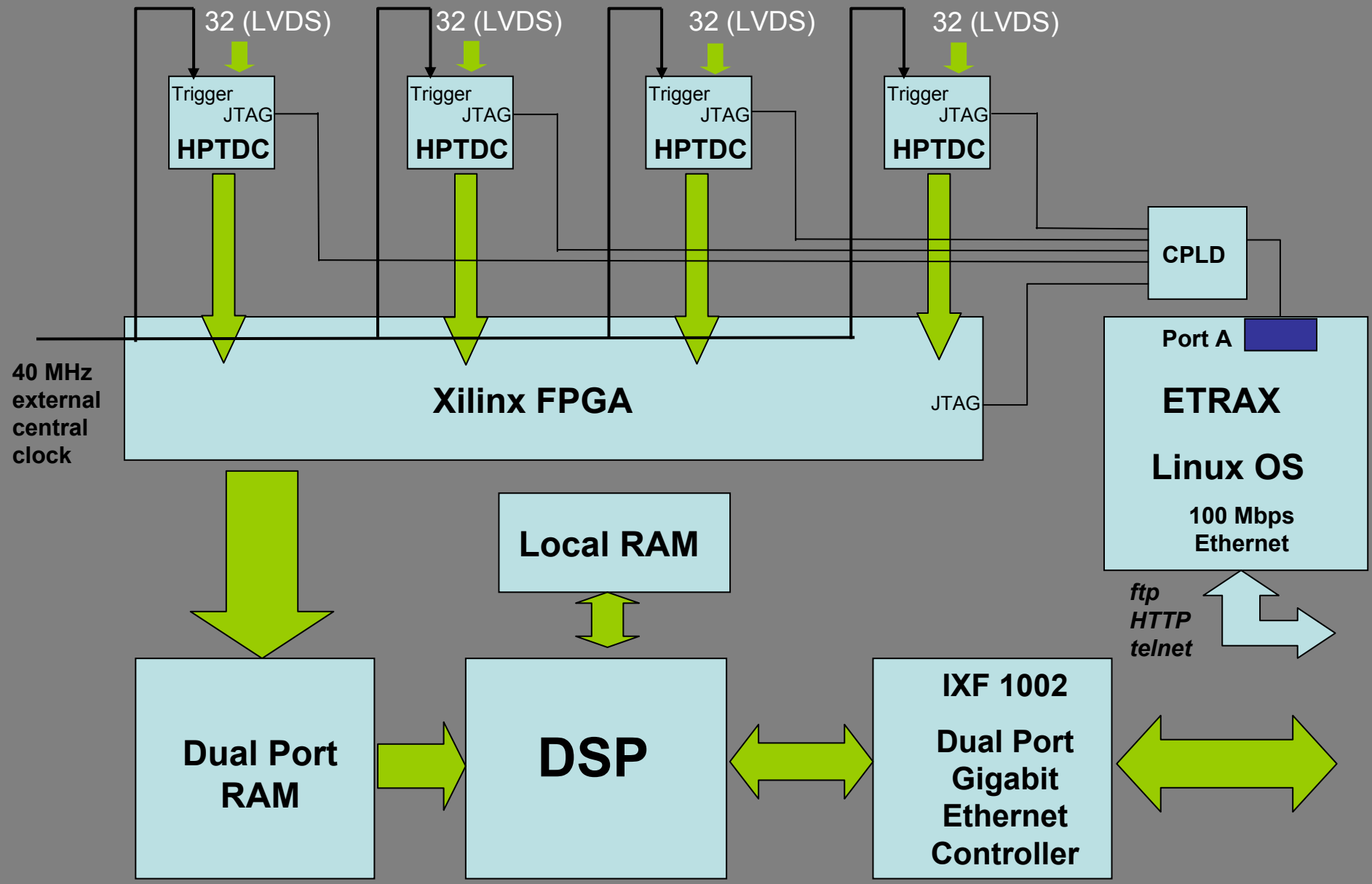


Fig. 57 L1 buffer occupancy with central trigger limitations

Modified architecture of the TDC board for PANDA



Summary

- Prototype board is currently under calibration tests (- see next talk from M. Palka)
- HPTDC are in mass production for the LHC experiments and will have long lasting support from CERN for the comming years
- Board is beeing integrated with the HADES trigger bus for the HADES RPC readout
  - With an intermediate upgrade – DSP + fast optical links - the board is to be used for the HADES LVL2 trigger
- With proposed upgrade – DSP + Gigabit Ethernet + modifications to the trigger logic – the board can be considered as candidate for the PANDA's MDC readout