

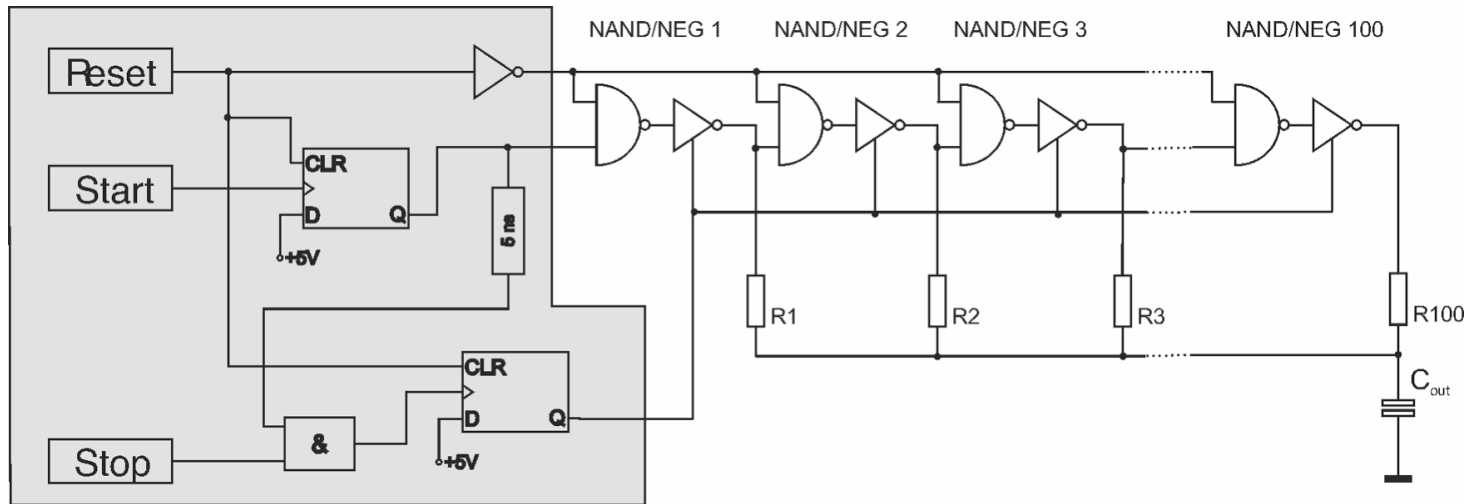
# **TAC based TDC ASIC's**

# Overview



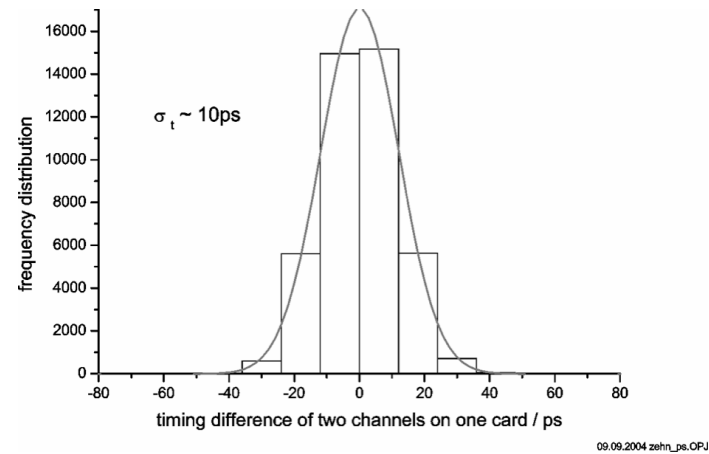
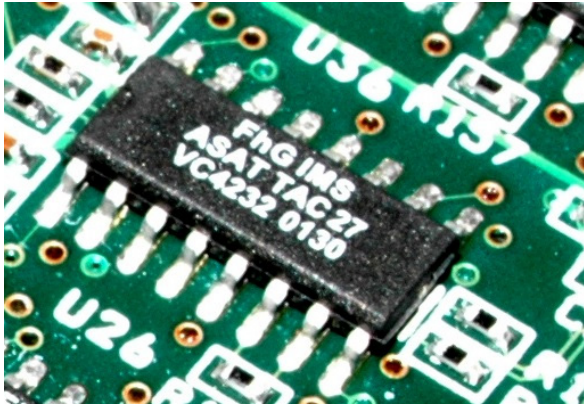
- The TAC core
- Experience from existing implementations
- Benefits and drawbacks
- A TAC based TDC concept
- Design challenges
- Open Questions

# The TAC Core



- Digital delay chain
- Distributed RC-Network
- Voltage on  $C_{out}$  increases linear with time

# Existing TAC-Core Implementation



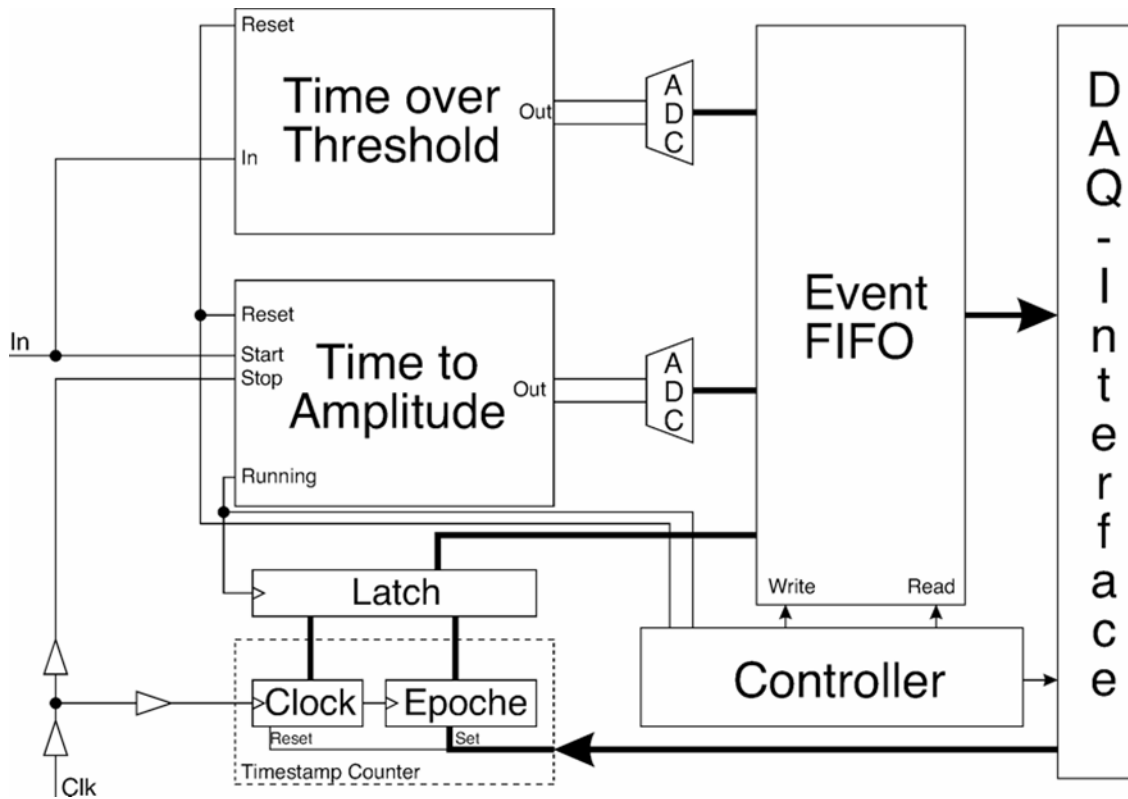
- TAC-ASIC by GSI and FhG IMS in  $0.8\mu\text{m}$  CMOS
- Used in FOPI RPC Readout
- TAC core implemented in ASIC, separate ADC and readout
- Time resolution better than 10 ps

# Benefits and Drawbacks



- Benefits
  - Time resolution not limited by delay of a digital element
  - Time resolution below 10 ps possible
  - Zero power consumption in standby mode
- Drawbacks
  - Calibration necessary
  - Deadtime during ramping and readout

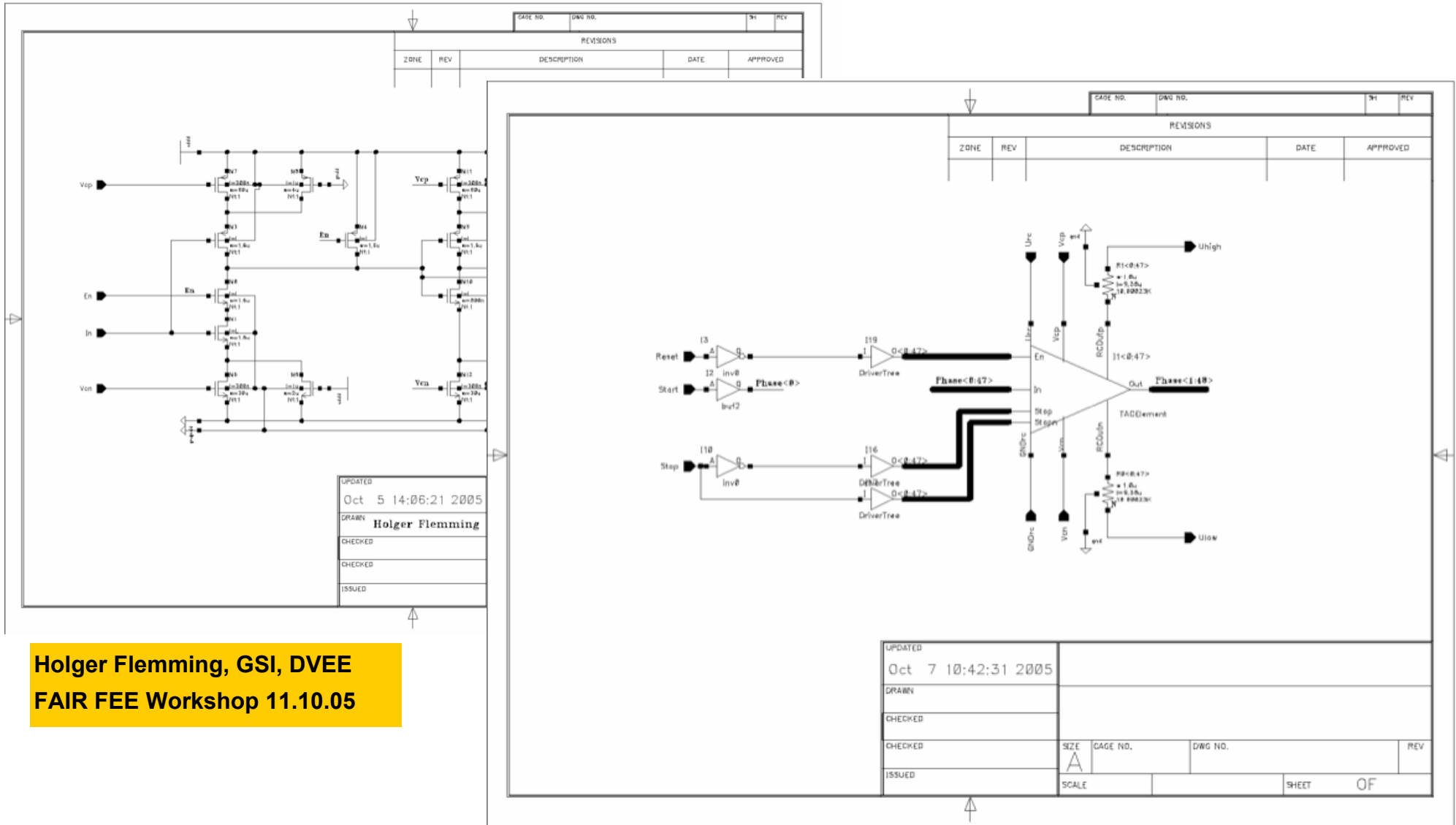
# TAC based TDC concept



- Time over Threshold measurement for signal amplitude determination
- Integrating TAC and ADC for converting time to digital
- Timestamp unit for Eventmarking
- Integrated Interface to DAQ

# First Testchip under design

- Migration of TAC Core to 0,18μm CMOS

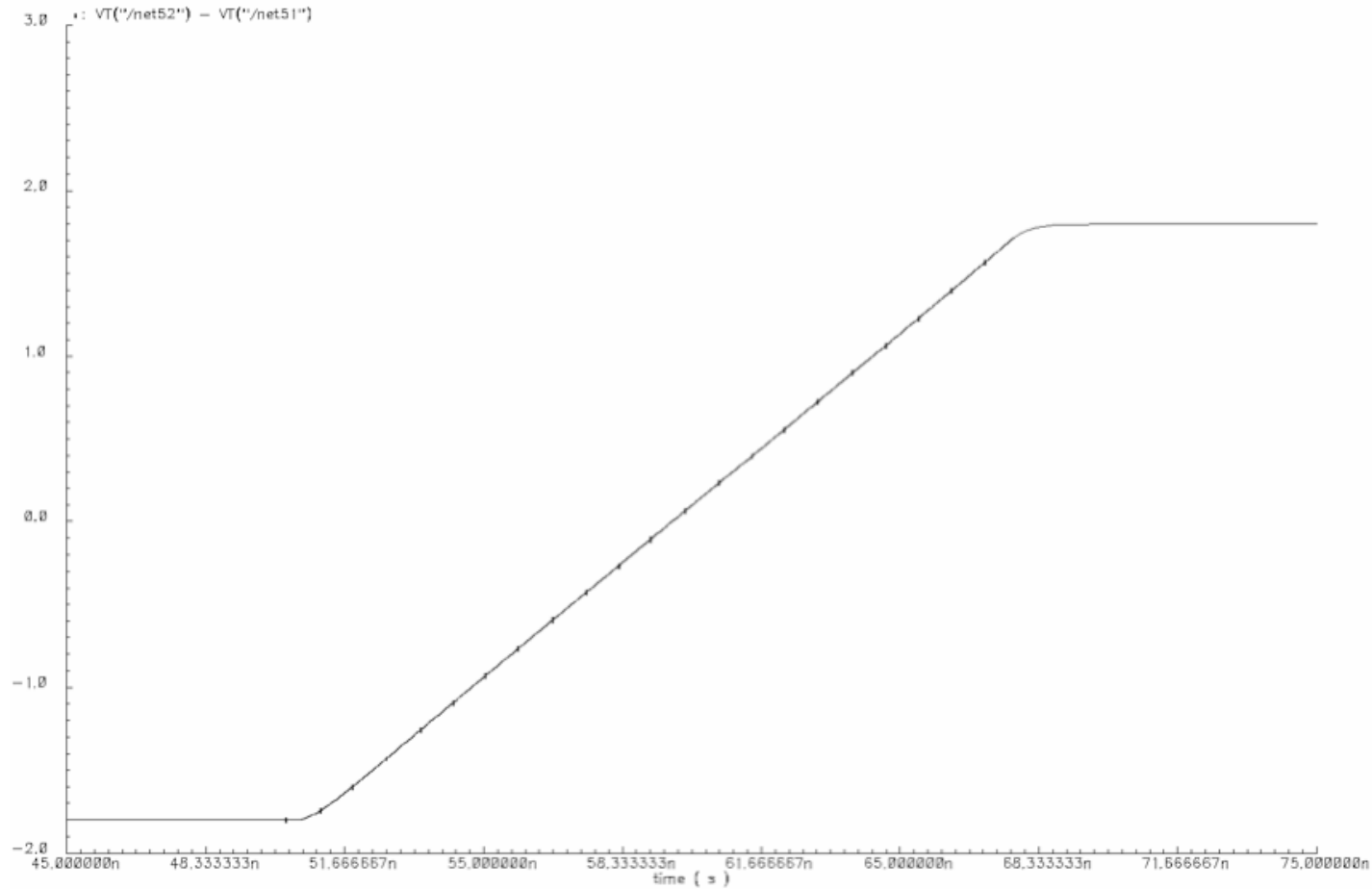


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# Simulation of First Testchip

VF\_grundtest1 TAUTestbench.schematic : Oct 11 09:55:27 2005

Transient Response



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# Design challenges

- TAC
  - migration to a later technology
  - power decoupling of TAC Cores on the same die to realize a multi channel chip
- ADC
  - 12 bit resolution
  - $\pm 1$  V input
  - single shot
  - 1  $\mu$ s converting time
- DAQ Interface
  - decoupling of analog components (TAC and ADC) from digital readout

# Open Questions

- Open questions concerning both, TAC and DLL solution
  - TDC resolution required?
  - Single / double hit resolution?
  - (double hit only flagged?)
  - Integration Level (Geometry)?
  - Event rate to cope with (100 kHz)?
  - Discriminator specs (time over threshold)?
    - min. and max. signal length
    - double hit resolution
  - Temperature?
  - Radiationhardness?
  - Interfaces?