



N-XYTER

The First Dedicated Neutron Detector Readout ASIC

DETNI

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DETNI Detectors for Neutron Instrumentation

Develop and prototype
three different advanced area sensitive detector systems
within FP-6

Gd/Si Micro Strip

Gd/CsI MSGC

CASCADE GEM

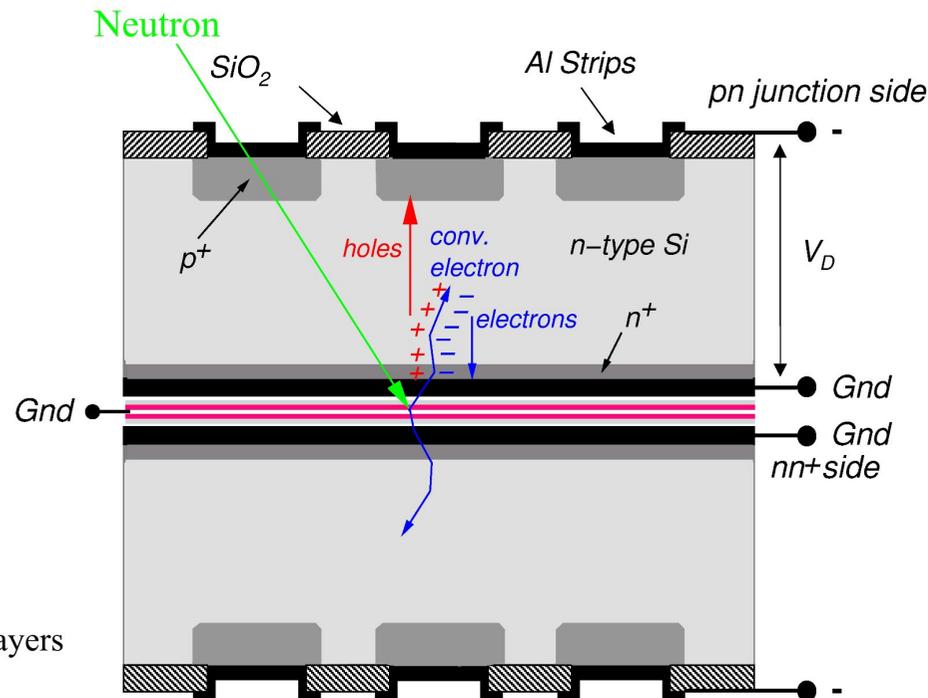
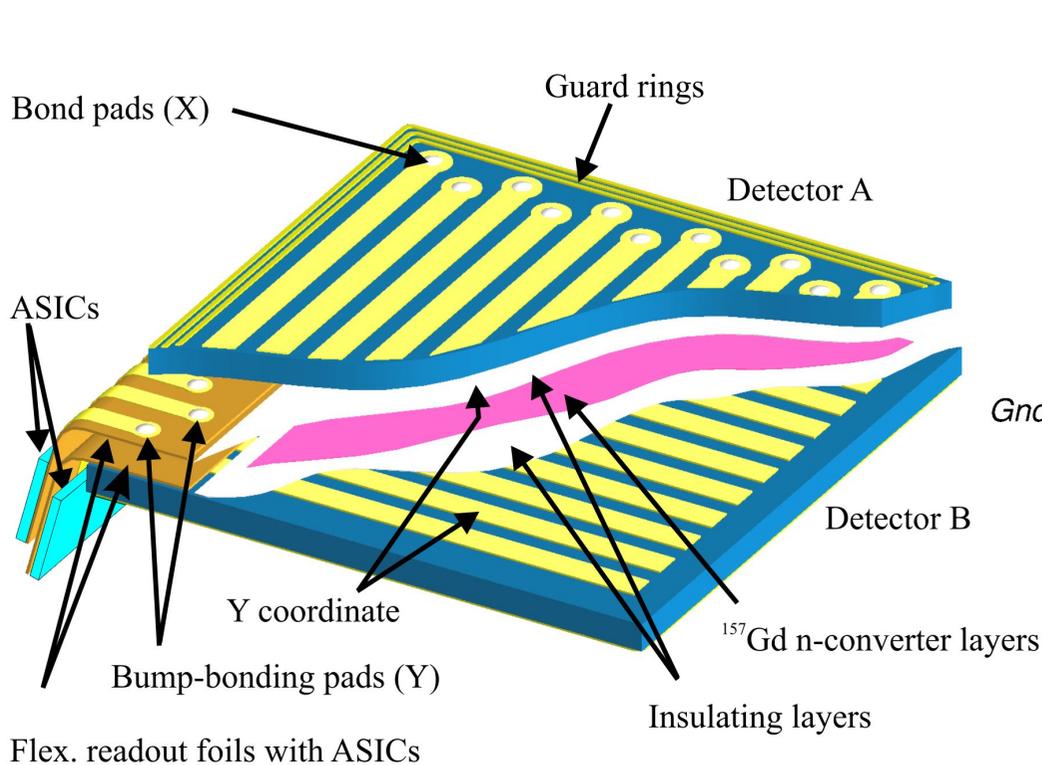
for

very high rates (10^8 Hz)
mm and sub mm resolution
highest possible detection efficiency

—

as a supplement:
develop the first dedicated
Neutron detector readout ASIC
universal to these detectors

A $^{157}\text{Gd}/\text{Si}$ Microstrip Detector

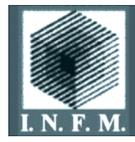


- Size 51 mm x 51 mm
- No. of strips 640
- Pitch 80 μm
- $\delta x \leq 50 - 100 \mu\text{m}$
- E_s 29 - 250 keV

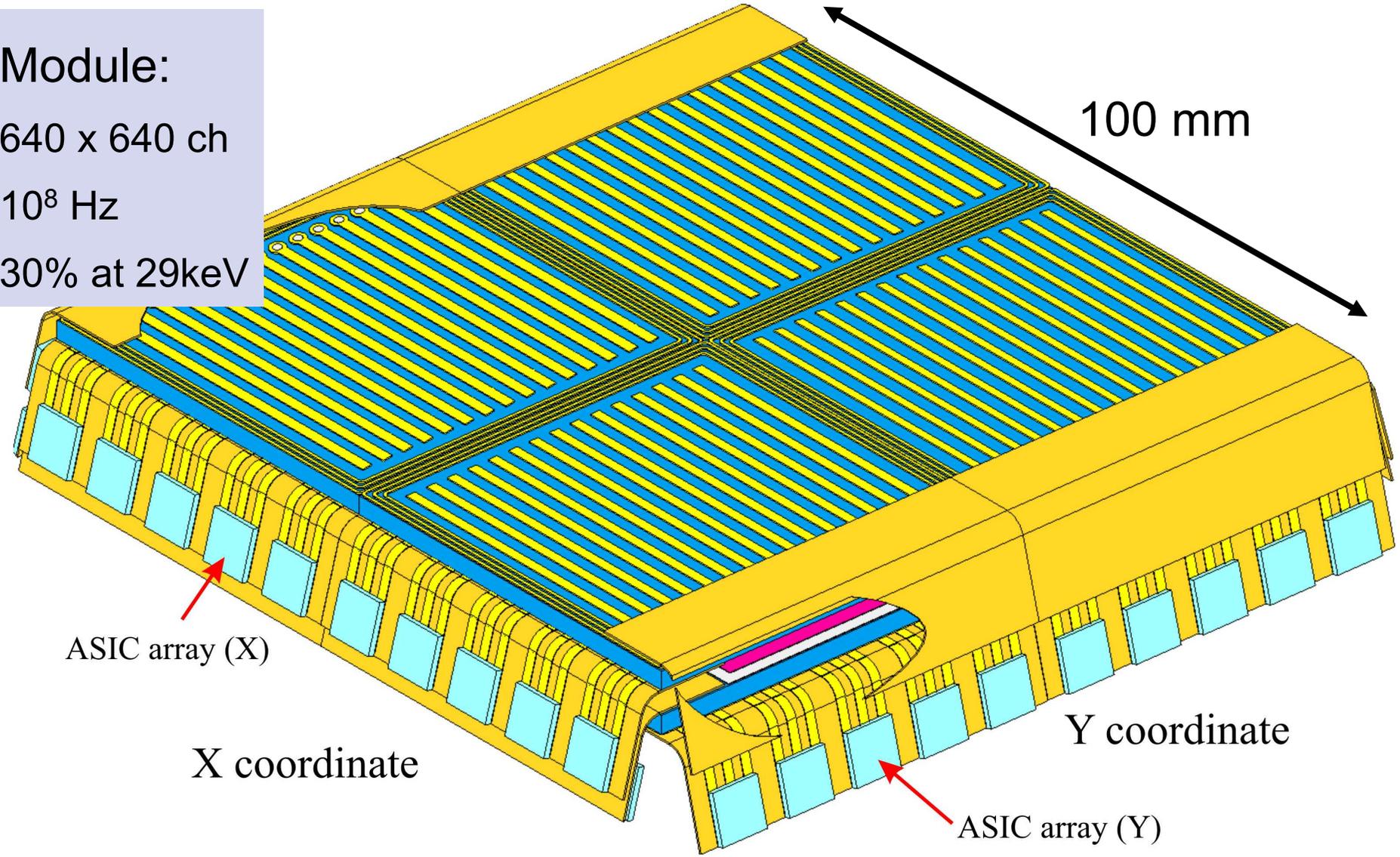
- $E_{th}(5\sigma)$ 10 keV
- ENC 550 e^- (20 - 30 pF)
- cps (global) 2.5×10^7
- cps/strip 7.5×10^4
- δT (x/y) 4 ns



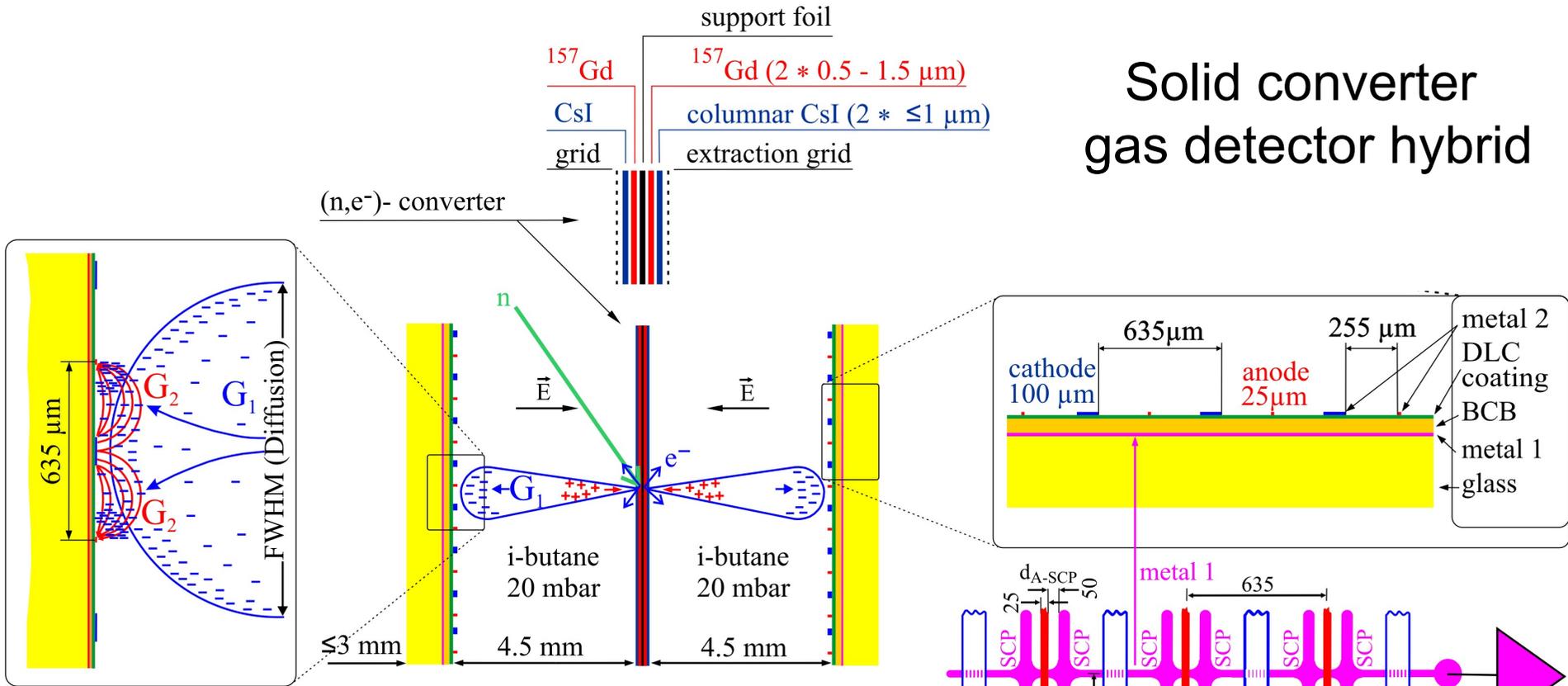
A $^{157}\text{Gd}/\text{Si}$ Microstrip Detector Module



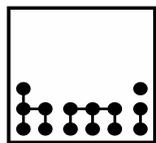
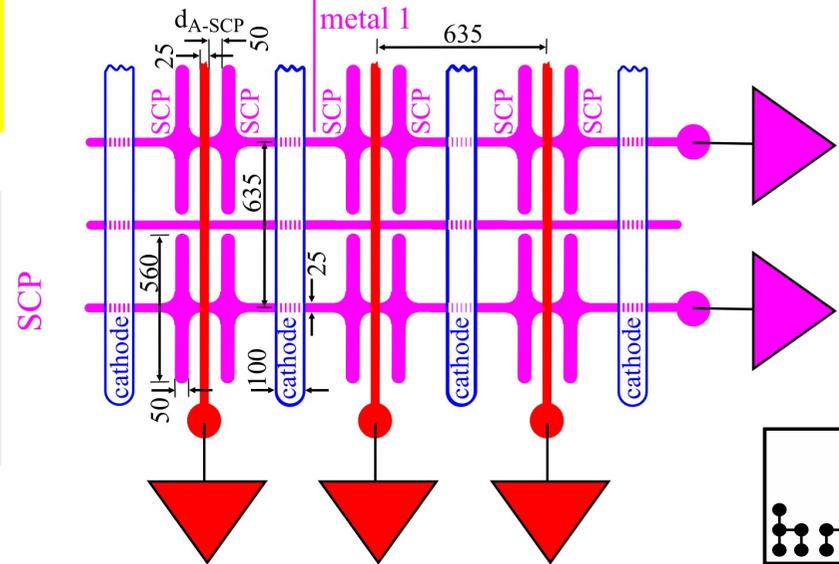
Module:
640 x 640 ch
 10^8 Hz
30% at 29keV



B $^{157}\text{Gd}/\text{CsI}$ Low-pressure MSGC Detector



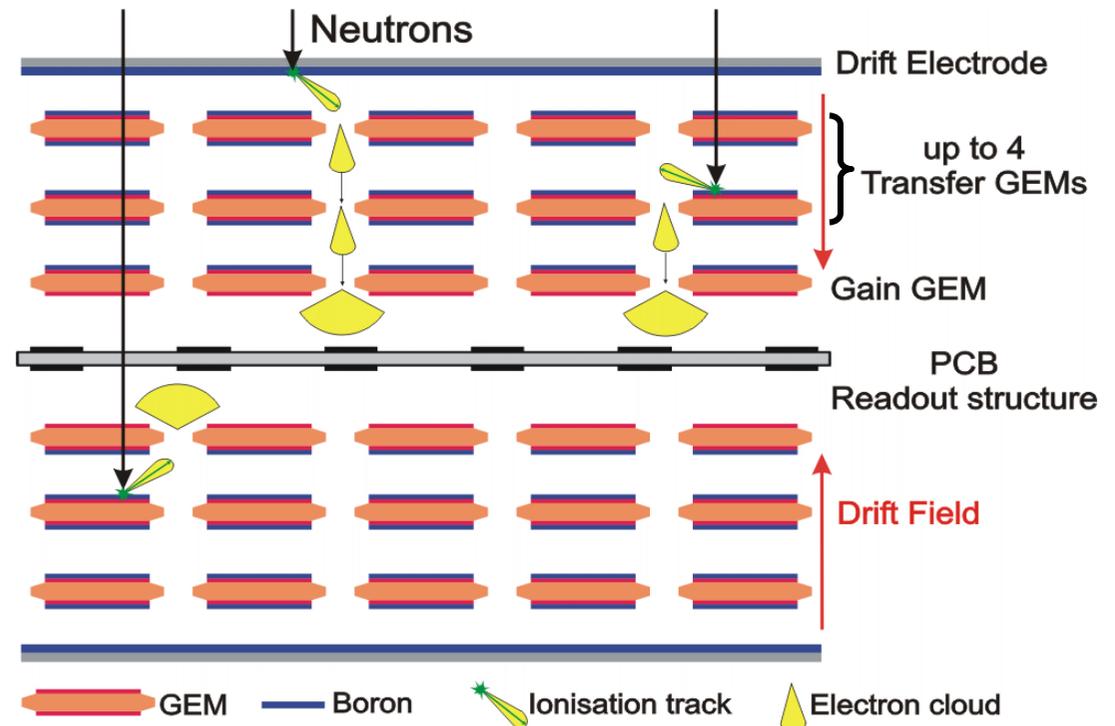
Each Coordinate:
 400 channels on 250mm
 event multiplicity 3.5 strips
 Maximum rate per channel: 950kHz



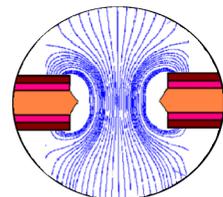
CASCADE: Multiple Boron Layers on GEMs



- GEMs can be operated to be transparent for charges!
→ they can be cascaded!
- Each one can carry two Boron layers
- Last one operated as amplifier

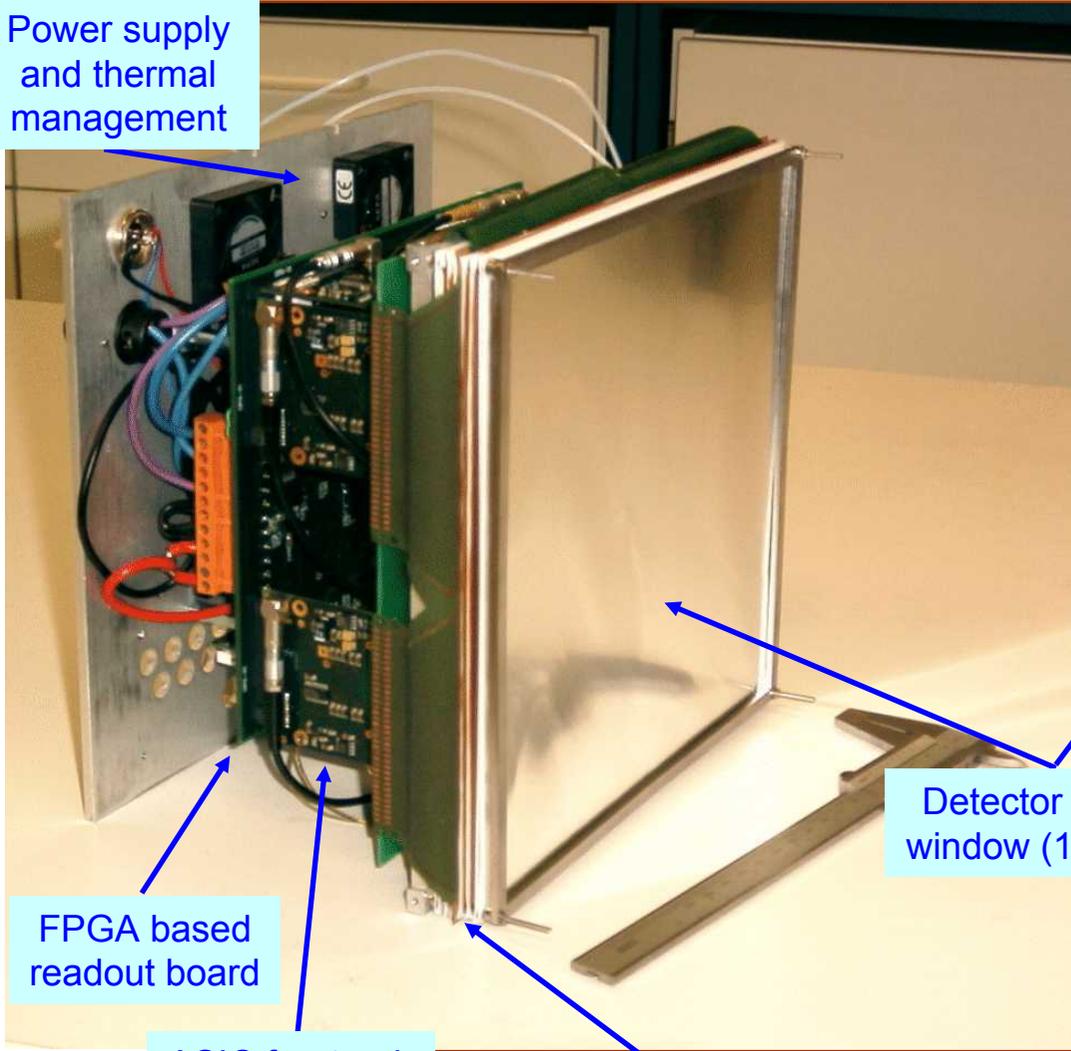


Cumulate 5% single layer detection efficiency to give 50% for thermal neutrons (1.8Å) → need 10 cascaded GEM-foils



Assembled 2D-200 Detector: the neutron „GameCube“ *

Power supply and thermal management

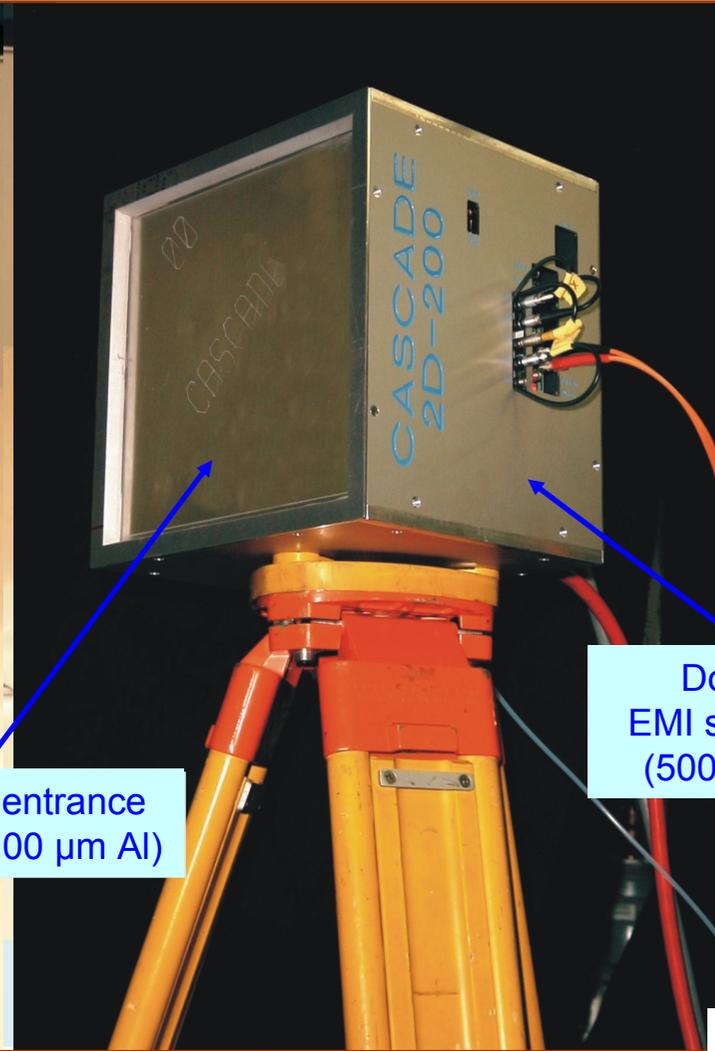


FPGA based readout board

ASIC frontend-electronic

Detector entrance window (100 μm Al)

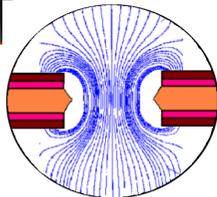
GEM-foils coated with ^{10}B and 2D readout structure



Double EMI shielding (500 μm Al)

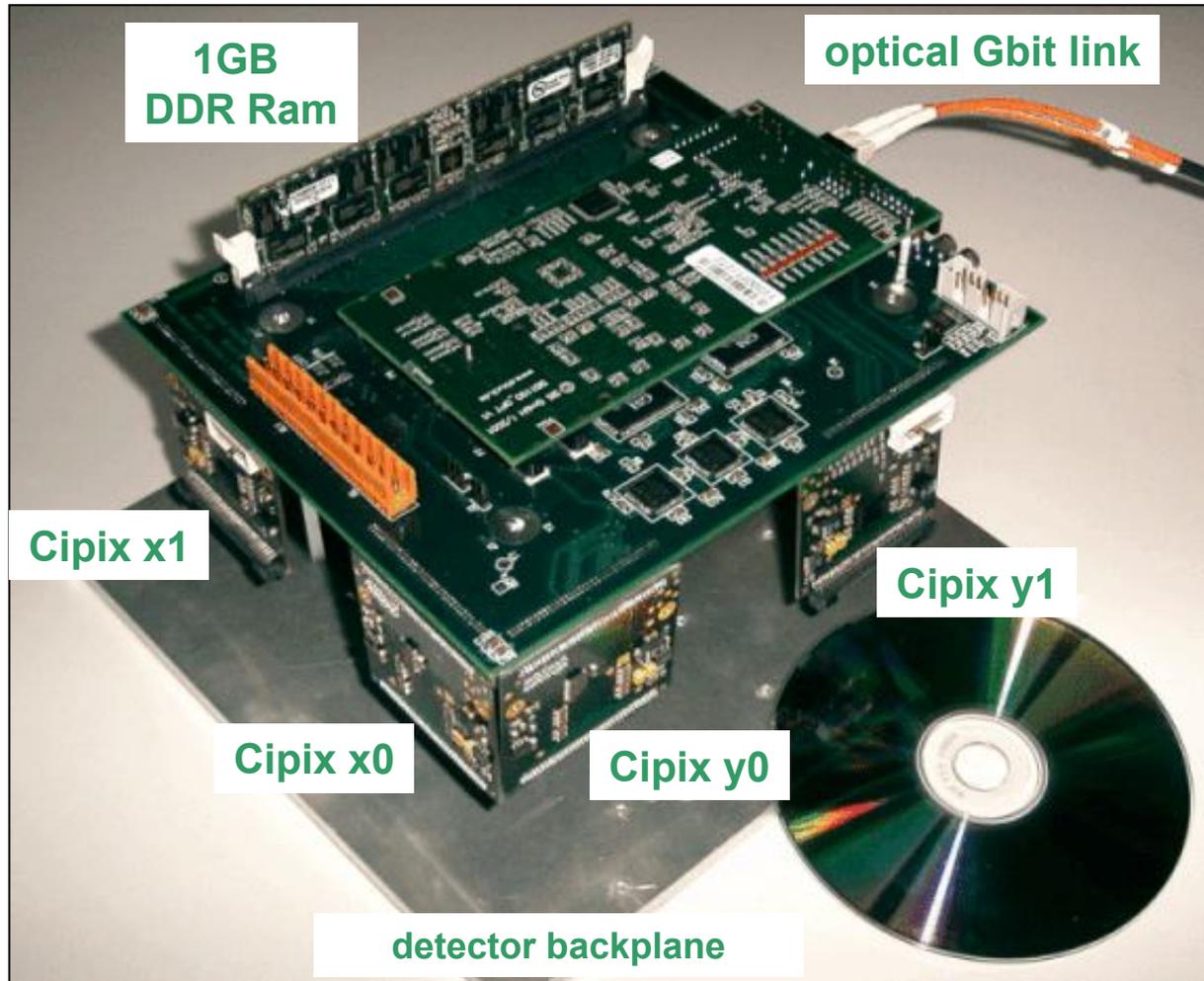


* GameCube is a trademark of Nintendo.



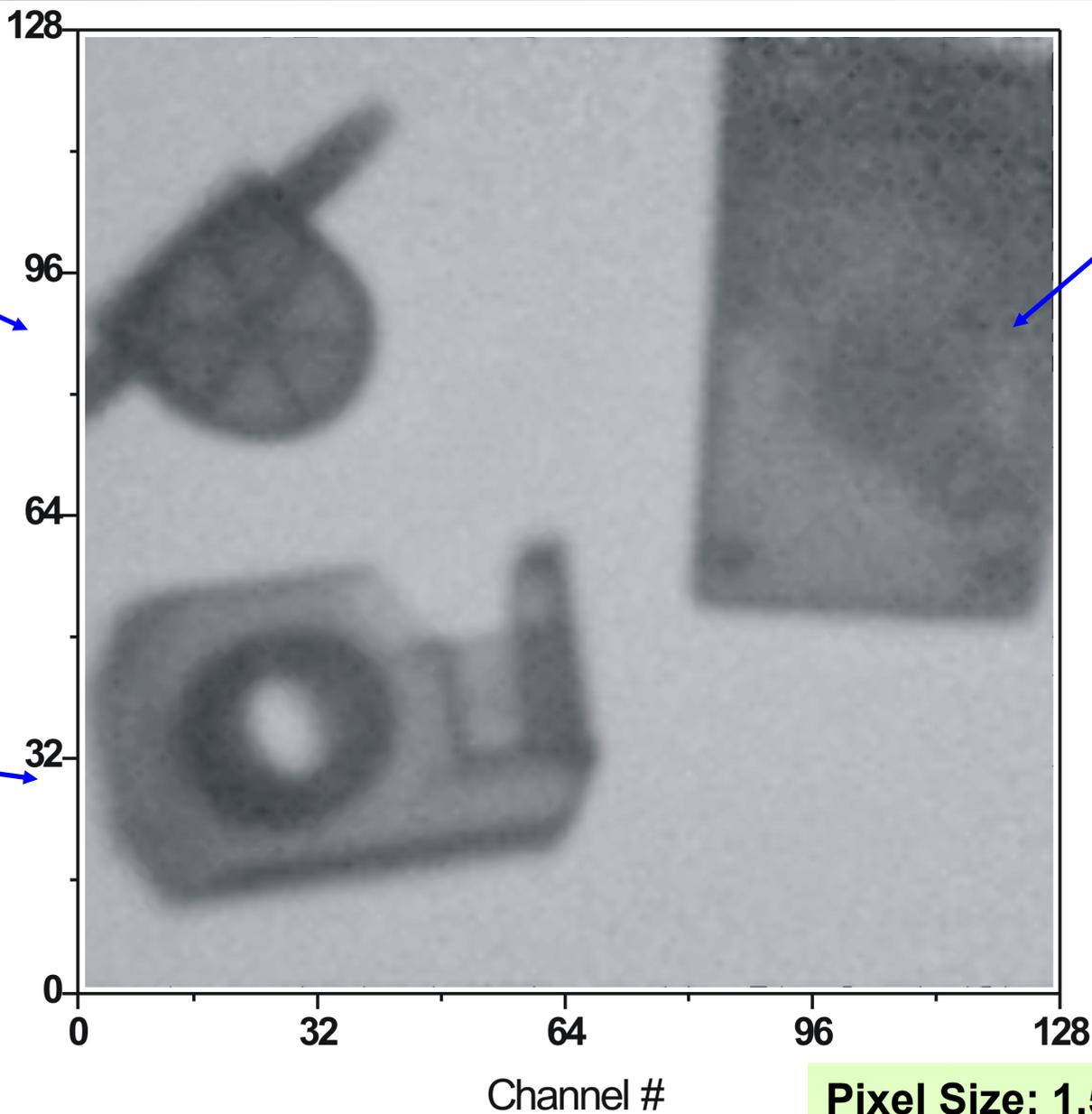
CASCADE

FPGA-based Readout of the 2D-200 Detector

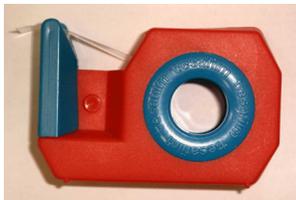


current design of
the CIPix board

Radiography with the 2D-200 CASCADE Detector System



Water
Flow-Indicator



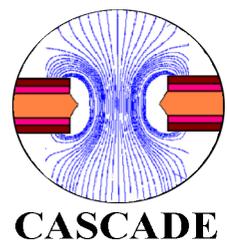
Tesa-Tape
Dispenser

old PC-Mouse

Data taken at
instrument
EKN at FZ
Jülich



Pixel Size: 1.56mm



Neutron Events vs. HE-Events

Character of Data and Challenges in Data Processing

High Energy/ Heavy Ion

- Periodic spill
or bunch crossing
- Detectors with millions of pixels
- MByte of data per event
- Correlations between data
across detector system

but:

- few events of interest
- low pixel occupancy
- low event rate

Neutrons

- Statistically incoming Neutrons
- Currently ~40 000 pixels, future up to 10^6
- ~ 8 byte of data per event
- All events of interest (up to 10^8 per sec)
- Pixel occupancy may be very high
- No fast trigger strategy (no data correlation)

Statistical Nature of Neutron Data

Mathematically

- The number of events in a time interval is poisson distributed
- The time between successive events is exponentially distributed

Practical consequences are:

- New events to be expected any time, no trigger available
- Events come in completely irregularly
- Only the mean rate is well defined
- Practical readout is bandwidth limited, need to specify maximum mean rate at maximum acceptable data loss (dead time).
- 10% max. data loss demands 10 x (mean rate) as readout bandwidth

Neutrons Generate Multiple-Hit Events

A single neutron will generate pulses on several read-out channels because

1. **X and Y detector strips (2D detectors)**
2. **multiple hits for every neutron due to induction of charge on several strips**

We need to correlate data coming from many channels and many ASICs in order to recover the information of every neutron

A precise **Time Stamp** attached to every pulse allows to identify correlated data off-chip



An off-chip sorting processor is required

One ASIC to suit three detector concepts

The Gd/Si-Microstrip Detector is

- the only one with fixed, unity gain in the detection mechanism!
- the one with potentially the smallest amount of charge. (29keV)
- the only one with positive and negative charges.

We should select ASIC specifications that will suit this detector!
The other detectors can be adjusted by manipulating gain and timeconstant.

But: unfortunately we have no clear picture of C_{in} yet.

Let us assume $C_{in} = 30$ pF, which is twice C_{bare}



Specifications for DETNI-ASIC as of 19.06.04

Property	Spec agreed upon	Gd/Si-MSD	Gd/CsI-MSGC	B-CASCADE GEM
channel pitch	50 μm	50 μm	arbitrary	arbitrary
input capacitance C_{in}	30 pF	10....15 pF or rather 25pF ?	23 pF X 40 (33)pF Y	10....30pF
T_p timing channel	30 ns			
T energy channel	$T_{5\%} = 650 \text{ ns}$	Def: Peak is above 5% no longer than $T_{5\%}$		
Max ENC at C_{in} and T_p for timing channel	optimize	550 e	2000 e	660 e
Dynamic range & gain two versions, low gain later	$(8 - 120) \cdot 10^3 \text{ e}$ $(2 - 30) \cdot 10^5 \text{ e}$	$(8 - 69) \cdot 10^3 \text{ e}$	$(2 - 30) \cdot 10^5 \text{ e}$	$(2 - 400) \cdot 10^3 \text{ e}$
no. of chan. per chip	128	128	64, 128	64, 128
timing resolution	4 ns (opt. res.)	8 ns	4 ns	10 ns
Max. % dead-time	10 % -> fifo depth: 10	10 %	10 %	10 %
average rate per chan.	160 kHz	160 kHz	960 kHz	160 kHz

N-XYTER: The DETNI Neutron Detector Readout ASIC

Architecture: 128 channel data driven charge sensitive front end

Front end for either polarity input signals:

Charge sensitive pre-amp

Fast analogue shaper as timing channel: init peak detector, timestamp

Slow analogue shaper as energy channel with peak detection

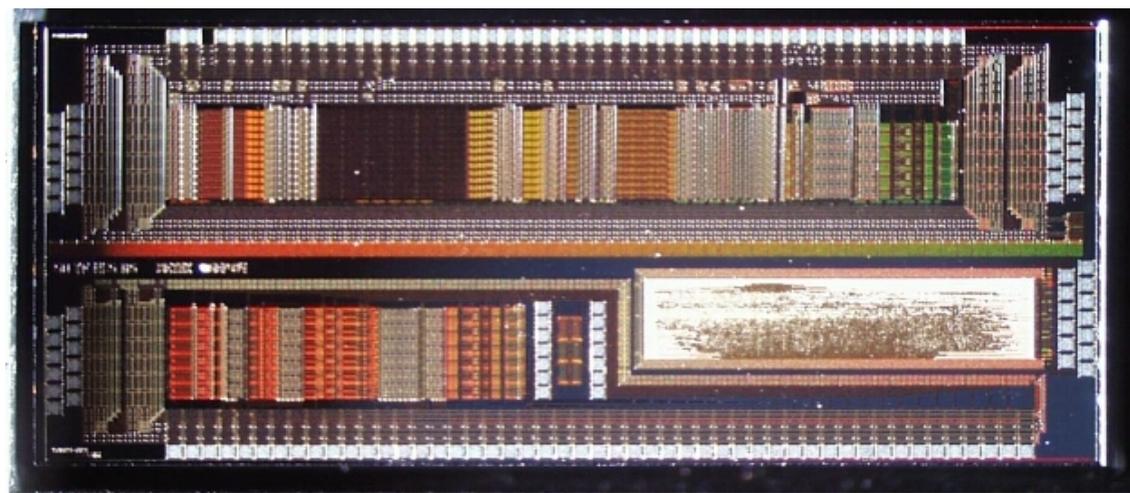
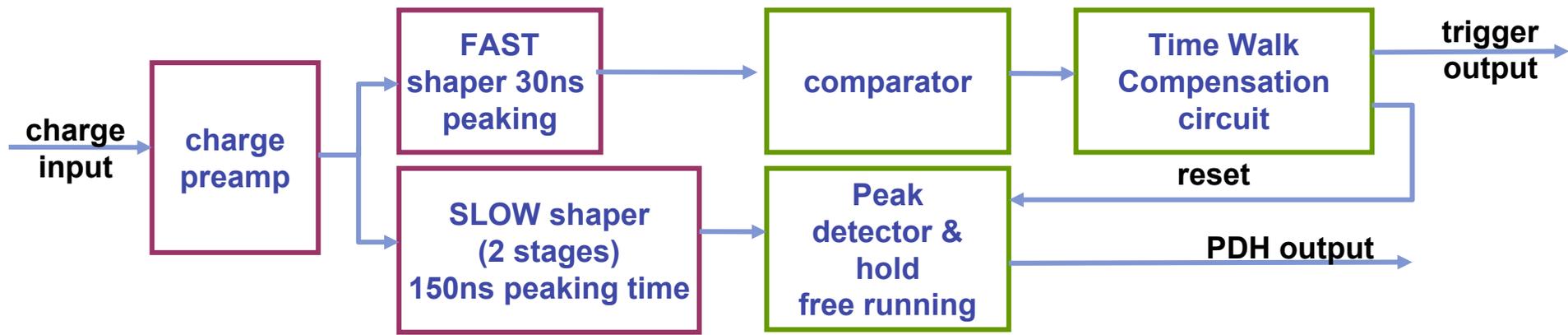
Readout:

- de-randomizing analogue energy and digital time stamp (2ns resolution) FIFO
- 2D-spatial information through X-Y-coincidence
- possible background suppression through spectroscopic window
- resolution enhancement through center of gravity determination
- de-randomizing robust and self sparsifying readout strategy (token ring).

AMS 0.35 microns



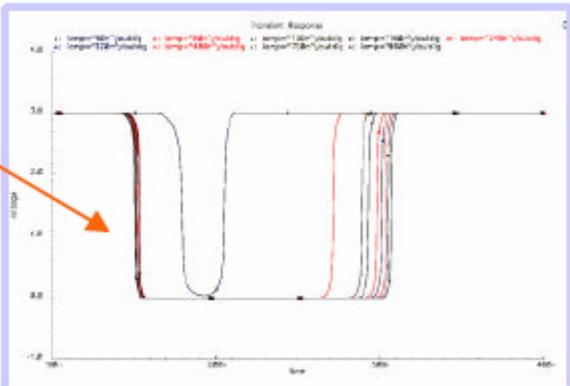
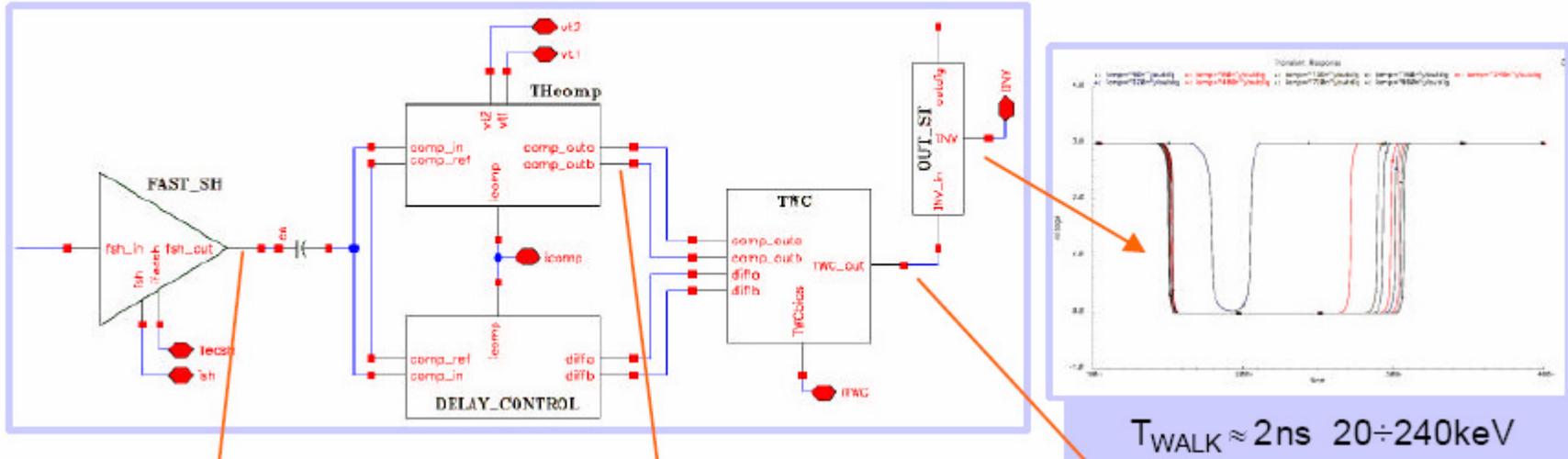
DETNI Data Driven Front End: towards N-XYTER



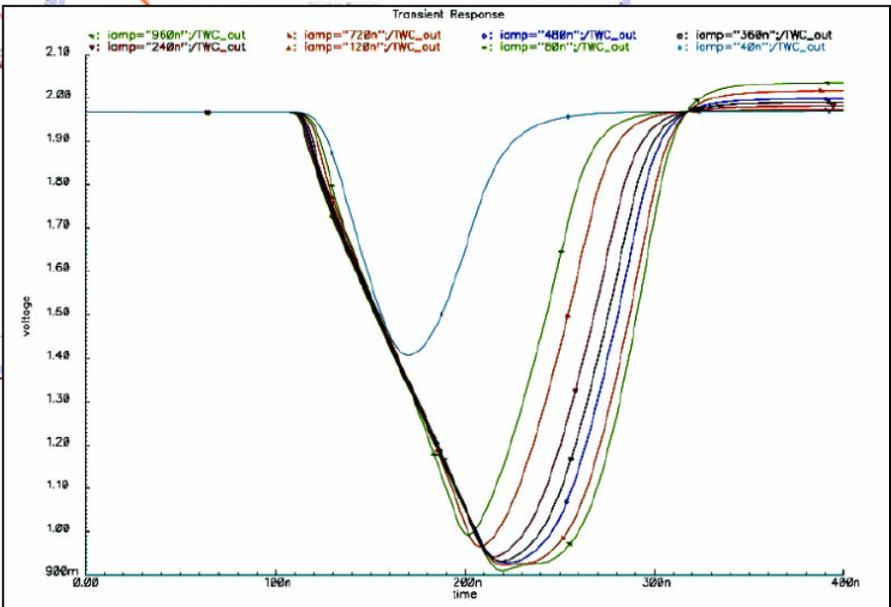
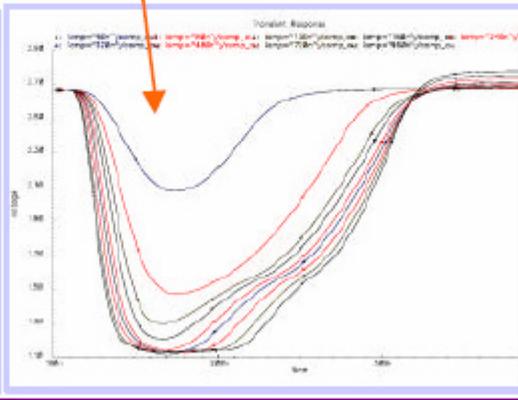
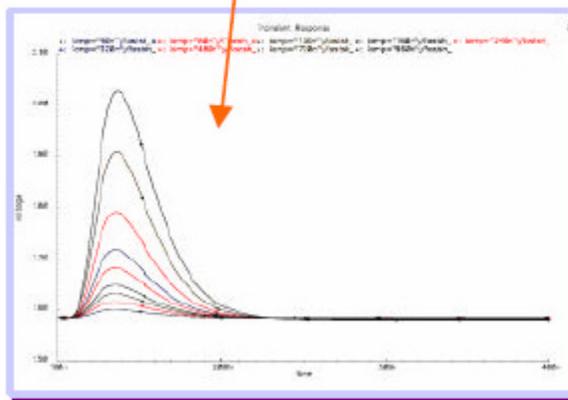
The DETNI ASIC 1.0, a front-end evaluation chip in AMS 0.35 μ



Nanosecond timing without constant fraction: TWC



$T_{WALK} \approx 2ns$ 20÷240keV

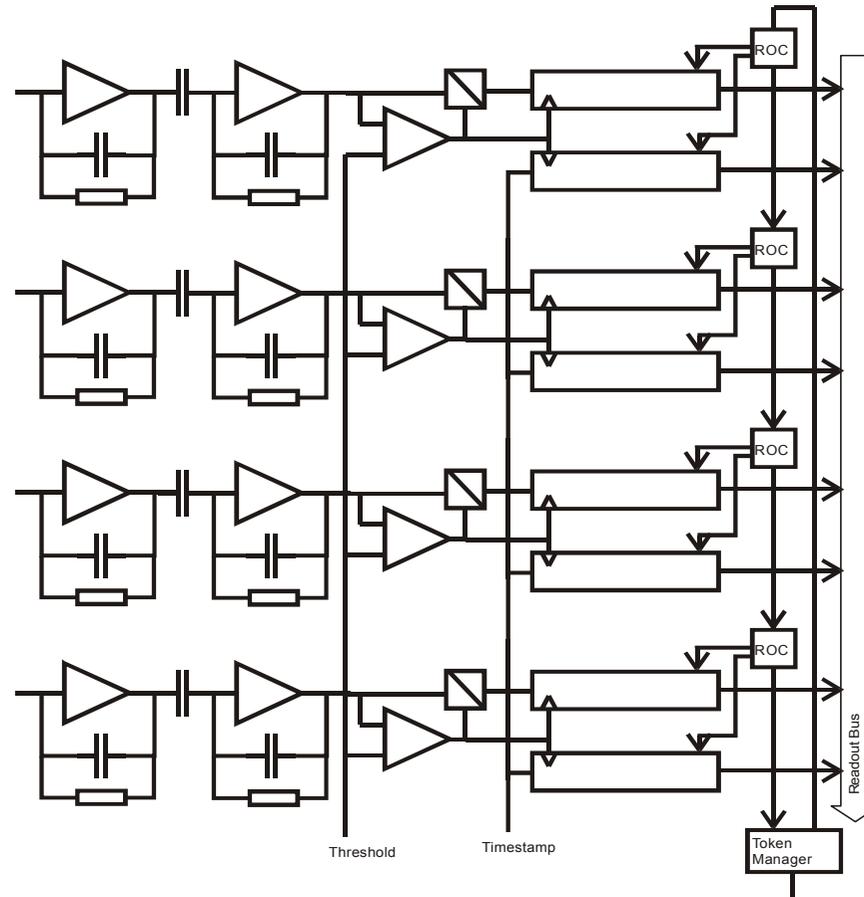


Time Walk Compensation

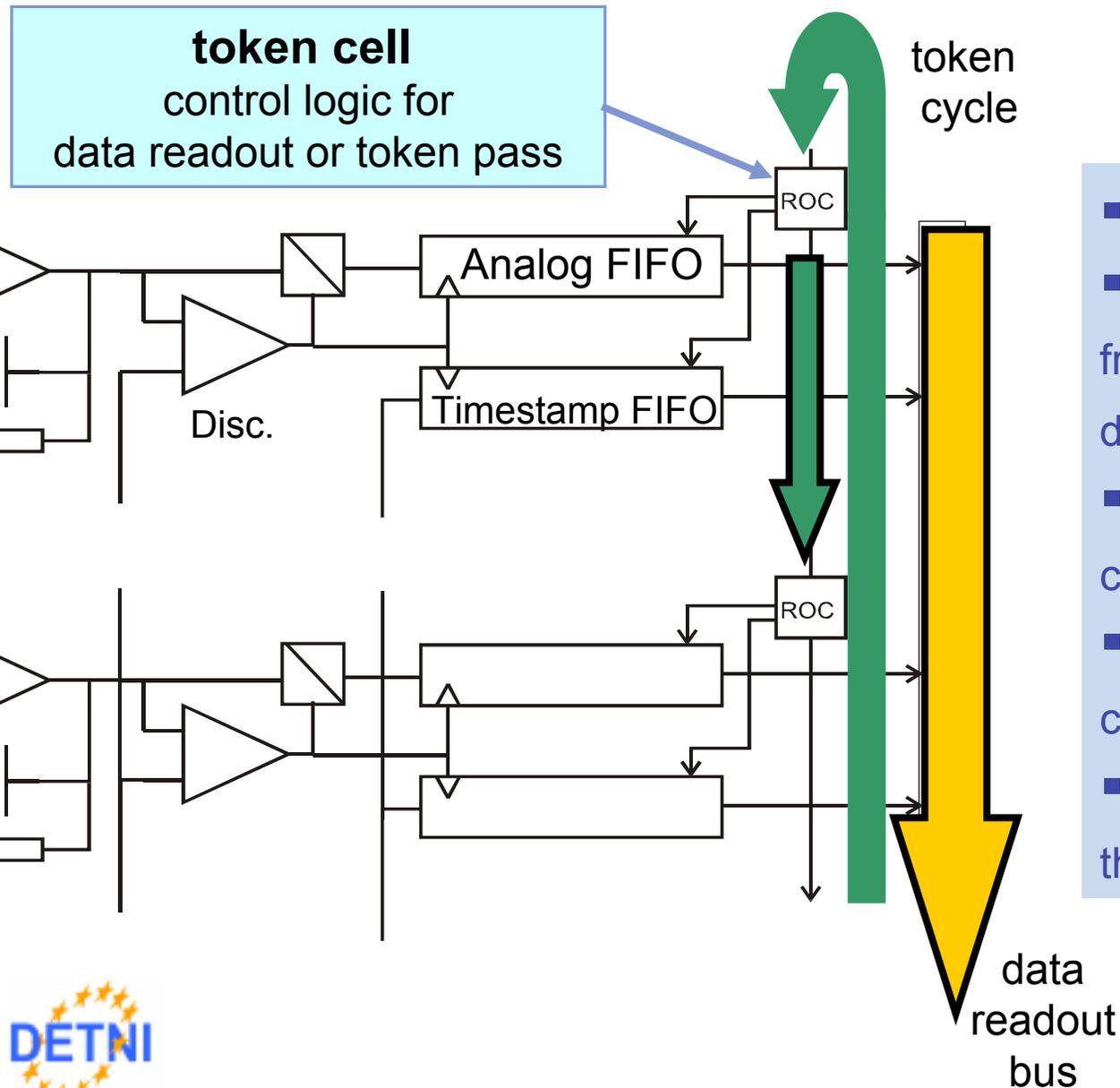


Token Ring Schema as proposed by Ulrich Trunk 2003

Sparsified, de-randomized readout



Token Ring Readout Process



- Periodic readout at 20MHz
- Token asynchronously passes from channel to channel in search of data
- Within one readout cycle token could pass through all channels
- If token encounters occupied channels, data readout is initiated.
- After readout the token passes to the next channel.

Token Ring Architectural Pros/Cons

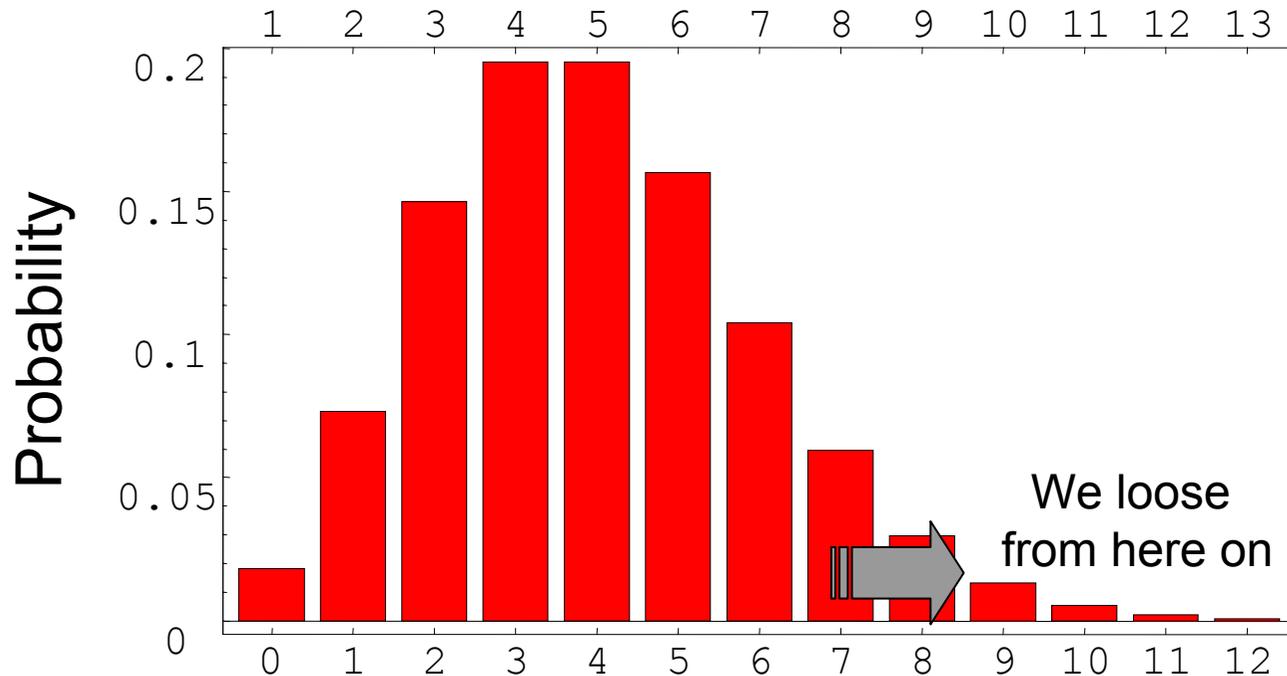
- High Efficiency
 - Empty channels automatically skipped in readout process
 - Built-in fair distribution of readout bandwidth, automatic bandwidth focussing
- Built-in de-randomization: 100% bandwidth used on data
- High Modularity
 - Identical, periodic internal structure for all the channels
 - ASICs with variable number of channels can be realized
 - unused channels remain unnoticed: no use of bandwidth, just power
- Error Robustness
 - Any problematic channel (e.g. continuously firering) will divert and occupy a maximum of $1/n^{\text{th}}$ of the bandwidth.
 - Built-in, non-perfect readout probability avoids unrecoverable logic deadlock: Problematic situations like any kind of pile-up, logic hang-ups or glitch cause mere deadtime but the “show will go on”.

But: Data needs to be tagged with a time-stamp
Data needs to be resorted and re-bunched after readout

Modelling FIFO Occupation

Poisson Distribution(λ):

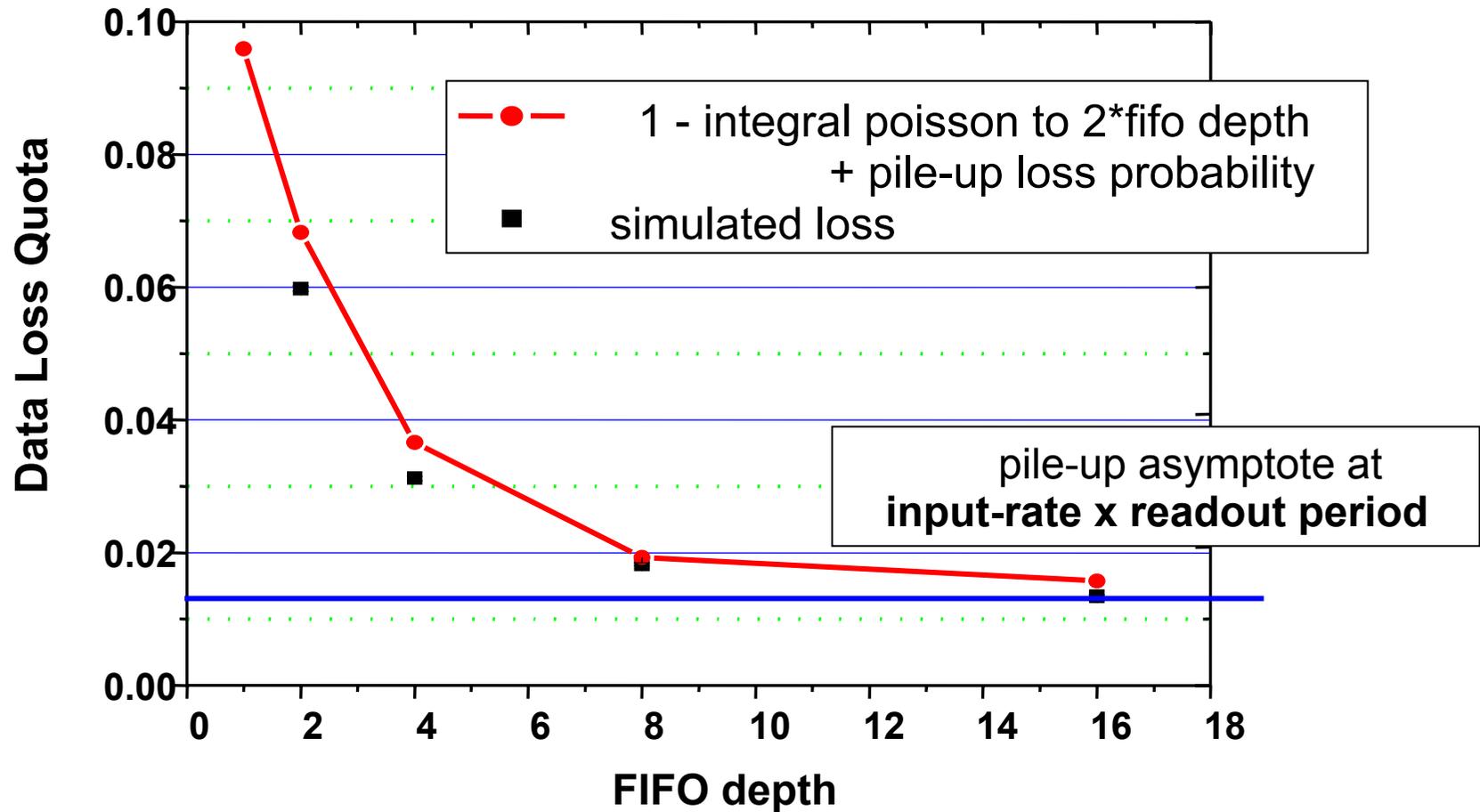
e.g.: fifo depth $n = 4$, so expect 4 events during readout
if incoming rate equals maximum readout rate. $\rightarrow \lambda = 4$.



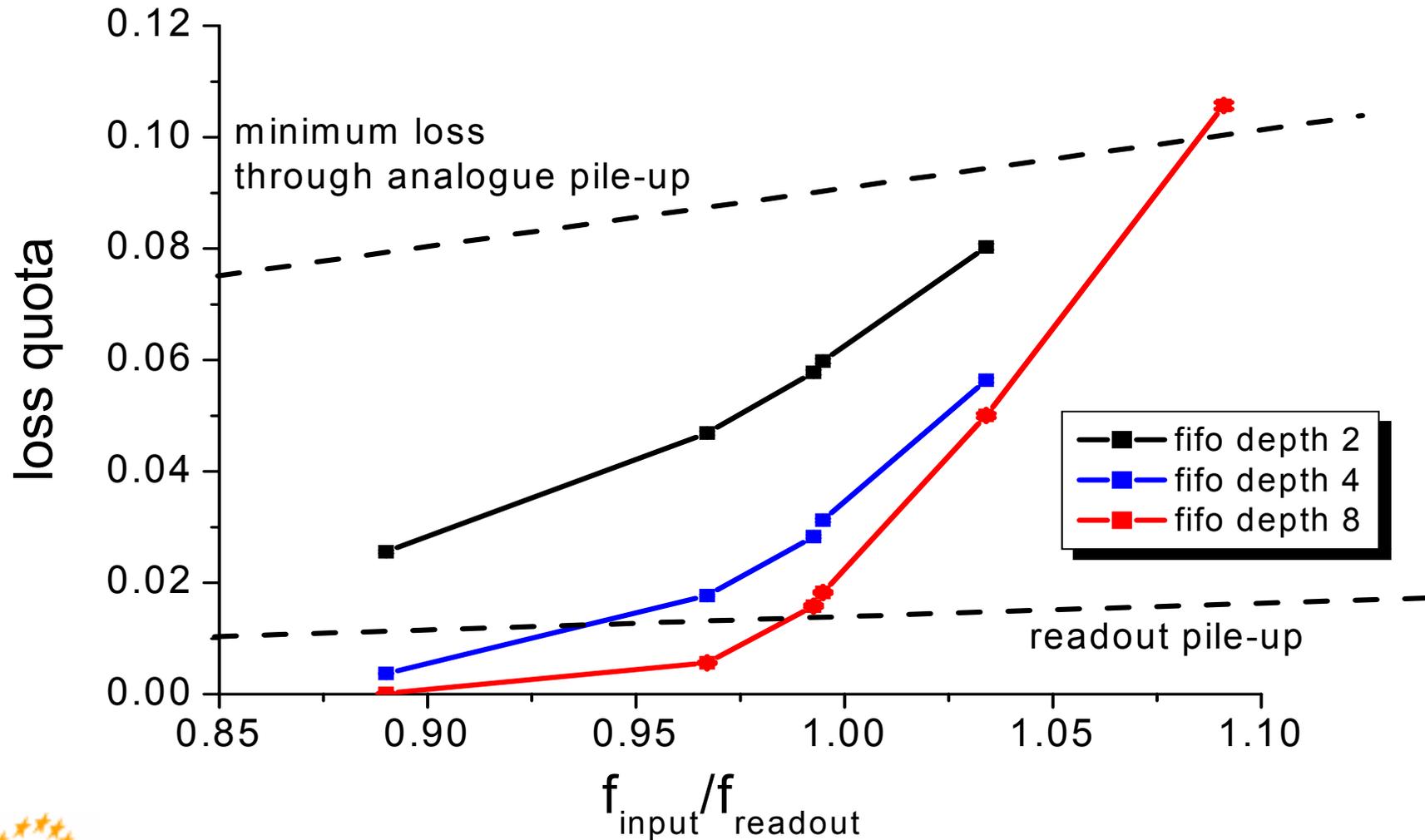
FIFO can virtually be filled with up to $2*n$ events with no data loss
since n elements are read while data comes in.

Study of Individual FIFO

Readout through Token Ring at Mean Input Rate

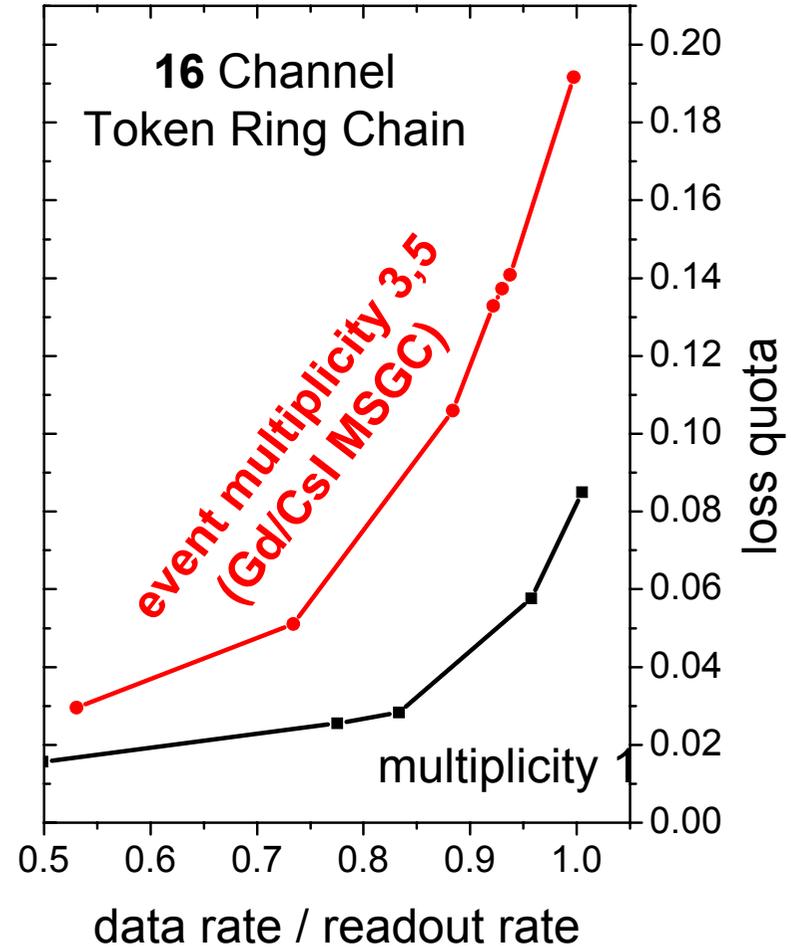
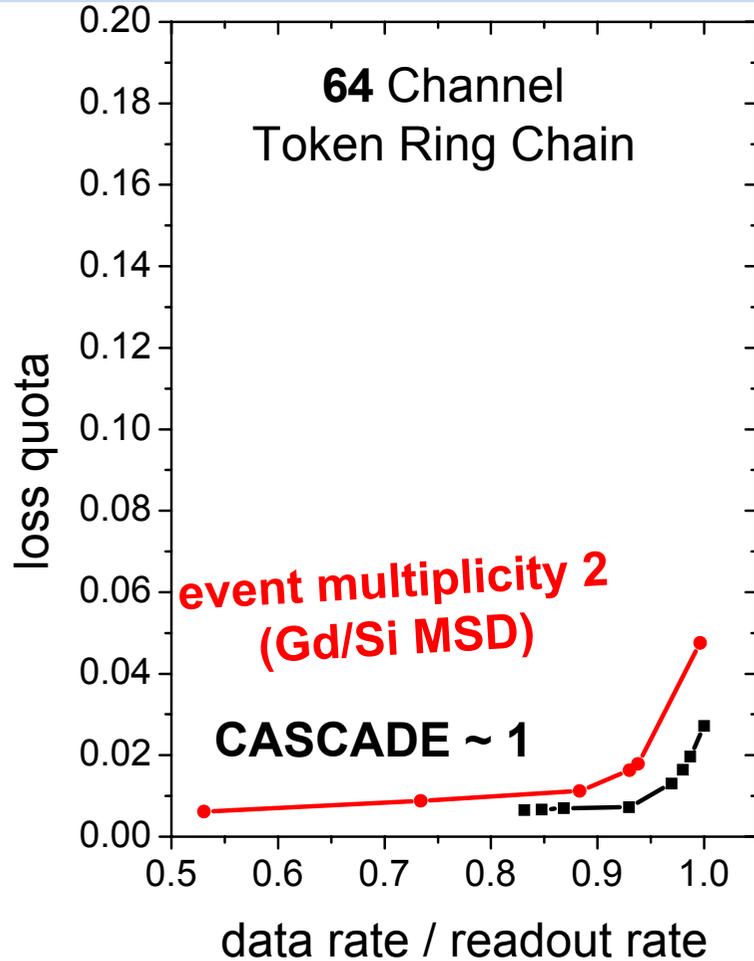


Statistics for the 64 and more channel token ring



DETNI Detectors Simulated Token Ring De-Randomization

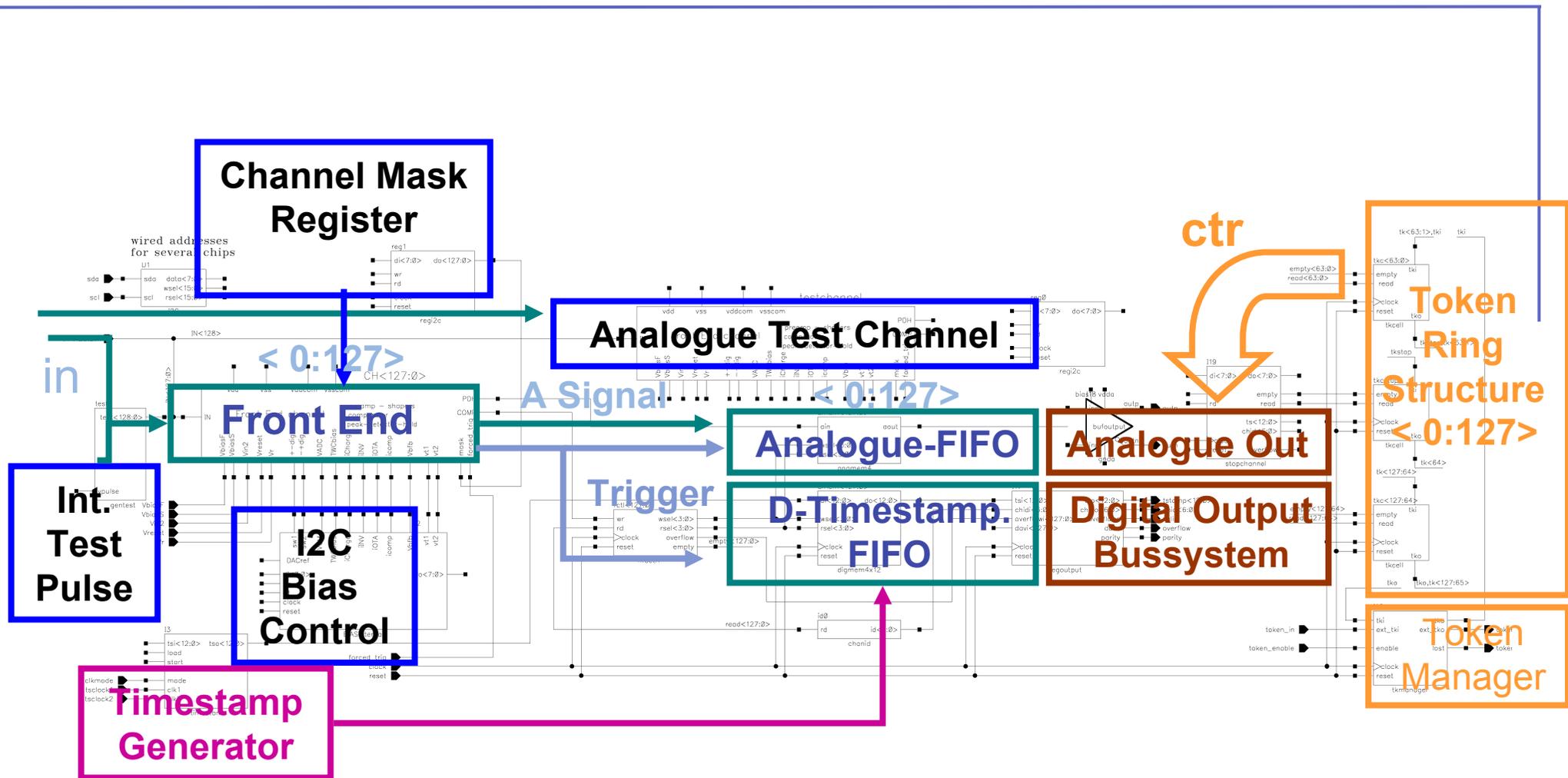
ModelSim simulations: Event multiplicity has impact on loss quota!
four level deep fifo



Conclusions from Simulations

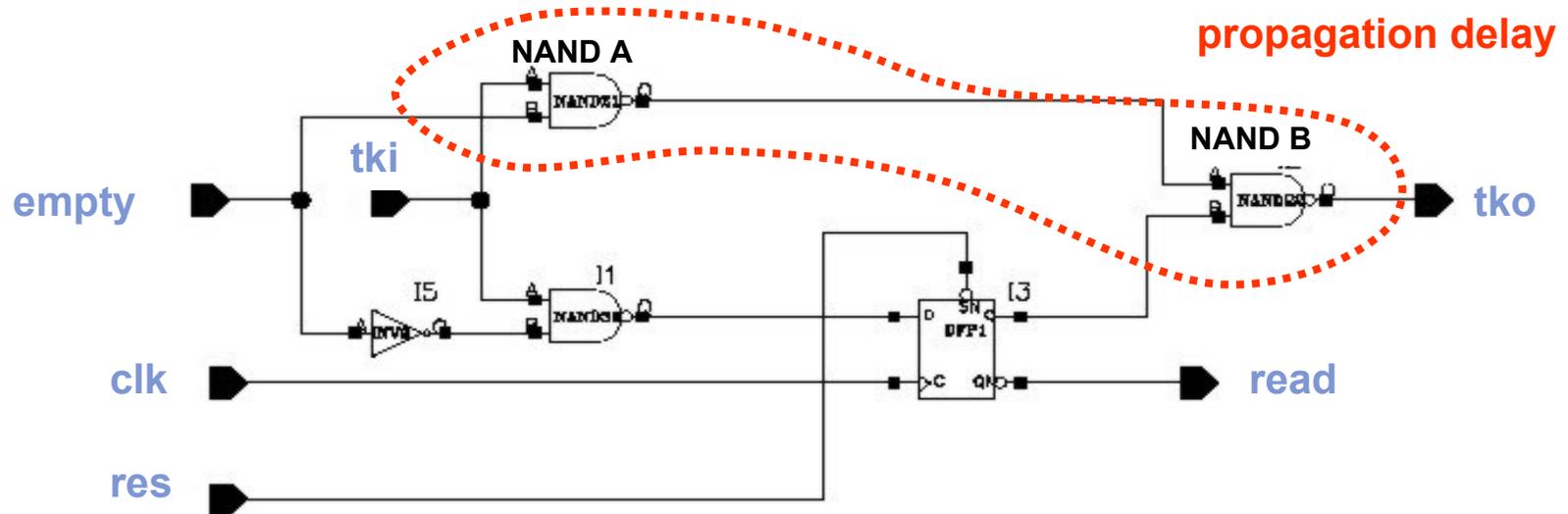
- Individual channel FIFOs add up, to form a large effective data buffer through the token ring.
- 4 level deep FIFOs do the job:
 - FIFO data loss shadowed by analogue pile-up
 - doubling FIFO depth gives little gain
 - more improvement/flexibility through readout overdrive
- 16 channel MSGC-case has less effective buffering memory but also larger margin through analogue pile-up
- Data multiplicity impairs loss quota through
 - correlated occupancy
 - necessity to re-sort data

N-XYTER Top Level Schematic

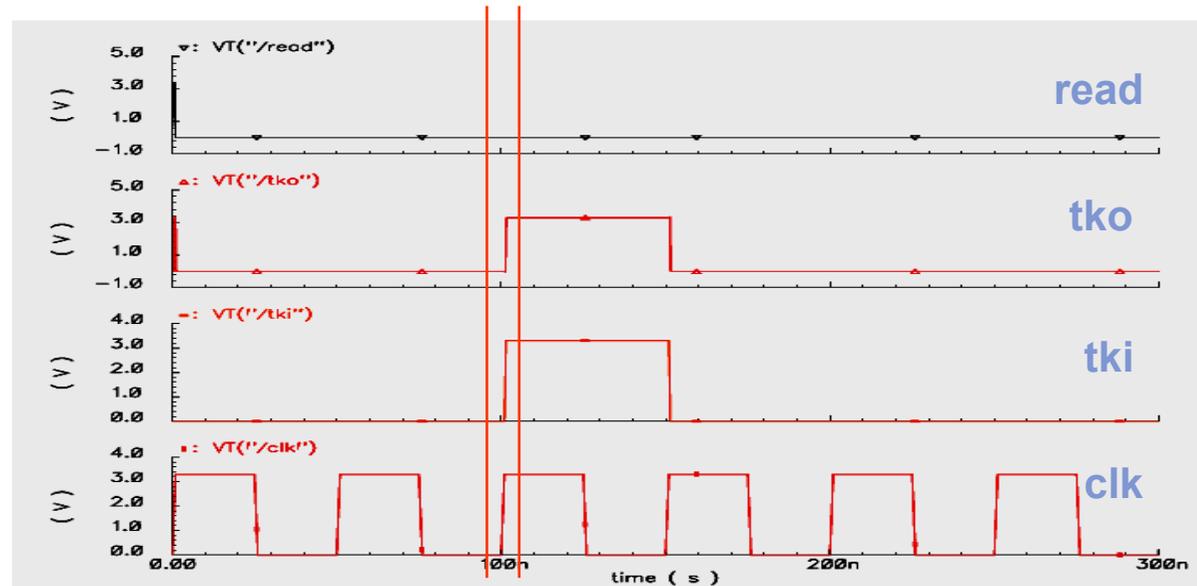


Along the road casting the N-XYTER in Silicon

The TOKEN cell scheme



empty = 1
fifo empty -
no data in this
channel
↓
token flows to next
channel

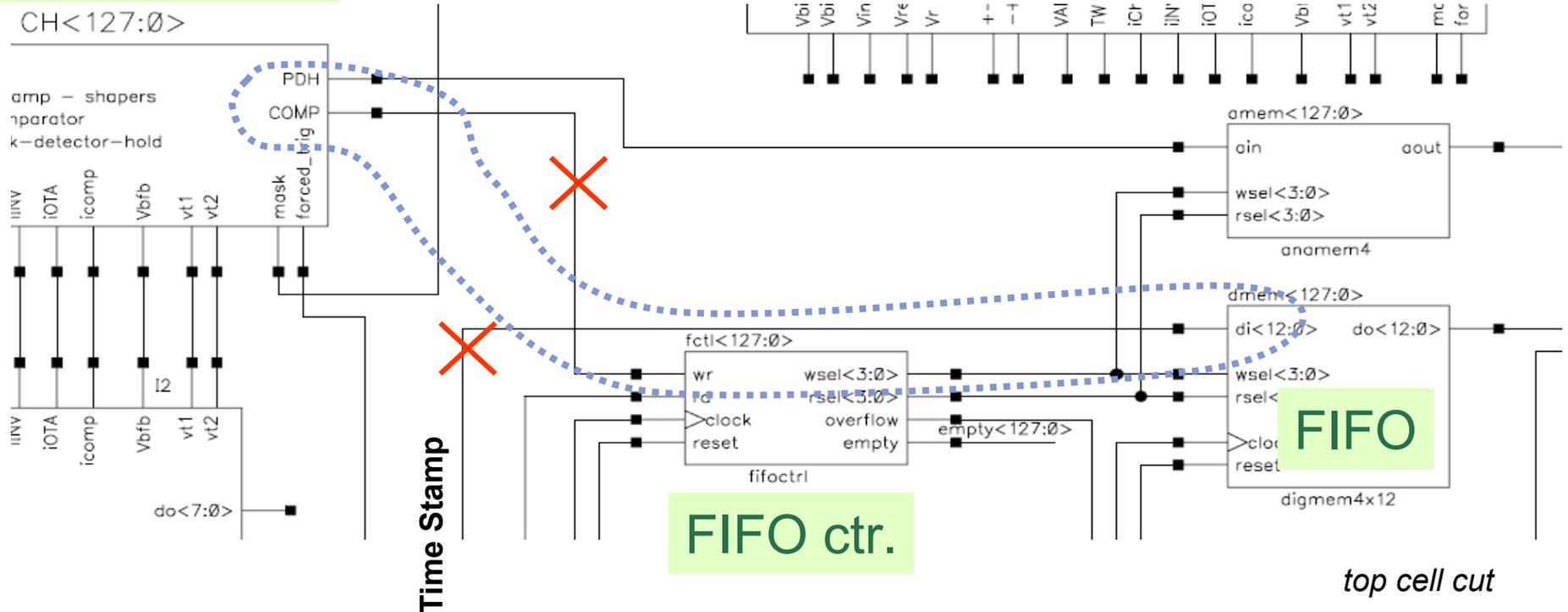


Conclusions on the Token Ring for DETNI

- Combination of token ring and single channel FIFOs allow to buffer statistical neutron data to be read out synchronously at the mean input rate of 20MHz.
- Token ring performance independent of incident neutron spatial distribution
- Severe data loss is possible only at or beyond maximum input data rate (very non-linear behaviour).
- Token can just about be handled in AMS-0.35 μ m technology on 128 channels at 20 MHz readout speed.
- A token break element could be included for risk minimization at very little cost in performance. Token bypass is considered.

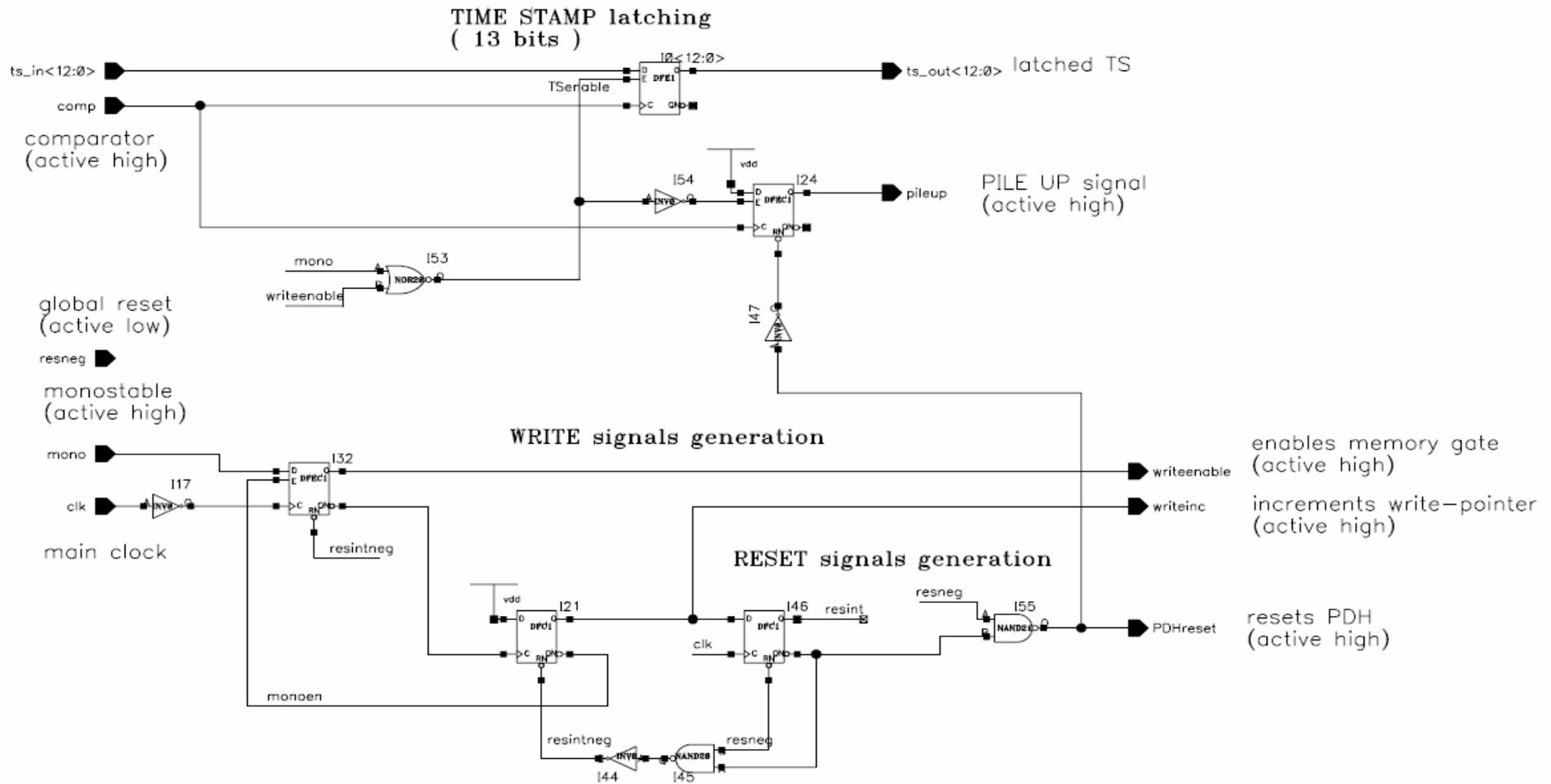
Synchronizer

FE and Comp



1. Comparator signal must be synchronized with the main clock
2. Time Stamp must be latched when comparator fires

Synchronizer



Synchronizer - statistical simulations

- Randomly generated *comparator* pulses (exponential distribution)
- *comparator* duration 5ns ... 50ns (randomly chosen)
- *monostable* duration 200ns (1ns after *comparator* - non-retriggerable)
- 1 million pulses generated

input rate	<i>comparator</i> rising edges	write pulses (% of 1M)	pile-up events (% of 1M)	detected pile-up events* (% of total pu)
200 kHz	994'571	956'818 (95.7%)	38'593 (3.8%)	37'300 (97%)
1 MHz	973'079	813'158 (81.3%)	165'563 (16.5%)	145'866 (88%)

* non-detected pile-up events are due to three pulses pile-up

no error condition detected so far

Near future outlook:

Target submission of 128 channel chip with complete readout architecture realized:

Submission Feb. 2006

Adaptation of N-XYTER to Gd/CsI MSGC detector needs:
16 channels, lower gain, higher rate per channel

Submission March 2006

During the rest of 2006:

Chip testing, evaluation
and introduction into DETNI
detector development projects



DETNI Collaboration

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