#### Status Report - DCS Hypernuclear setup

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- Overview Hypernuclear/-atomic experiment
- DCS of the single elements
  - -Prim. Target
  - -Sec. Target
  - -Germanium Array (PANGEA)

#### Hypernuclei and hyperatoms

- Exited states of AA hypernuclei
- 2 step production
- γ energy range ~ 1–10 MeV
- "Standard" PANDA luminosity conditions



- States of hyper atoms
- $\gamma$  cascading in the atomic shell
- $\gamma$  energy range < 1 MeV
- Similar setup
- First phase of PANDA

Target	F	C1	Sn	Ι	Pb
Transition	$4F \rightarrow 3D$	$5G \rightarrow 4F$	$8J \rightarrow 7I$	$8J \rightarrow 7I$	$10L \rightarrow 9K$
$E_x$ (keV)	131.29	223.55	420.25	474.71	558.47
Y	0.31	0.37	0.76	0.43	0.58
Shift (keV)	1.56	1.84	0.67	2.79	1.73
Width (keV)	0.99	1.14	0.43	2.21	1.26

C. J. Batty, E. Friedman, and A. Gal, Phys. Rev. C 59, 295

#### **Changes in the PANDA Setup**

- Removal of target, MVD and backward endcap
- New beam pipe, prim. and sec. target, Germanium Array









#### Hypernuclear Setup DCS



# **Primary Target**

- Multiple spare targets in the vacuum chamber
- 2 D movement needs 2 kinds of piezo motors
- Nanomotion HR1-1-U-0 to move the carriage
- Galil DMC-4113 controller board (EPICS IOC from manufacturer)
- Some small problems with this controller, so not much information about this one now



# **Primary Target**

- Piezo Wave for target movement
- Small driver board for prototyping
- Beaglebone Black running EPICS IOC (thanks to Florian :D )
- CSS GUI
- State machine via SNL sequencer
- BBB GPIOs seems too slow, real time system needed
- 5 actuators planed for spare targets





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## **Secondary Target**

- Si strip detectors similar to the MVD
- Same electronics than MVD
- Synergy in DCS between both compotents
- Not much progress in here, parameters on the MVD side not fixed yet

### PANda GErmanium Array (PANGEA)

- 16 Cluster with 3 crystals each
- 1 BBB per Cluster
  - monitor all supply voltages (created on board)
  - Set and monitor HV
  - Monitor temperatures
  - Set amplification of the pre amp.
  - Check status of all modules



### PANda GErmanium Array (PANGEA)

- Channels per cryostat:
  - Digital in 15
  - Digital out 21
  - ADC in 20
  - I2C out 6
- Piggyback board for ADCs and stuff
- External reset for BBB foreseen
- Prototype of fully functional detector in 2016

#### Summary / Outlook

- Work on DCS has started
- More details on hardware in Alicias talk
- Ongoing activities focused on the primary target until now
- Parameters for PANGEA recently fixed
- Secondary target connected to MVD DCS
- Germanium prototype in 2016



# Thanks for your attention

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# **Backup slides**

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#### Luminosity





# PANGEA Signals (1)

	А	В	С	D					
1	Signal	Funktion	Variable Type	Direction					
2		HV							
3	HV- SET ON A	Set HV module A ON	TTL/CMOS	OUT					
4	HV- SET ON B	Set HV module B ON	TTL/CMOS	OUT					
5	HV- SET ON C	Set HV module C ON	TTL/CMOS	OUT					
6	HV - STATUS A	Check ON/OFF status HV Module A	TTL/CMOS	IN					
7	HV - STATUS B	Check ON/OFF status HV Module B	TTL/CMOS	IN					
8	HV - STATUS C	Check ON/OFF status HV Module B	TTL/CMOS	IN					
9	HV SET A	Set HV Module A to a given value	REAL (I2C)	OUT					
10	HV SET B	Set HV Module B to a given value	REAL (I2C)	OUT					
11	HV SET B	Set HV Module C to a given value	REAL (I2C)	OUT					
12	HV - V-A	Check HV set to the Module A	REAL (ADC)	IN					
13	HV - V-B	Check HV set to the Module B	REAL (ADC)	IN					
14	HV - V-C	Check HV set to the Module C	REAL (ADC)	IN					
15	HV- I-A	Check current of HV Module A	REAL (ADC)	IN					
16	HV- I-B	Check current of HV Module B	REAL (ADC)	IN					
17	HV- I-C	Check current of HV Module C	REAL (ADC)	IN					
18	HV-SET-BSD-A	Set BSD of HV Module A ON	TTL/CMOS	OUT					
19	HV-SET-BSD-B	Set BSD of HV Module B ON	TTL/CMOS	OUT					
20	HV-SET-BSD-C	Set BSD of HV Module C ON	TTL/CMOS	OUT					
21	HV-BSD-A	Check status of BSD of HV Module A	TTL/CMOS	IN					
22	HV-BSD-B	Check status of BSD of HV Module B	TTL/CMOS	IN					
23	HV-BSD-C	Check status of BSD of HV Module C	TTL/CMOS	IN					
24									
25									
26	26 Temperatures								
27	T-COLDFRAME	Temperature at the cold frame	REAL (ADC)	IN					
28	T-COOLER	Temperature at the cooler	REAL (ADC)	IN					
29	T-BC A	Temperature at the Backcatcher A	REAL (ADC)	IN					
30	T-BC B	Temperature at the Backcatcher B	REAL (ADC)	IN					
31	T-BC C	Temperature at the Backcatcher C	REAL (ADC)	IN					
32	T-PA	Temperature in the PA compartment	REAL (ADC)	IN					
33	T-POWER	Temperature in the power converter compartment	REAL (ADC)	IN					
34	T-CT COOLING	Temperature of the water coolant of the CT-Cooler	REAL (ADC)	IN					
35									

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## **PANGEA Signals (2)**

37	Power Management					
38	P - POS24V SET	Set +24V converter ON	TTL/CMOS	OUT		
39	P - NEG24V SET	Set -24 V converter ON	TTL/CMOS	OUT		
40	P - POS6V SET	Set +6 V converter ON	TTL/CMOS	OUT		
41	P - NEG6V SET	Set -6 V converter ON	TTL/CMOS	OUT		
42	P - POS12V SET	Set +12 V converter ON	TTL/CMOS	OUT		
43	P - POS3.3V SET	Set +3.3 V converter ON	TTL/CMOS	OUT		
44	P - POS24V STATUS	Check ON/OFF status of +24V converter	TTL/CMOS	IN		
45	P - NEG24V STATUS	Check ON/OFF status of -24V converter	TTL/CMOS	IN		
46	P - POS6V STATUS	Check ON/OFF status of +6V converter	TTL/CMOS	IN		
47	P - NEG6V STATUS	Check ON/OFF status of -6V converter	TTL/CMOS	IN		
48	P - POS12V STATUS	Check ON/OFF status of +12V converter	TTL/CMOS	IN		
49	P - POS3.3V STATUS	Check ON/OFF status of +3.3V converter	TTL/CMOS	IN		
50	P - POS24V	Check the output voltage of +24V converter	REAL (ADC)	IN		
51	P - NEG24V	Check the output voltage of -24V converter	REAL (ADC)	IN		
52	P - POS6V	Check the output voltage of +6V converter	REAL (ADC)	IN		
53	P - NEG6V	Check the output voltage of -6V converter	REAL (ADC)	IN		
54	P - POS12V	Check the output voltage of +12V converter	REAL (ADC)	IN		
55	P - POS3.3V	Check the output voltage of +3.3V converter	REAL (ADC)	IN		
56	HV-ENABLE A	Enable HV module A	TTL/CMOS	OUT		
57	HV-ENABLE B	Enable HV module B	TTL/CMOS	OUT		
58	HV-ENABLE C	Enable HV module C	TTL/CMOS	OUT		
59	PA-ENABLE A	Enable PA A	TTL/CMOS	OUT		
60	PA-ENABLE B	Enable PA B	TTL/CMOS	OUT		
61	PA-ENABLE C	Enable PA C	TTL/CMOS	OUT		
62	BC-ENABLE A	Enable Backcatcher A	TTL/CMOS	OUT		
63	BC-ENABLE B	Enable Backcatcher B	TTL/CMOS	OUT		
64	BC-ENABLE C	Enable Backcatcher C	TTL/CMOS	OUT		
65						
66						
67		Varia				
68	CT-OPERATIONAL STATUS	Check the operational status of the CT-Cooler	TTL/CMOS	IN		
69	CT-COOLING STATUS	Check the water cooling status of the CT-Cooler	TTL/CMOS	IN		
70	XC-OPERATIONAL STATUS	Check the operational status of the XC-Cooler	TTL/CMOS	IN		
71						
72	PA-AMP-A	Adjust the amplification of of the last preamp stage	REAL (I2C)	OUT		
73	PA-AMP-B	Adjust the amplification of of the last preamp stage	REAL (I2C)	OUT		
74	PA-AMP-C	Adjust the amplification of of the last preamp stage	REAL (I2C)	OUT		
75						