Overview on EoI 13b

① SIS100 Bunch Compression System

② SIS100 Barrier Bucket System

③ Interfaces and Low-Level RF for:

- all SIS100 RF Systems (Accel., BC, BB, Long. Feedback)
- all CR RF Systems (Debuncher)
- all NESR RF Systems (Decel., BB, HH)
- all RESR RF Systems (Decel.)
- all SIS300 RF Systems (Accel.)
- all ER RF Systems (Accel.)
- all HESR RF Systems (High-Power, Low-Power)

④ pLINAC (Interfaces & Low-Level RF – rest included in EoI 13a)

⑤ CR Debuncher System (not yet part of EoI 13b signature)

13b①: SIS100 Bunch Compression System (2.8.4.3)

Included Items

- 9 Bunch Compressor Cavities incl. Tetrode Amplifier and Amplitude Control (3026.4 k€) 2.8.4.3.1
- 9 Supply Units (2202.2 k€) 2.8.4.3.3

Excluded Items

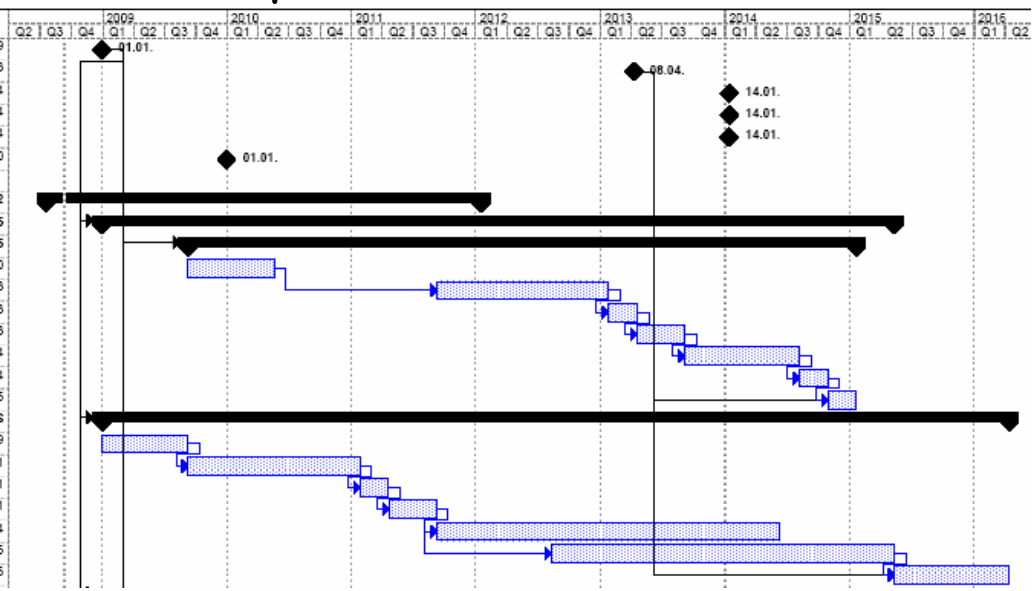
- Driver Amplifiers (however included in 13b③) – 567k€ 2.8.4.3.2
- Dig. Phase Control, Control System Interfaces (however included in 13b③) – 437.4k€ 2.8.4.3.4
- Dig. Cavity Synchronization (however included in 13b③) – 168.9k€ 2.8.4.3.5
- Optical Transmission of Gap and Grid Voltages, Vacuum Gap Relays, Fast Switches (however included in 13b③) – 247.1k€ 2.8.4.3.6
- Media Supply Infrastructure
- Room-to-Room Cables

13b①: SIS100 Bunch Compression System (2.8.4.3)

Time Schedule

- Design completed: Draft 03/2009, Final 09/2009
- 01/2011 First system produced
- 09/2011 First system tested and optimized
- 06/2014 Series production completed
- 05/2015 Lab & acceptance tests completed

Vorgangsname	Dauer	Anfang	Ende
Availability FAIR Project Financing	0 Tage	01.01.09	01.01.09
Building SIS100 available for installation	0 Tage	08.04.13	08.04.13
Building CR available for installation	0 Tage	14.01.14	14.01.14
Building NESR available for installation	0 Tage	14.01.14	14.01.14
Building RESR available for installation	0 Tage	14.01.14	14.01.14
Testing hall available	0 Tage	01.01.10	01.01.10
SIS12/18 h=2 System	**910 Tage**	**22.07.08**	**16.01.12**
SIS100 Acceleration	**1660 Tage**	**01.01.09**	**13.05.15**
SIS100 Barrier Bucket	**1400 Tage**	**10.09.09**	**21.01.15**
Design	9 Monate	10.09.09	19.05.10
Production of first system	18 Monate	08.09.11	23.01.13
Lab tests & acceptance tests first system	3 Monate	24.01.13	17.04.13
Optimization first system	5 Monate	18.04.13	04.09.13
Series production	12 Monate	05.09.13	06.08.14
Lab & acceptance tests	3 Monate	07.08.14	29.10.14
Installation	3 Monate	30.10.14	21.01.15
SIS100 Bunch Compression	**1900 Tage**	**01.01.09**	**13.04.16**
Design	9 Monate	01.01.09	09.09.09
Production of first system	18 Monate	10.09.09	26.01.11
Lab tests & acceptance tests first system	3 Monate	27.01.11	20.04.11
Optimization first system	5 Monate	21.04.11	07.09.11
Series production	36 Monate	08.09.11	11.06.14
Lab & acceptance tests	36 Monate	09.06.12	13.05.15
Installation	12 Monate	14.05.15	13.04.16



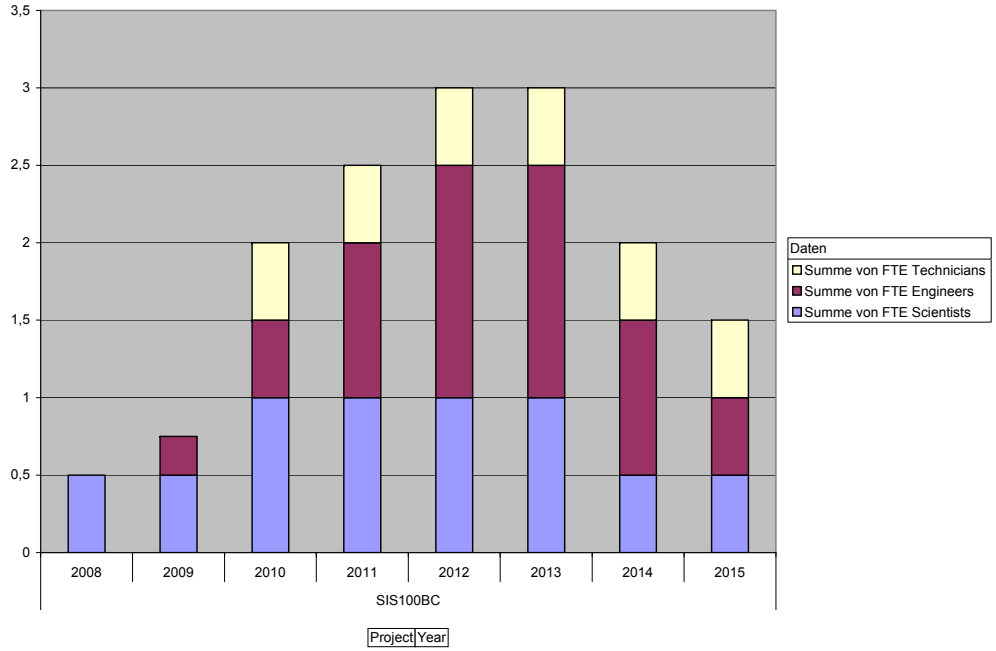
13b①: SIS100 Bunch Compression System (2.8.4.3)

Prerequisites

Construction and manufacturing by industrial partner

Required Resources

Tasks: specification, call for tenders, supervision of manufacturer, project tracking, test & optimization, acceptance tests)



13b②: SIS100 Barrier Bucket System (2.8.4.4)

Included Items

- 2 Barrier Bucket Cavities incl. Tetrode Amplifier and Driver Amplifiers (580.5 k€) 2.8.4.4.1
- 2 Supply Units (540.0 k€) 2.8.4.4.2

Excluded Items

- Dig. Phase Control, Control System Interfaces (however included in 13b③) – 84.6k€ 2.8.4.4.3
- Dig. Cavity Synchronization (however included in 13b③) – 48.2k€ 2.8.4.4.4
- Optical Transmission of Gap and Grid Voltages, Vacuum Gap Relays, Fast Switches (however included in 13b③) – 54.9k€ 2.8.4.4.5
- Media Supply Infrastructure
- Room-to-Room Cables

13b②: SIS100 Barrier Bucket System (2.8.4.4)

Time Schedule

- Design completed: Draft 05/2010, Final 05/2011
- 01/2013 First system produced
- 09/2013 First system tested and optimized
- 08/2014 Series production completed
- 10/2014 Lab & acceptance tests completed

Vorgangsname	Dauer	Anfang	Ende
Availability FAIR Project Financing	0 Tage	01.01.09	01.01.09
Building SIS100 available for installation	0 Tage	08.04.13	08.04.13
Building CR available for installation	0 Tage	14.01.14	14.01.14
Building NESR available for installation	0 Tage	14.01.14	14.01.14
Building RESR available for installation	0 Tage	14.01.14	14.01.14
Testing hall available	0 Tage	01.01.10	01.01.10
SIS12/18 h=2 System	**910 Tage**	**22.07.08**	**16.01.12**
SIS100 Acceleration	**1660 Tage**	**01.01.09**	**13.05.15**
SIS100 Barrier Bucket	**1400 Tage**	**10.09.09**	**21.01.15**
Design	9 Monate	10.09.09	19.05.10
Production of first system	18 Monate	08.09.11	23.01.13
Lab tests & acceptance tests first system	3 Monate	24.01.13	17.04.13
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SIS100 Bunch Compression	**1900 Tage**	**01.01.09**	**13.04.16**
Design	9 Monate	01.01.09	09.09.09
Production of first system	18 Monate	10.09.09	26.01.11
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Lab & acceptance tests	36 Monate	09.06.12	13.05.15
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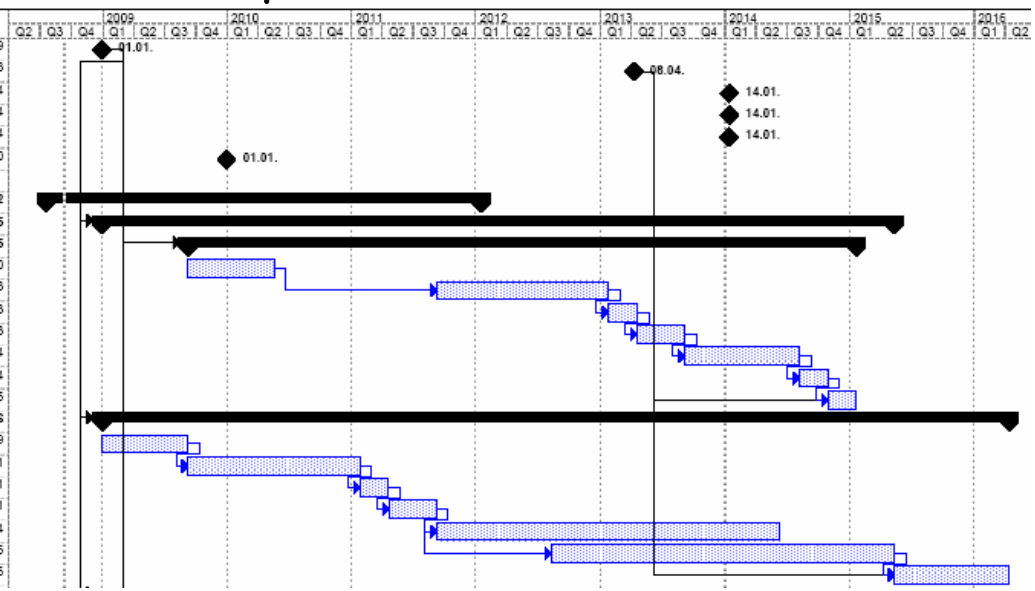


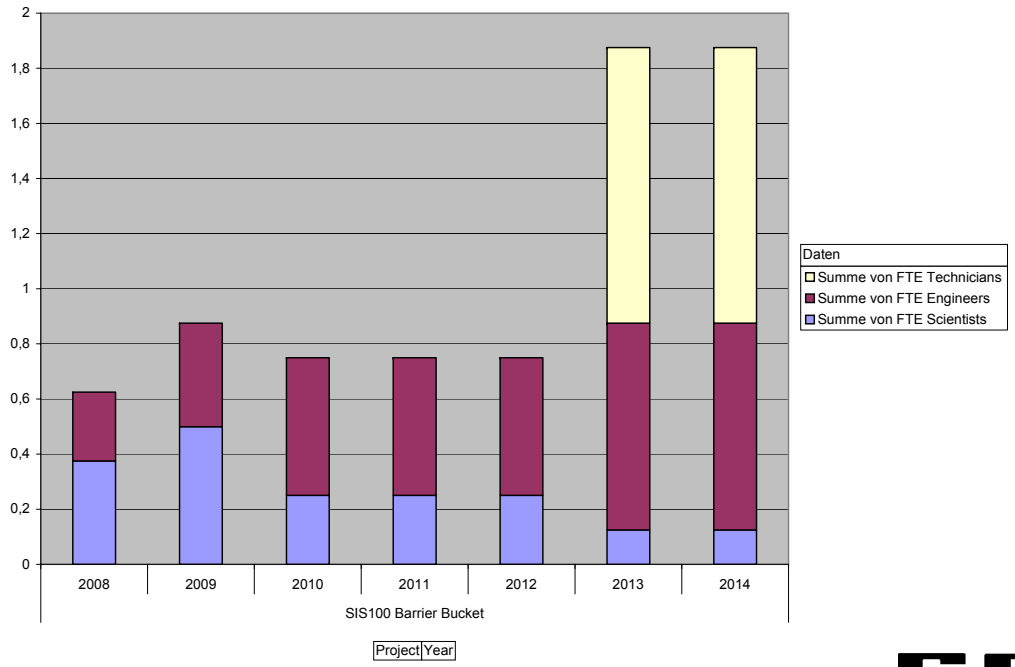
13b②: SIS100 Barrier Bucket System (2.8.4.4)

Prerequisites

Construction and manufacturing by industrial partner

Required Resources

Tasks: development of signal generation electronics, specification, call for tenders, supervision of manufacturer, tracking, test & optimization)



13b③: Interfaces & Low-Level RF

Included Items (for all SIS100 RF systems)

- Driver Amplifiers except BB and long. feedback
- Dig. Phase Control, Control System Interfaces (incl. all DDS units)
- Dig. Cavity Synchronization
- Optical Transmission of Gap and Grid Voltages, Vacuum Gap Relays, Fast Switches

Excluded Items

- Non-standard driver amplifiers (broadband for BB)
- Gap and grid voltage dividers (part of the cavity)
- Amplitude and resonant frequency control (part of the cavity system)
- DAC units (included in EoI 13d)

13b③: Interfaces & Low-Level RF

Time Schedule & Required Resources

- Driver Amplifiers (0.25 FTE): Availability of prototype: 06/2009 — ext. company
- Dig. Phase Control and Dig. Cavity Synchronization (2.5 FTE): Continuous development — in-house
- Maintenance & Diagnostics (0.5 FTE): Continuous development — ext. companies
- Optical Transmission of Gap and Grid Voltages (0.5 FTE): Availability of prototype: 09/2009 — ext. company
- Vacuum Gap Relays: Call for tenders starts after funding — series product
- Fast Switches: Availability of prototype: 12/2009 — ext. company

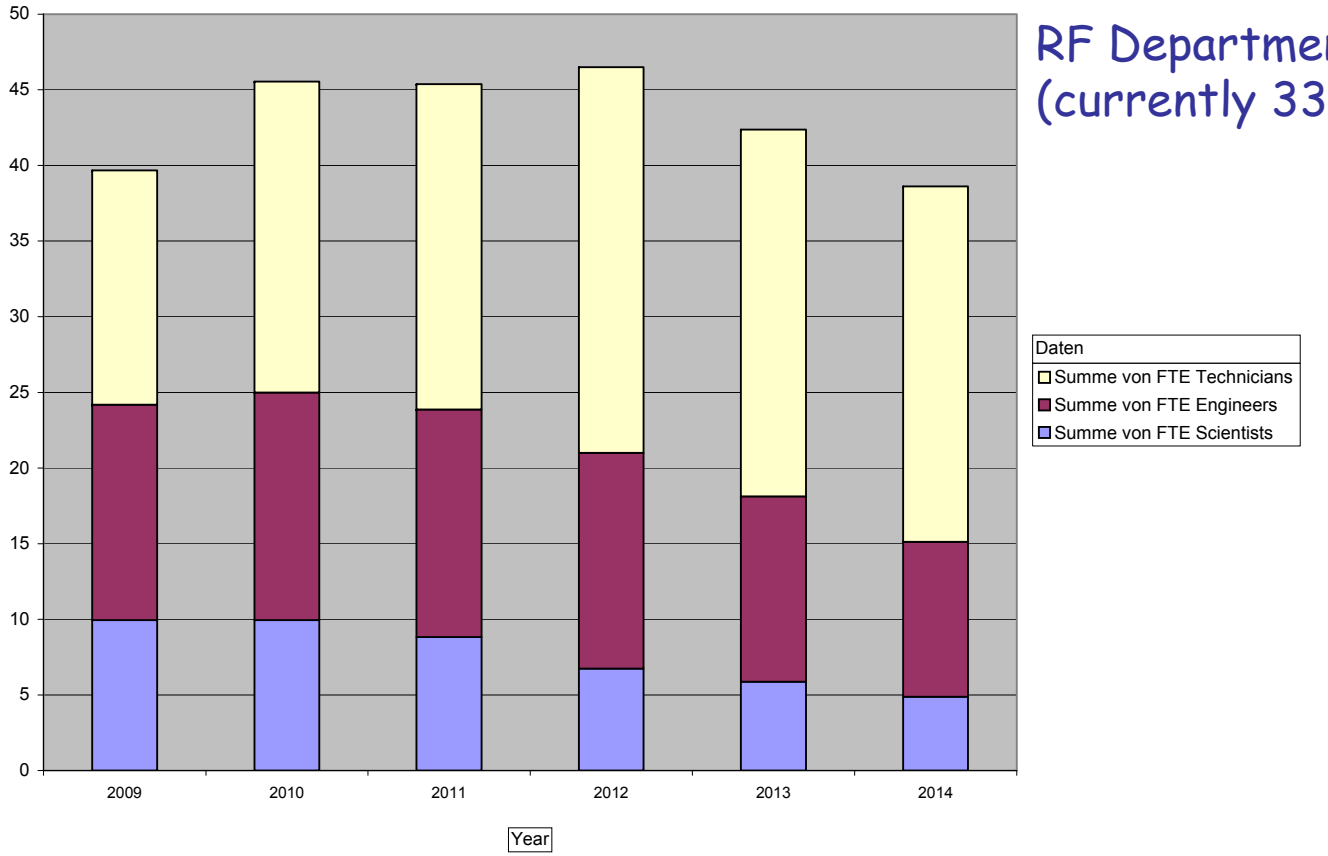
These components are not on the critical path, i.e. they can be ordered in time for the corresponding cavity systems.

3.75 FTE are required continuously

Decision for this in-kind contribution must be valid for all synchrotrons & storage rings.

Prerequisites for All Tasks

- Official assignment of in-kind contribution 12/2008
- Assignment of manpower (about 5 additional specialists in 2009,
  about 5 additional specialists in 2010)
- Funding



RF Department
(currently 33 FTE)

Appendix

Synchrotron RF Systems

Ring	RF System	Frequency Range [MHz]	Total Voltage [kV] Stage A/B	Duty Cycle	Cavity Length	Qty Stage A/B
SIS18 Upgrade 2.2.4	Accel. h=2 Bunch Compression	0.43 ... 2.8 0.8	40 40/80	50% 0.05%	1.27 m 1 m	3 1/2
SIS100 2.8.4	Accel. h=10 (Ferrite) Bunch Compression Barrier Bucket Long. Feedback	1.1 ... 2.7 0.395 ... 0.485 1.5 (broadband) LF...5.6 (broad-band)	280/400 360/640 2 x 15 20	100% 0.05% 20% 100%	2.8 m 1 m 1 m 1 m	14/20 9/16 2 2
SIS300 2.12.4	Accel. h=10 (Ferrite)	1.1 ... 2.7	0/160	100%	2.8 m	0/8

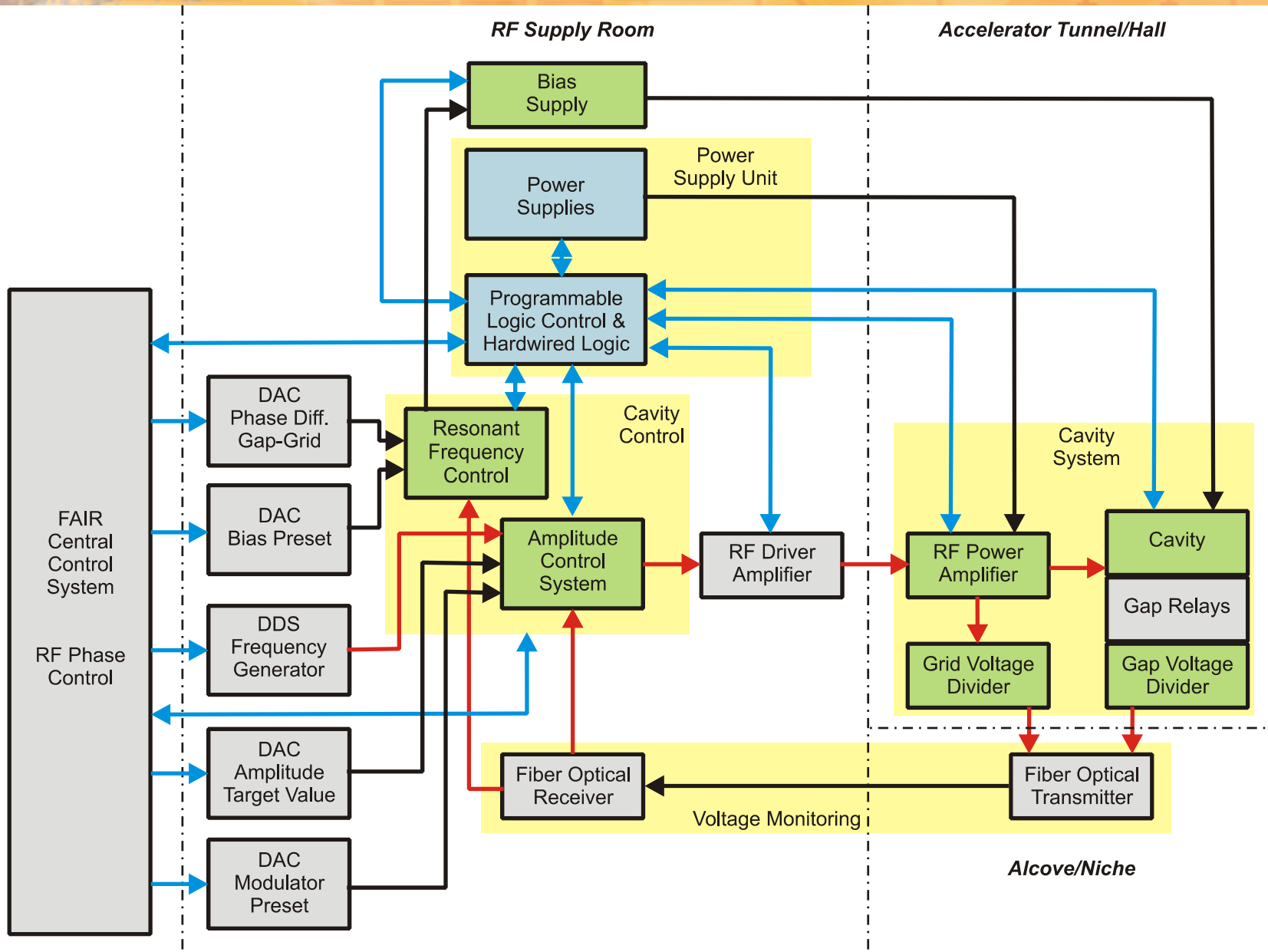
Storage Ring RF Systems

Ring	RF System	Frequency Range [MHz]	Maximum Voltage [kV] Stage A/B	Duty Cycle	Cavity Length	Qty Stage A/B
CR 2.5.4	Debuncher (RIB, anti-protons, includes Bucket Generation)	1.18...1.38	200 10	0.05% 100%	1 m	5
NESR 2.6.4	Deceleration Barrier Bucket Stacking High Harmonics	0.998...2.28 5 (broadband) 44.8	15 2 0/50	100% 20% 100%	2.8 m 0.8 m 1 m	1 4 0/1
RESR 2.10.4	Deceleration	0.52...1.21	15	100%	3.2 m	1
HESR 2.11.4	Responsibility Jülich					

Technical Structure of Ring RF Systems

- Power Supply Unit (including Programmable Logic Control, PLC) – especially relevant for RF tube power amplifiers, PLC required for slow-control, interlock handling, etc. – Siemens S7 is standard
- Cavity and Power Amplifier
- Driver Amplifier
- Low-Level RF System
  - Cavity control
    - Amplitude control
    - Resonant frequency control (if required)
    - Feedback around the amplifier (if required)
  - Phase control and other higher-level control systems

SIS100 - FAIR EoI 13b: RF Systems



Grey Boxes:

Content of EoI 13b "Interface and Low-Level RF"

Green Boxes:

Usually included in content of delivery of cavity supplier

Standardization Requirements

Background: Keep maintenance effort & costs for spare parts low

Sub-systems to be standardized (EoI 13b):

- Limited number of different types of **driver amplifier** (modular system)
- **Gap switches**
  - Fast semiconductor switches for cycle-to-cycle switching
  - Slow ones for de-activating cavities (vacuum relays)
- Gap and grid **voltage monitors** (optical transmission)
- Limited number of different types of **supply units** (only one type of PLC)
- **Interfaces** to central control system (e.g. DDS, DAC)

Reference: H.Klingbeil et al.: "Standardization Requirements for FAIR RF Systems" (Common Remarks for FAIR RF Systems)

FAIR RF Work Packages (1/2)

- CAVITY SYSTEMS
  - SIS18 h=2 Cavities (SIS18_h=2_CAV)
  - CR Debuncher Cavities (CR_DB_CAV)
  - SIS100/300/NESR Accelerating Cavities (SIS100_300_NESR_CAV)
  - SIS100 Barrier Bucket Cavities (SIS100_BB_CAV)
  - SIS100 Bunch Compressor Cavities (SIS100_BC_CAV)
  - NESR Barrier Bucket Cavity (NESR_BB_CAV)
  - NESR High Harmonics (NESR_HH)
  - RESR Cavity (RESR_CAV)
  - HESR RF Systems (HESR_RF_Jülich)
  - ER Cavity (ER_CAV)
  - pLINAC Cavities (pLINAC_CAV)
  - SIS100 Longitudinal Feedback System (SIS100_Long_Feedb_CAV)

Reference: H.Klingbeil et al.: "FAIR RF Work Packages"

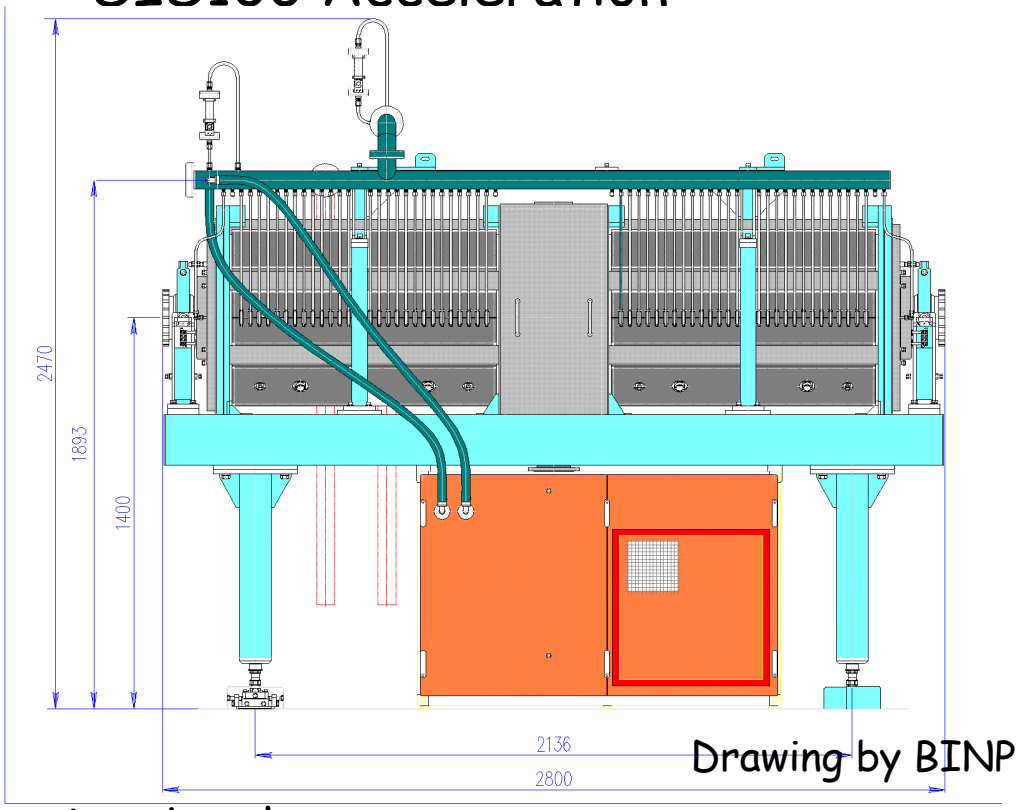
FAIR RF Work Packages (2/2)

- COMMON RF SYSTEMS
  - Digital Low-Level RF Control for Synchrotrons & Storage Rings (Digital_LLRF_Sync)
  - pLINAC Low-Level RF Control (LLRF_pLINAC)
  - pLINAC Power Amplifiers (pLINAC_AMP)
  - Modular Driver Amplifiers (Driver_Amplifiers)
  - Gap Periphery (Gap_Periphery)
- SUPPLY UNITS
  - Supply Units for SIS100, SIS300 and NESR Accelerating Systems (SU_SIS100_300_NESR)
  - Supply Units for SIS100 Barrier Bucket Systems and Longitudinal Feedback System (SU_BB_Long_Feedb)
  - Supply Units for CR Debuncher and SIS100 Bunch Compression (SU_CR_SIS100BC)
  - Supply Units for SIS18 h=2 System (SU_SIS18)
  - Supply Units for pLINAC RF Systems (SU_pLINAC)

Reference: H.Klingbeil et al.: "FAIR RF Work Packages"

SIS100 - FAIR EoI 13b: RF Systems

SIS100 Acceleration



Drawing by BINP

Tasks:
- Main RF system of the SIS100
- Acceleration (*h=10*)
- AP Batch compression (t.b.d.)

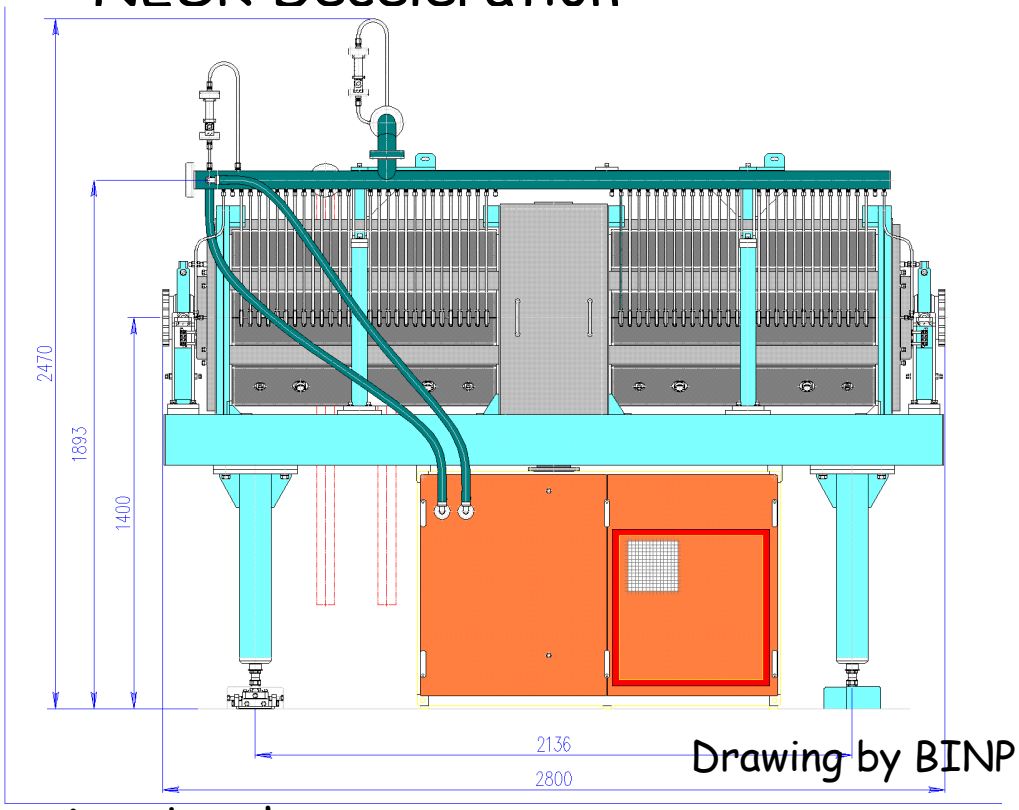
Main Parameters (one of 14/20 RF units):

Frequency (MHz)	$1.1 < f \leq 2.7$
Gap voltage (kV)	0.03 to 20
Duty cycle	c.w.
Aperture of the beam pipe, circular diameter (mm)	150 (CF160)
Installation length, flange to flange (m)	2.8
Installation width (m)	±0.70
Installation height around beam axis (m)	+ 0.50 / -1.40
Height of beam axis (m)	1.4
Pressure of beam pipe (mbar)	$\leq 1 \cdot 10^{-12}$
In situ heating of the cavity beam pipe (°C)	300

Design sketch:
Two inductively loaded (ferrite) coaxial quarter wave resonators operating on a single gap. Indirect water cooling of ferrites. Resonant frequency controlled by ferrite biasing.
Capacitively coupled singled ended tetrode amplifier.

SIS100 - FAIR EoI 13b: RF Systems

NESR Deceleration



Drawing by BINP

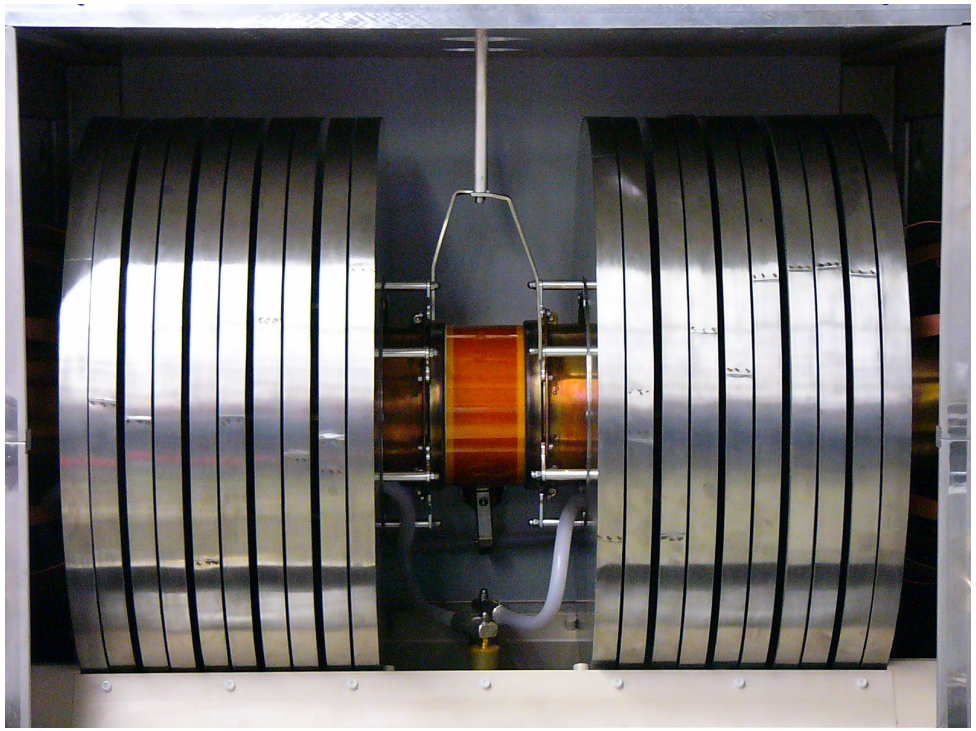
Design sketch:
Two inductively loaded (ferrite) coaxial quarter wave resonators operating on a single gap. Indirect water cooling of ferrites. Resonant frequency controlled by ferrite biasing.
Capacitively coupled single-ended tetrode amplifier.

Tasks:
- Main RF system of the NESR
- Deceleration of RIBs and APs at different harmonic numbers (1-8)

Main Parameters (one RF unit):

Frequency (MHz)	$0.99 < f \leq 2.3$
Gap voltage (kV)	0.05 to 15
Duty cycle	c.w.
Aperture of the beam pipe, circular diameter (mm)	200 (CF200)
Installation length, flange to flange (m)	2.8
Installation width (m)	±0.70
Installation height (m)	+ 0.80 / -2.00
Height of beam axis (m)	2.0
Pressure of beam pipe (mbar)	$\leq 1 \cdot 10^{-11}$
In situ heating of the cavity beam pipe (°C)	300

SIS100 Bunch Compression



Design Sketch:
Two inductively loaded (MA) quarter wave coaxial resonators operating on a common gap.
Air cooling of MA cores.
Push-Pull Amplifier consisting of two tetrodes.
Design based on existing SIS18 BC (see above).

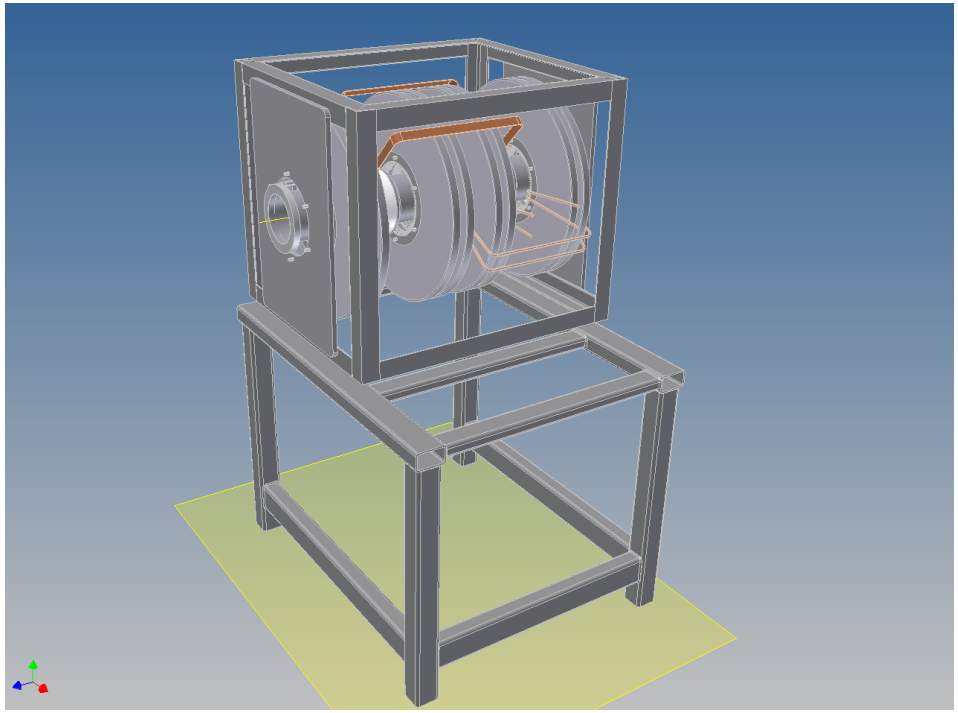
Tasks: • Bunch compression by rotation of bunches in phase space *(h=2)*

Main Parameters (one of 9/16 RF units):

Frequency (MHz)	$0.395 \leq f \leq 0.485$
Gap voltage (kV)	1 to 40
Duty cycle	$3 \cdot 10^{-4}$ ($5 \cdot 10^{-4}$)
Maximum pulse duration (µs)	300 (500)
Maximum repetition rate (Hz)	1
Aperture of the beam pipe, circular diameter (mm)	150 (CF160)
Installation length, flange to flange (m)	1
Height of beam axis (m)	1.4
Pressure of beam pipe (mbar)	$\leq 1 \cdot 10^{-12}$
In situ heating of the cavity beam pipe (°C)	300

SIS100 - FAIR EoI 13b: RF Systems

SIS100 Barrier Bucket



Design Sketch:
Inductively loaded (MA) quarter wave resonator. Two gaps connected in parallel. Inductively coupled (two figure of 8 coupling loops) push-pull amplifier consisting of two tetrodes. Rectangular offset pulses to generate single sine waves.

Tasks: • Precompression by moving single sine wave barriers.

Main Parameters (one of two RF units):

Frequency (MHz)	1.5
Max. barrier voltage (kV)	15
Duty cycle	20% (3.2%)
Aperture of the beam pipe, circular diameter (mm)	150 (CF160)
Installation length, flange to flange (m)	1
Height of beam axis (m)	2.0
Pressure of beam pipe (mbar)	$\leq 1 \cdot 10^{-12}$
In situ heating of the cavity beam pipe (°C)	300