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Frontend Electronics for high-precision single photo-electron timing (PANDA)

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High-precision single photon timing with resolutions well below 100 ps is becoming increasingly important. It enables new detector designs, like the Time-of-Propagation DIRC of Belle II, or the TORCH upgrade for LHCb, and to improve existing designs, e.g. allow chromatic corrections in DIRCs. These applications have in common a high channel density, limited available space and low power consumption.
We report on Frontend Electronics developed for the PANDA Barrel DIRC. The customised design utilises high-bandwidth pre-amplifiers and fast discriminators providing LVDS output signals which can be directly fed into the TRBv3 readout using FPGA-TDCs with a precision better than 20ps RMS. The discriminators also provide Time-over-Threshold (ToT) information which can be used for walk corrections thus improving the obtainable timing resolution. Two types of cards, optimised for reading out 64-channel Photonis Planacon MCP-PMTs, were tested: one based on the NINO ASIC and the other, called PADIWA, on FPGA-based discriminators. Both types feature 16 channels per card, thus requiring four cards to read out one 64-channel MCP-PMT. Power consumption for the complete readout of one Planacon MCP-PMT is approx. 10W for the NINO FEE and approx. 5W for the PADIWA FEE.
The timing performance of the cards was tested with a fast laser system and also in a test experiment at the MAMI accelerator in Mainz using a small DIRC prototype to image Cherenkov patterns. In both cases, using the ToT information, a timing resolution of better than 100ps was found for the complete readout chain.

Primary author: CARDINALI, Matteo (HIM)

Presenter: CARDINALI, Matteo (HIM)

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