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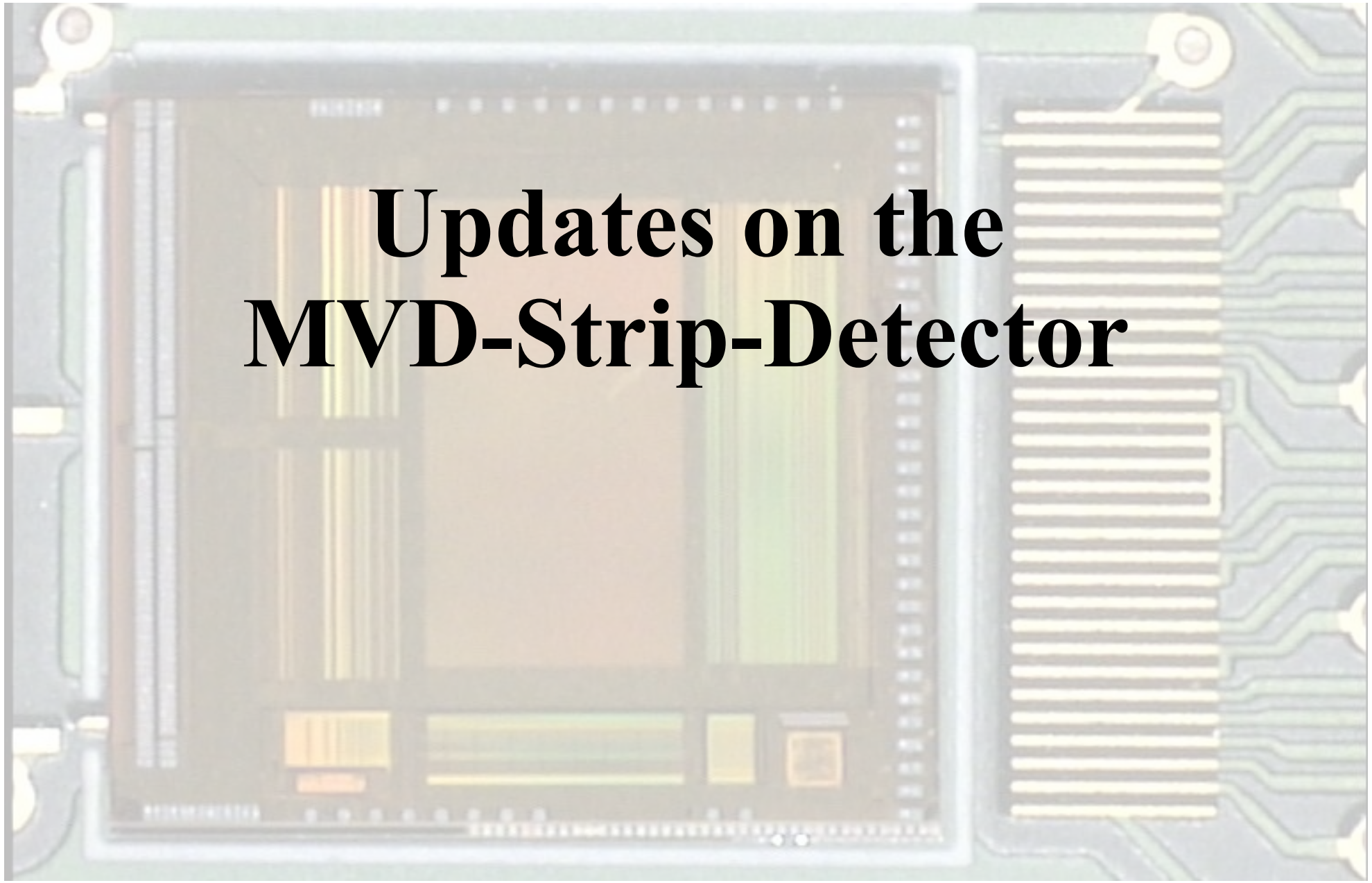


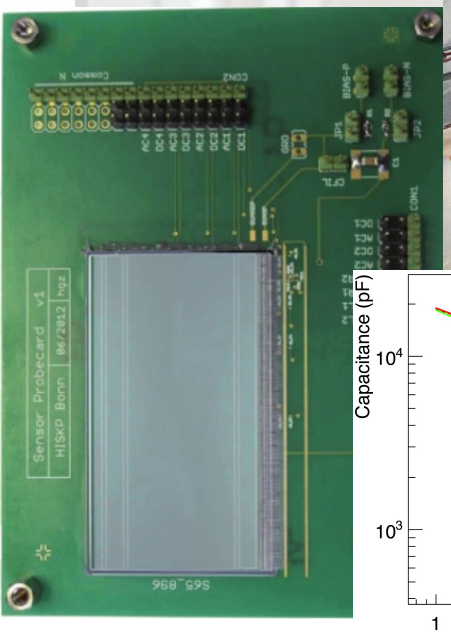
Updates on the MVD-Strip-Detector

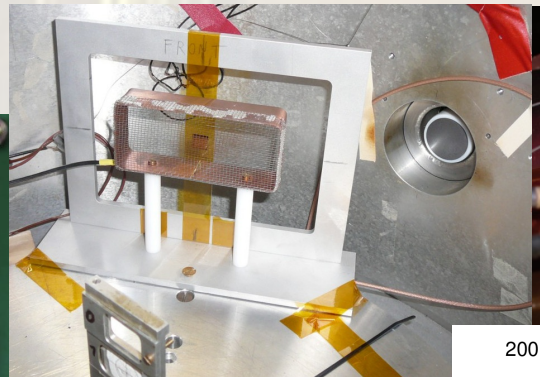
PANDA Front-end and DAQ Workshop, Alba, April 28-30, 2013

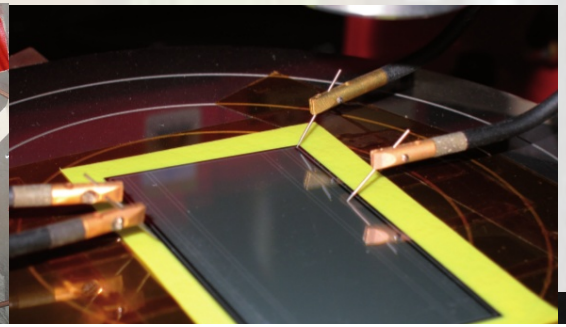
Detector Development

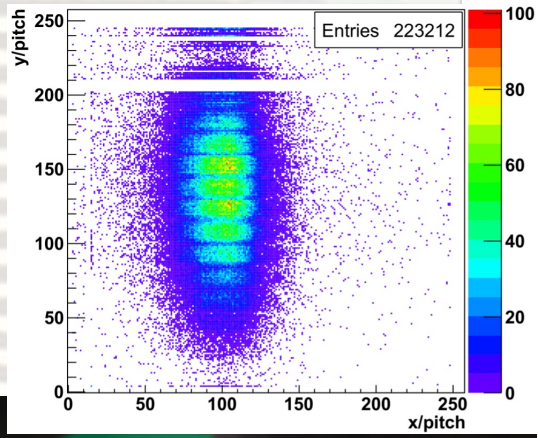
- barrel sensors been intensively tested
- new engineering run submitted beginning 2013

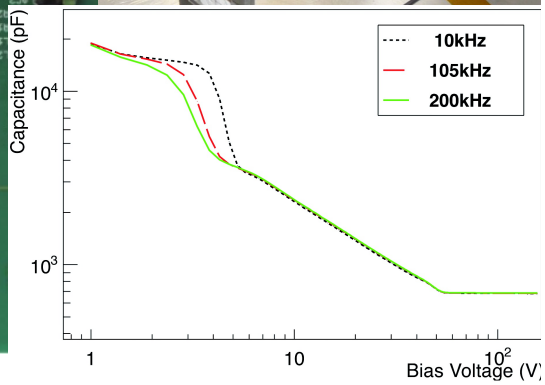
→ investigate different biasing method

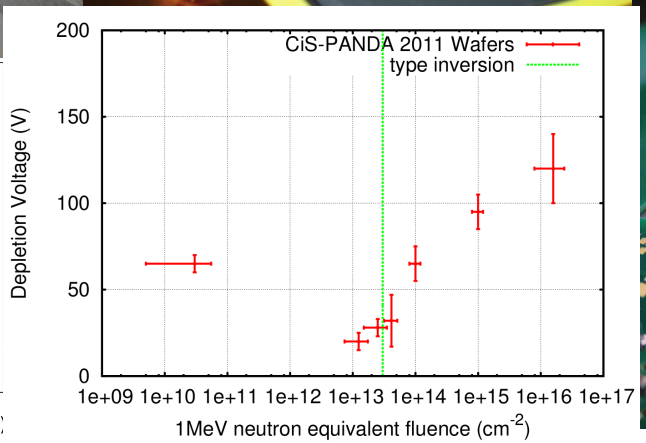


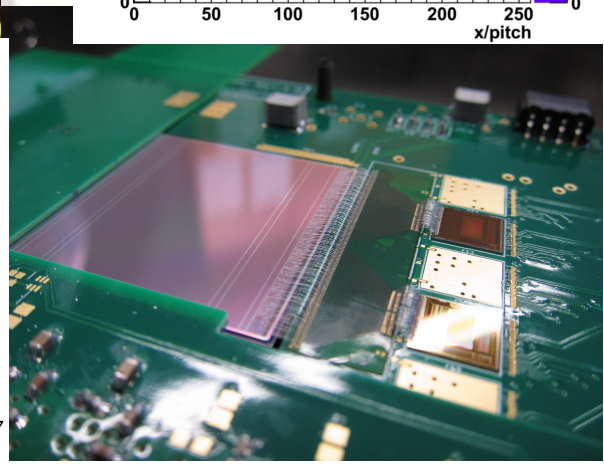








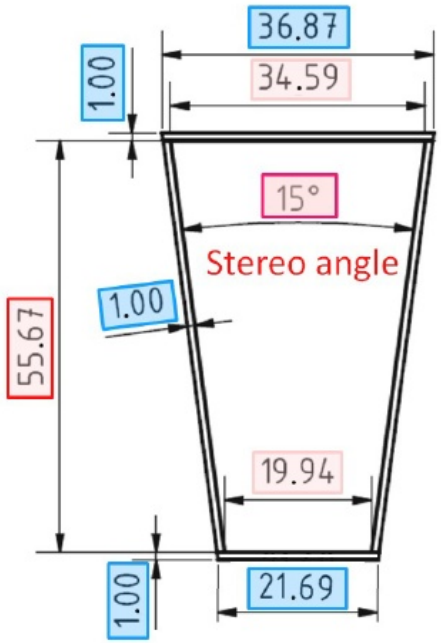




Detector Development

- disk sensors engineering run arrived @Jülich
- CiS Erfurt, same technology as barrel sensors

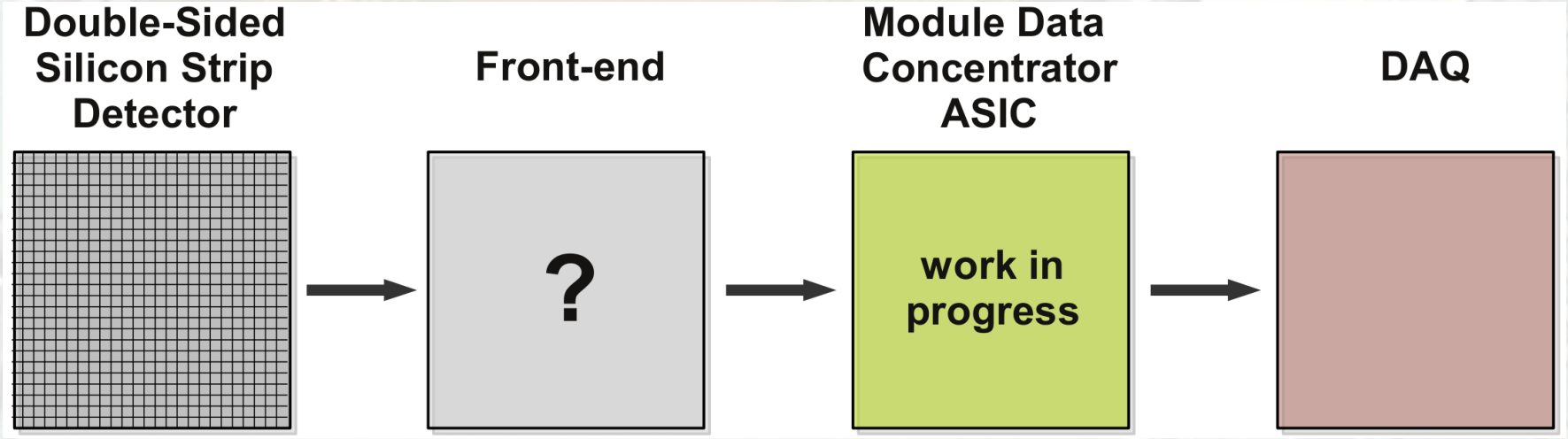
strip implants:	512 p^+-strips in n-substrat and 512 n^+-strips for the backside.
Strip orientation:	parallel to the long sensor edges, skew angle = 15°
pitch:	67.5 µm
Biasing:	punch-through
n-side charge sep:	p-spray
height:	57.67 mm
thickness:	250 – 300 µm



MVD group Jülich

Front-end Status

- decision for the strip detector front-end made
- based on TOFPET ASIC (EndoTOFPET-US coll.)
- modifications towards silicon strip detectors already started at INFN Torino



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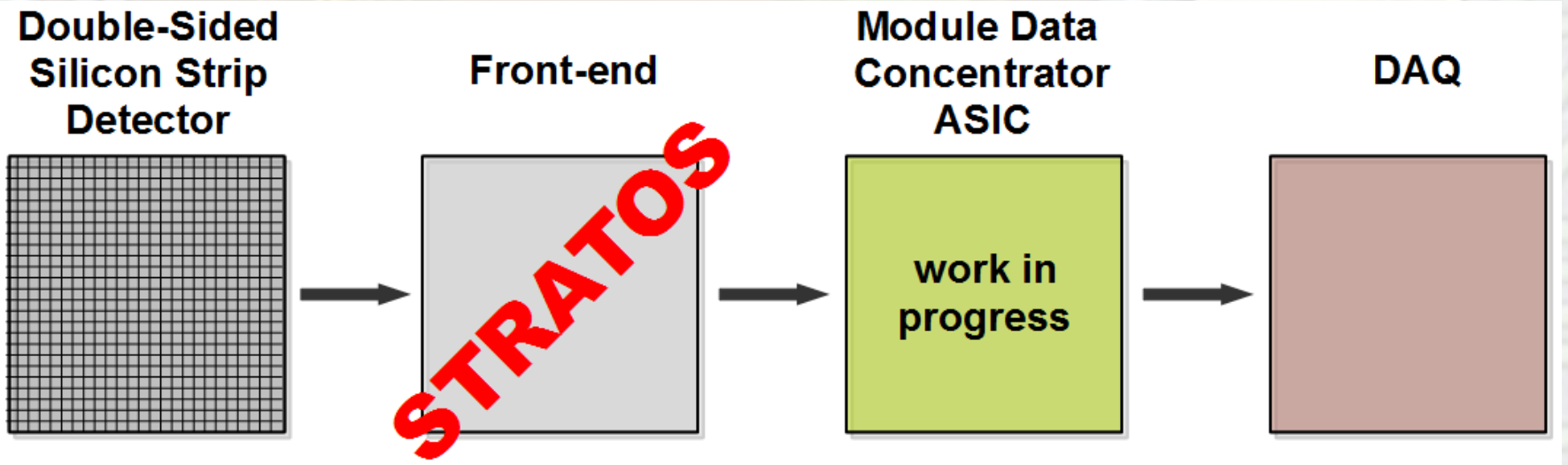


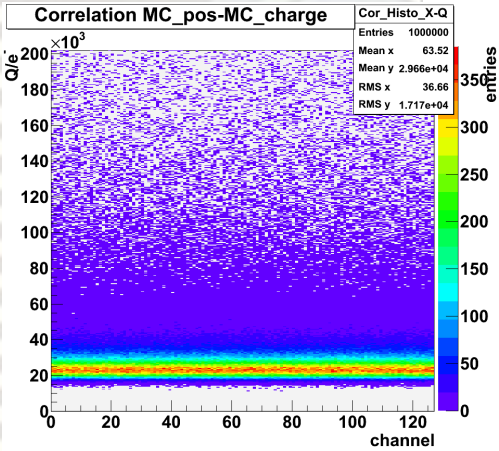
Front-end Features

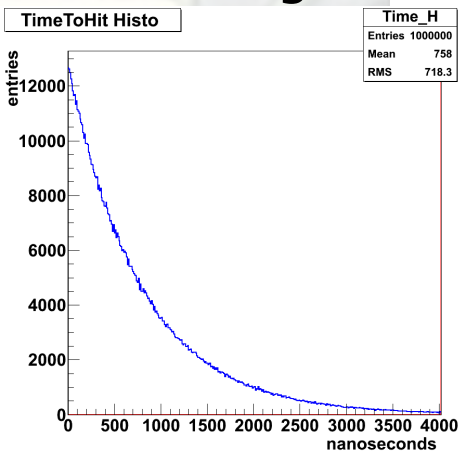
- self-triggering, fully digital data output
- analog part customized to sensor capacitance
- short ToT to avoid pile-up
- fast sampling (binning ~100ps)
  - using TDCs based on time interpolation
- high digitization resolution
  - clustering to improve spacial resolution
  - energy loss information as additional PID input

MVD group Turin

Strip Front-end Simulation

- fast and flexible using C++ and Root to compare with VHDL simulations
- Features (so far):
  - adjustable number of channels (64 vs. 128)
  - adjustable sensor thickness (charge)
  - uniform distribution in position, landau distribution in charge
  - double strip hit with charge sharing (CoG)
  - exponential distribution in time
  - wave-form from device simulation
  - … work in progress





MVD group Gießen

MVD Strip-Detector count

	Barrel Part	Disk Part	**Sum**
Sensors	184 rectangular 64 square	48 trapezoidal	**296**
Front-ends	2536 (64 ch)	768 (64 ch)	**3304**
DC-DCs	1240	240	**1480**
MDCs	248	48	**296**

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Gießen Infrastructure

- installed beginning of April
- size: 3,00 x 3,50 m², internal height: 2,20 m
- approx. 10m² clean room space
- designed for ISO 6
- measured to comply better then ISO 6

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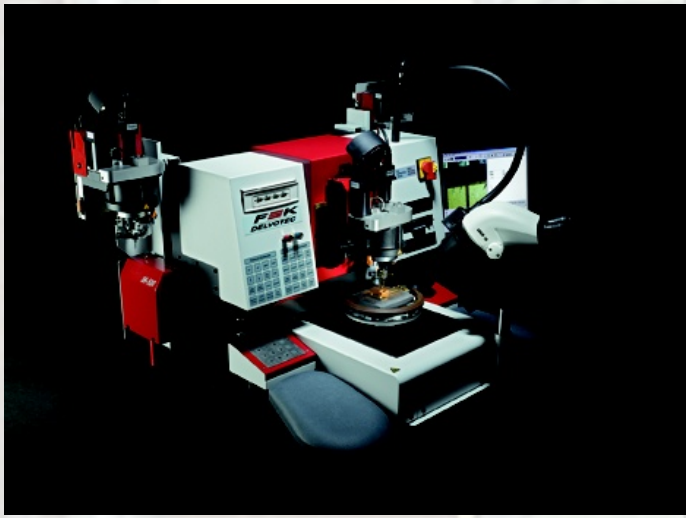
MVD panda

panda

Gießen Infrastructure

bonding machine:
F&K Delvotec 5630
already in Gießen
will be assembled soon

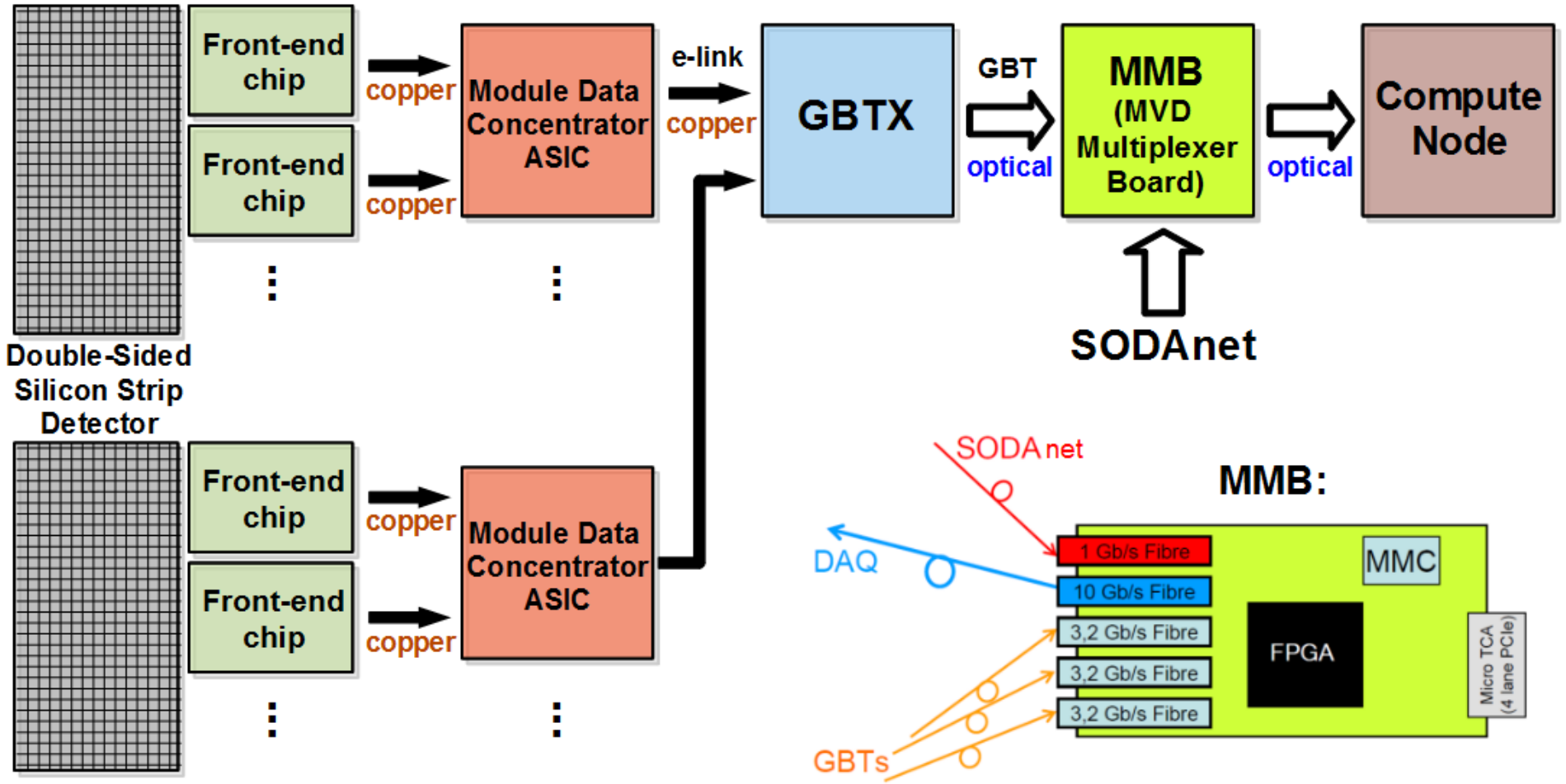


PA200 BlueRay

200 mm Semi-Automatic Probe System with BlueRay Technology

wafer prober:
Cascade Microtech PA200BlueRay
ordered

Strip-DAQ-Chain

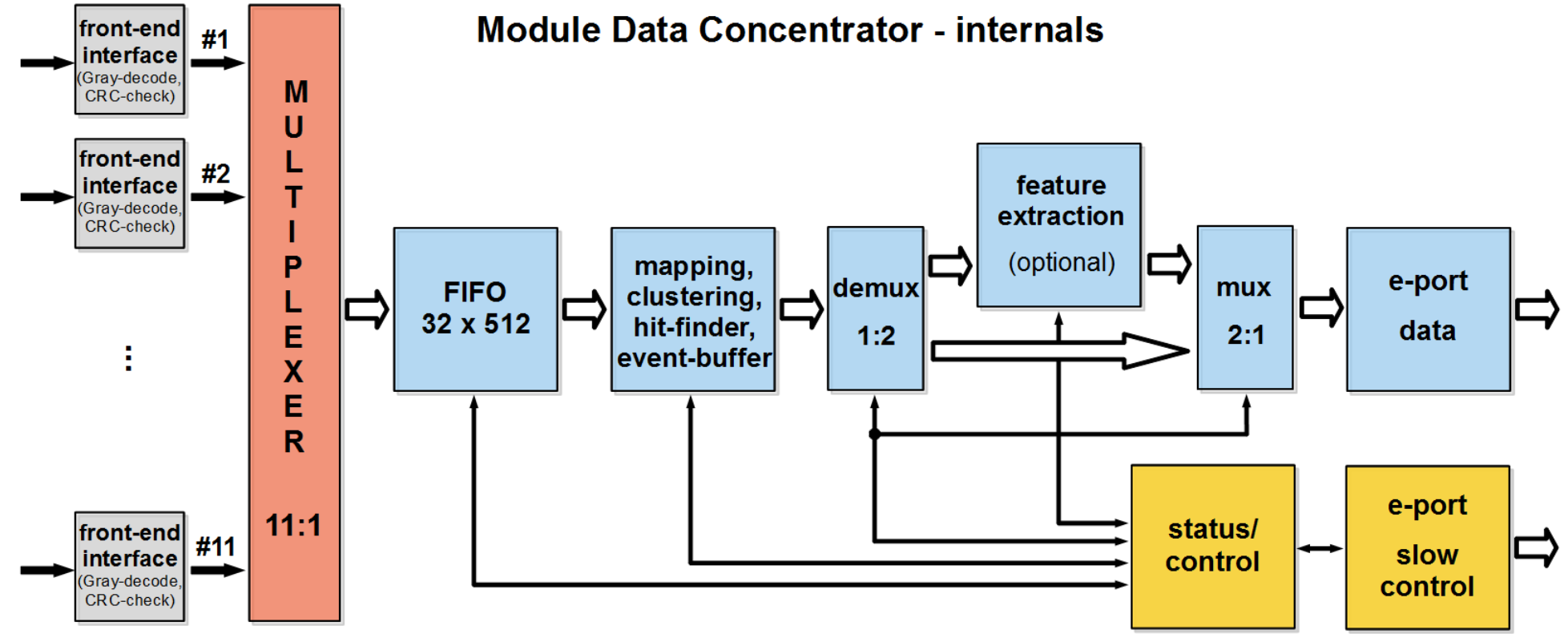


Module Data Concentrator

- all front-ends of one strip sensor connected to one module data concentrator ASIC (MDC)
- front-end data:
  - strip address
  - time information
  - ToT
- e-links (GBT) will be used for data transfer and slow control

H. Sohlbach, FH Iserlohn

Module Data Concentrator



H. Sohlbach, FH Iserlohn

Module Data Concentrator

- Status as of April 2013
  - design versions: with/without feature extraction
  - design & simulation of FPGA prototype (VHDL-based) finished for:
    11:1 multiplexer, FIFO, clustering/hit finding
  - in design/redesigning:
    triple redundancy, clustering/hit finding, e-link, status/control
  - work on the specification of the front-end/module controller interface in progress

H. Sohlbach, FH Iserlohn

Summary

- strip front-end in development
- MDC in development

=> both developed for the specific requirements of the PANDA MVD

- feature set customized to our requirements
- no dependence on external developments

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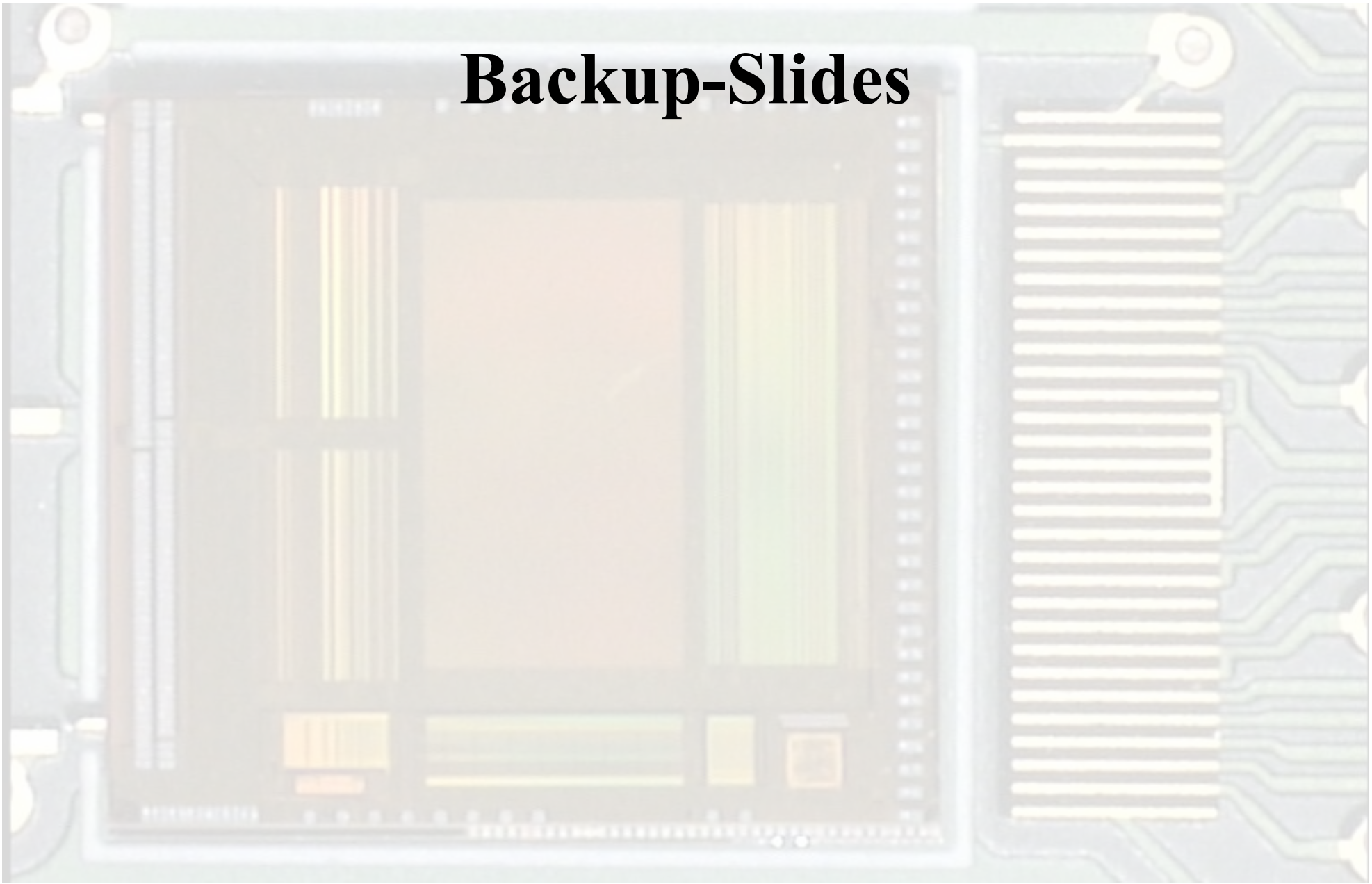
Thank you for your attention

STRATOS = **ST**rip **R**eadout **A**SIC **TO**rino **S**olution
(Lancia Stratos)



Backup-Slides

Pile-up

- short ToT to avoid pile-up: $P_{pile-up} = 1 - e^{(-\dot{N}_{chn} \cdot t_{ToT})}$

assuming 36ns ToT (5fC ~ 1 MIP in a single strip):
P(pile-up) = 0.036% @ 10kHz channel hit rate (SF=1)
P(pile-up) = 0.072% @ 20kHz channel hit rate (SF=2)
P(pile-up) = 0.144% @ 40kHz channel hit rate (SF=4)

assuming 60ns ToT (10fC ~ 2 MIP in a single strip):
P(pile-up) = 0.06% @ 10kHz channel hit rate (SF=1)
P(pile-up) = 0.12% @ 20kHz channel hit rate (SF=2)
P(pile-up) = 0.24% @ 40kHz channel hit rate (SF=4)

(ToT based on device simulation from Valentino)

Gießen Infrastructure