JÜLICH
FORSCHUNGSZENTRUM

panda

Implementation of UDP into Jülich Readout System

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Outline

- Jülich Digital Readout System
  - Purpose & Structure
- Firmware Developments
  - LCD on the Board
  - Ethernet Connection
    - Single Register Handling
    - Block Data Transfer
    - First Performance Results
- Conclusion

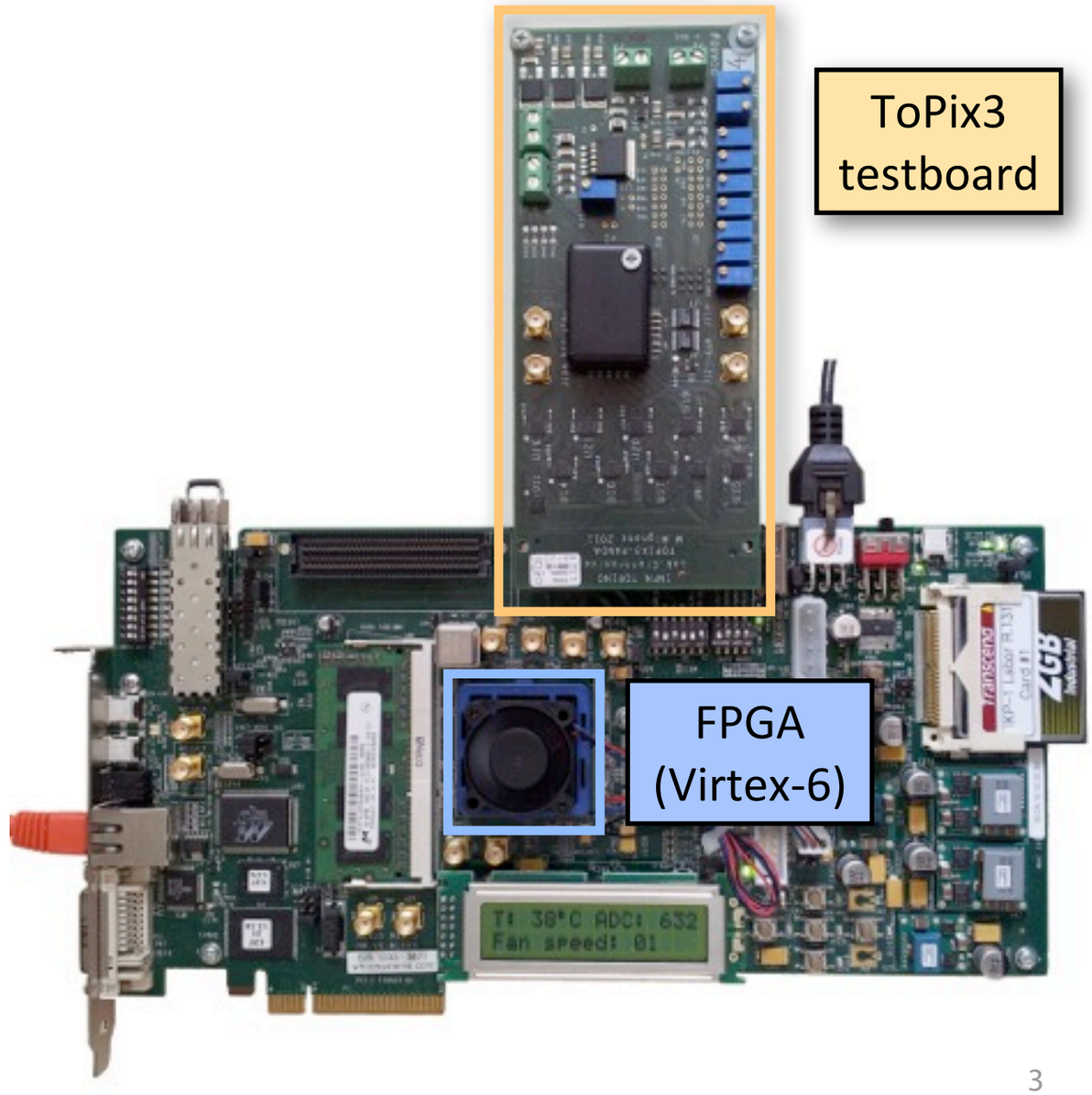
Concept of the Jülich Readout System

- Flexible system for readout of front-end chips under development
- Based on FPGA (Virtex-6), ML605 board from Xilinx
- Successful use in Jülich testbeam (Dez. 2012)
  up to 25 MBit/s

ML605
(ToPix3)

comm. link
up to now:
SIS1100

PC



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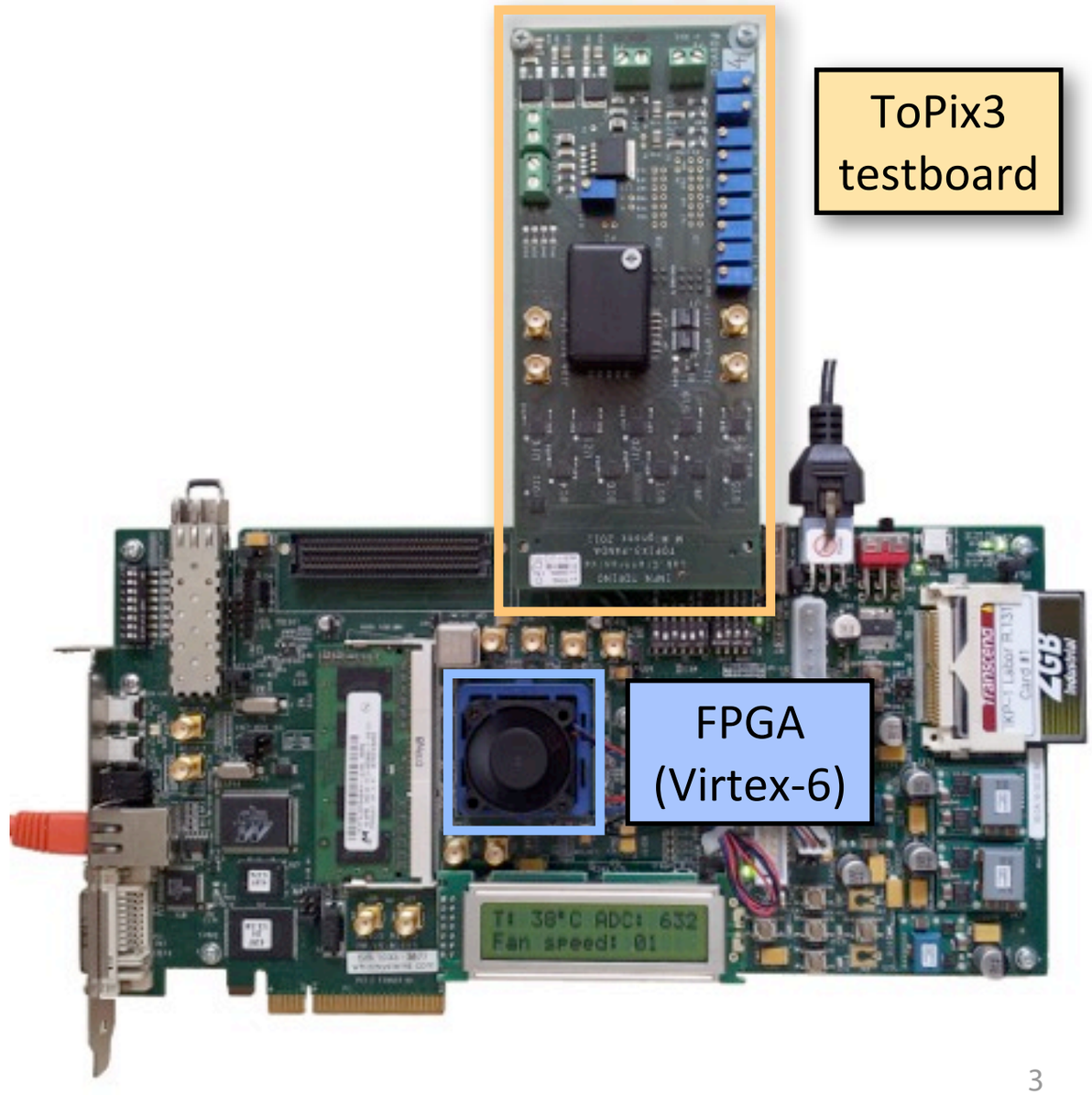
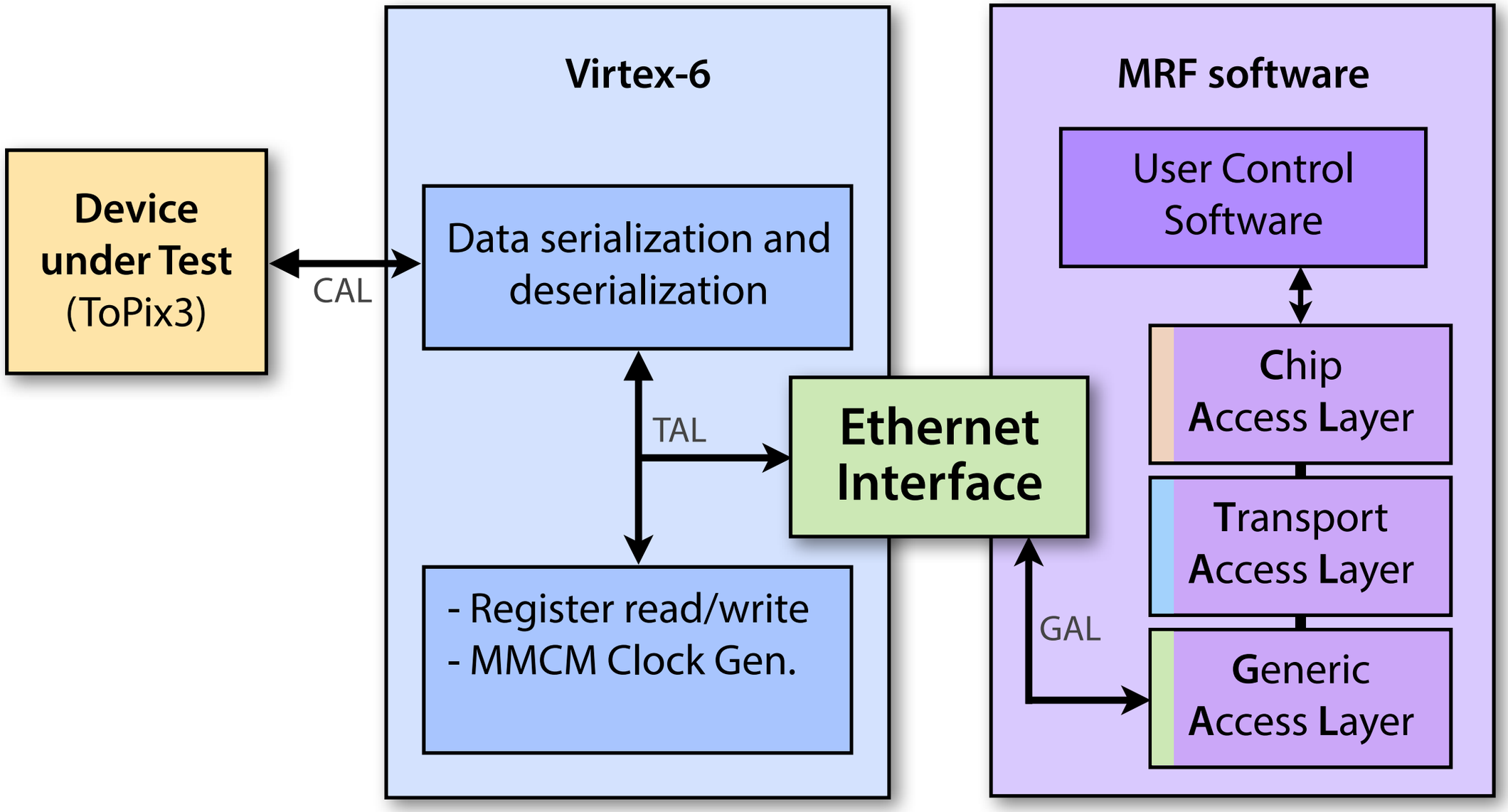
change to:
Gigabit Ethernet

PC



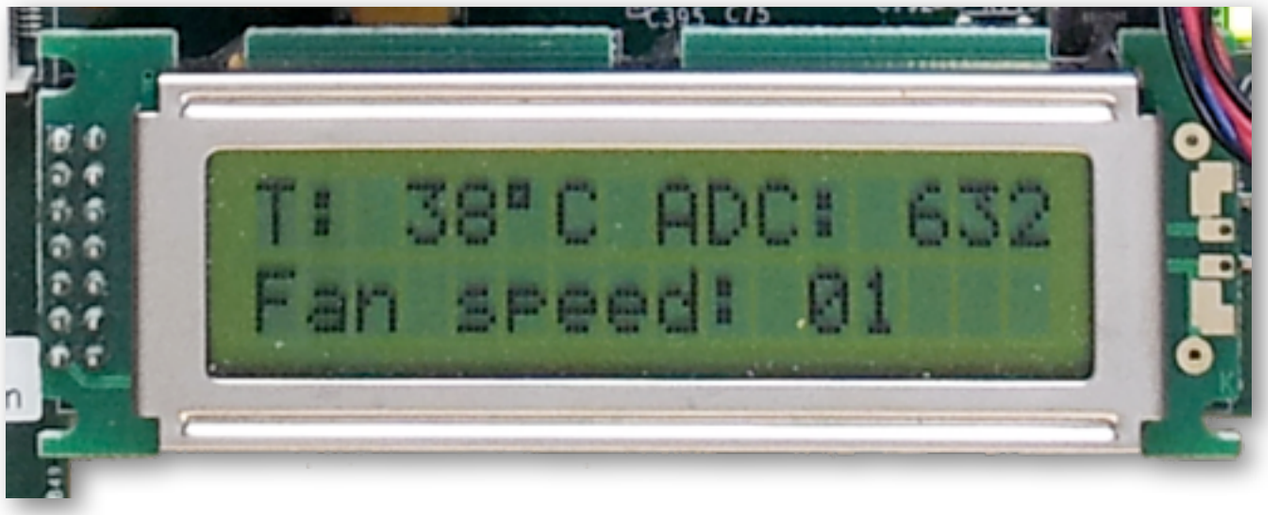
Structure of the Jülich Readout System

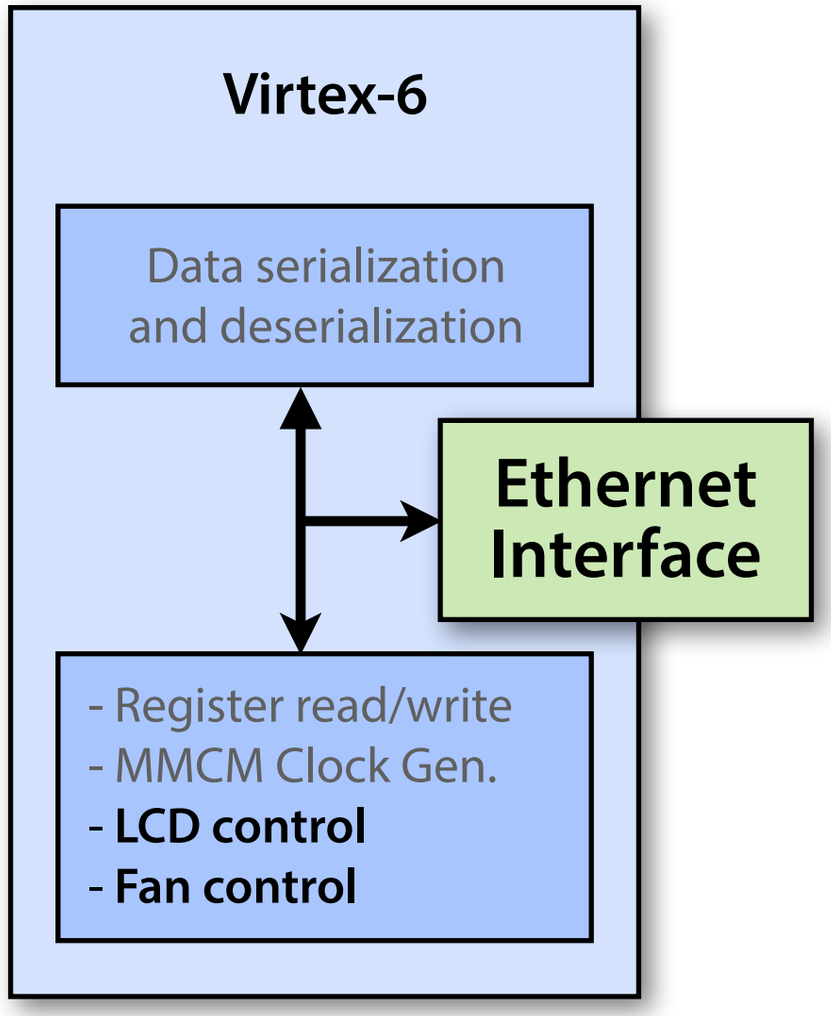


MRF: **M**VD **R**eadout **F**ramework

Simplification of Development

- Use built-in LCD
  - Easily adaptable to user's needs
  - Example:
    FPGA temperature and fan speed





- Temperature in °C
- ADC value of the temperature
- Fan speed setting:
  from »01« [slow] to »20« [fast]

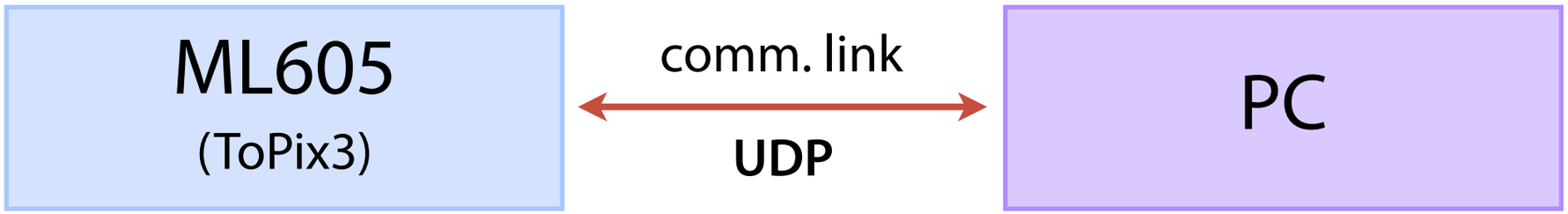
Why Change to Ethernet (UDP)?

- **Advantages**
  - + Almost no investment costs
    (Compared to ~1500 € for SIS1100)
  - + No additional drivers on PC side
  - + Useable with notebook
  - + UDP feasible for FPGA
  - + Additional communication link on ML605

- **Disadvantages**
  - – Development needed
  - – No validation for receiving in UDP

UDP: **U**ser **D**atagram **P**rotocol

Single Register Handling



Register Handling
read and set firmware parameter

Request Process
send a request to ML605 and get a result back

Configure CLK generator
built-in clock generator (MMCM) drives ToPix3

Include into MRF
existing framework uses UDP standard

Configure ToPix3
set several configuration parameter for the chip and readout to confirm

Read ToPix3 data
data are put into buffer (DMA), single readout

Single Register Handling - Performance

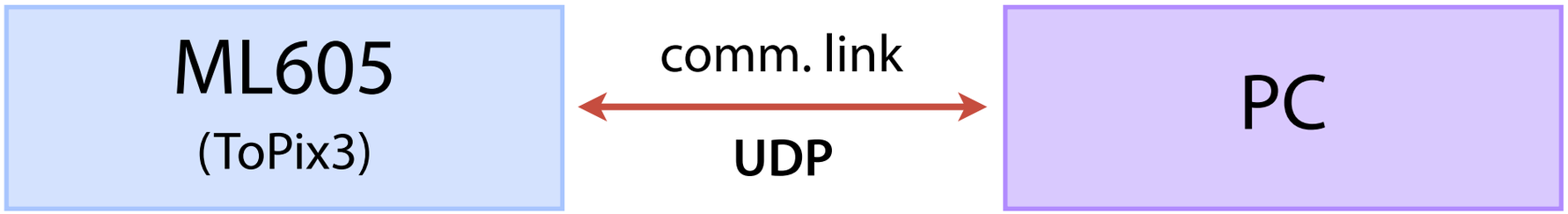
- Performance Test:
  - read register 10^6 times
  - SIS: ~ 4.7 Mbit/s
  - UDP: ~ 0.9 Mbit/s

=> ~ factor 5 slower

- Reasons:
  - Software not yet performance optimized
  - UDP overhead per package
    - only for single register

Package Contribution	
Compl. Header:	46 Byte
Data Word:	4 Byte

Block Data Transfer (DMA)



Process DMA Request
read the DMA buffer and create UDP package

Request Process
send a request to ML605 and get a result back

Read Requested Amount
stop after the requested amount is reached

Include into MRF
existing framework uses DMA over UDP

Stop if DMA is Empty
only send valid data

Recv. Multiple Packages
send multiple DMA pkg. with one request

Multiple DMA Packages
send multiple DMA pkg. with one request

Performance Test
check transfer speed for different request sizes

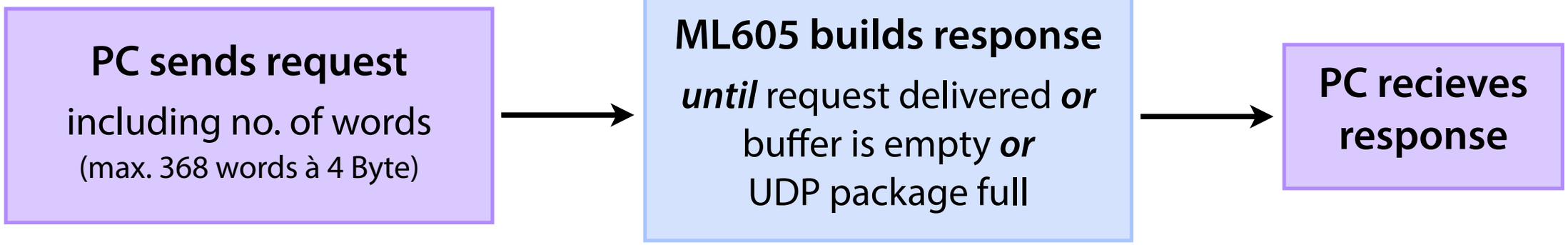
Block Data Transfer (DMA) - Performance

- Performance Test:
  - read 10^7 entries from DMA buffer
  - SIS: ~ ? Mbit/s (during last testbeam in Jülich ~ 25 Mbit/s)
  - UDP: ~ 45 Mbit/s

- Ongoing Optimizations:
  - Only request once, send multiple packages
    - First implementation stops after one UDP package is full
  - Data handling inside software

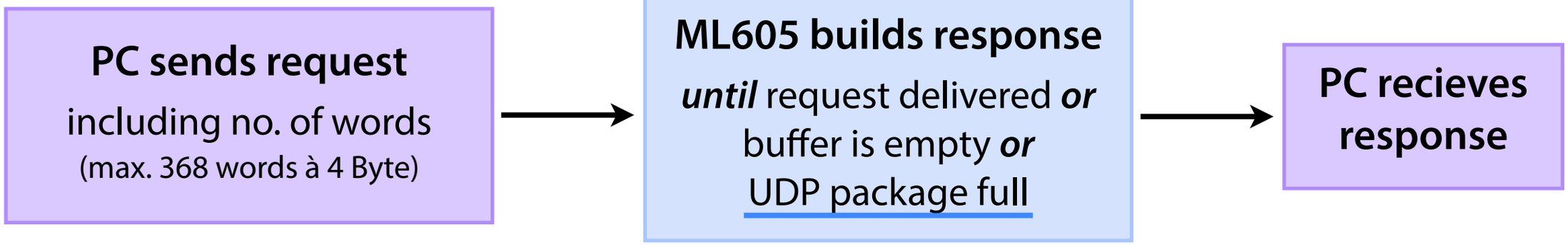
»Multi« Block Data Transfer

first version:

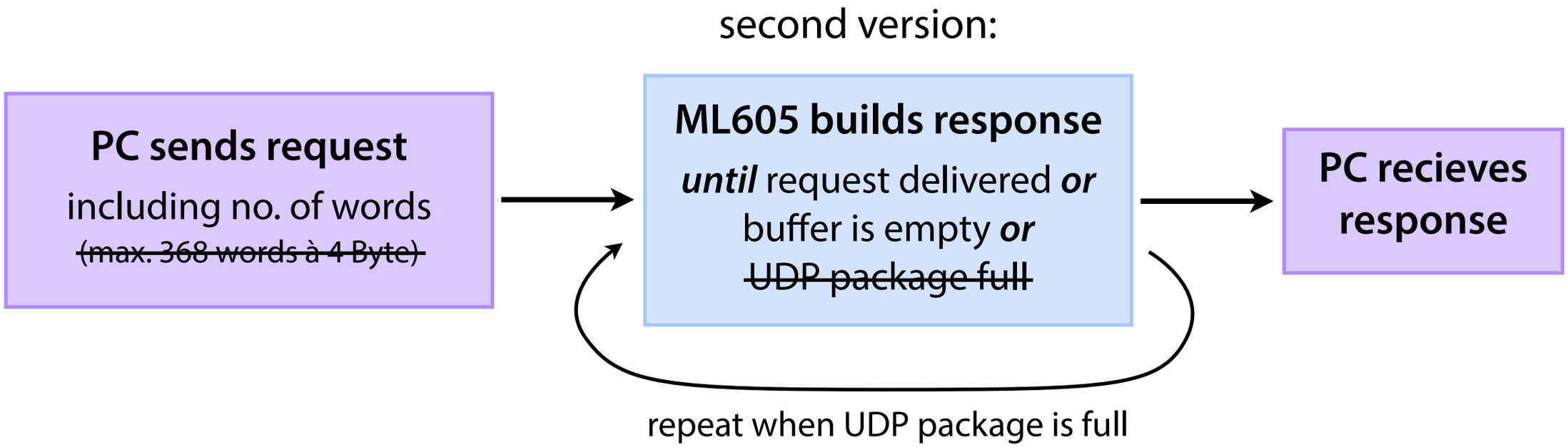


»Multi« Block Data Transfer

first version:



»Multi« Block Data Transfer



- Multiple packages with one request
  - ML605 firmware: ✅
  - MRF framework: ⚙️

Conclusion

- Jülich Digital Readout System
  - Modular structure with ML605-board
    - Easily adaptable to custom chip development
  - Successful use at Jülich testbeam
- Communication to PC
  - Switch to UDP standard
    - Optimizations in progress
  - Usage of widely accessible hardware

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Thank you!

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