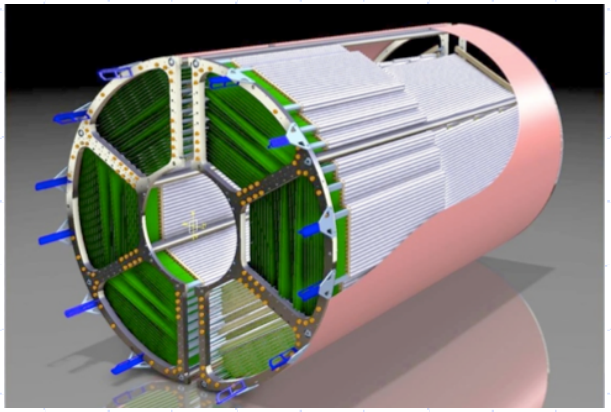
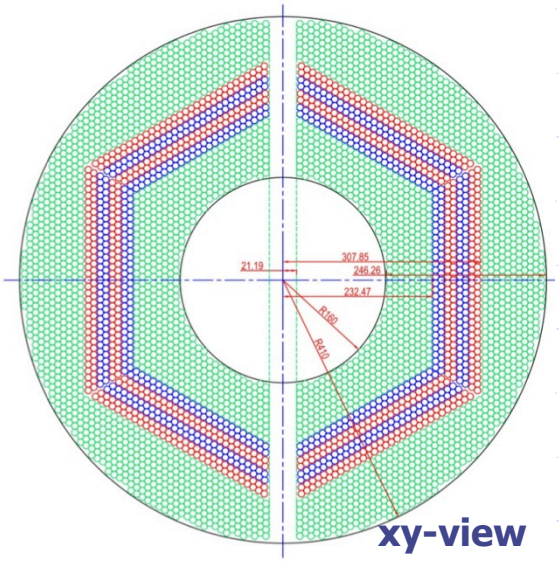


Updates on the STRAW front-end electronics

- STT layout;
- The readout concept;
- Electronics developments;
- Status and perspectives.

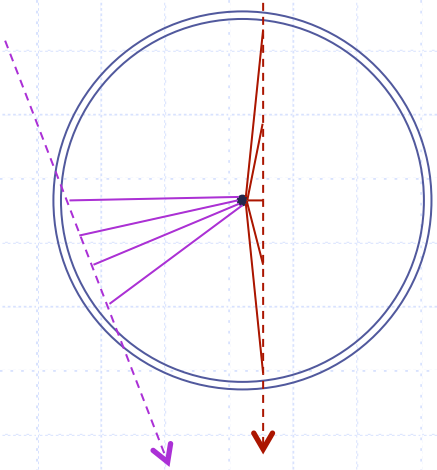
Detectors requirements and layout

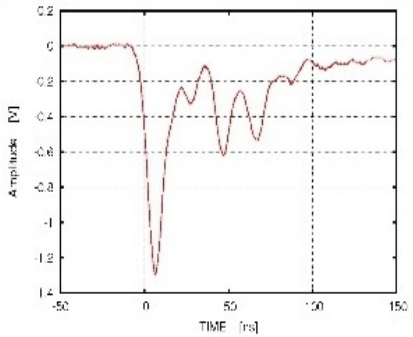
- 4636 Straw tubes arranged in planar layers (24-27)
- $\sigma_p/p \sim 3 - 4\%$ at B=2 Tesla
- $\sigma_{r\Phi} \sim 150(100)$ μm , $\sigma_z \sim 3.0(2.0)$ mm (single hit)
- Time readout (isochrone radius) drift time ~ 200 ns (B=2T)
  req. electronic resolution < 1 ns
  sensitivity (threshold) ~ 2 fC
- $\sigma_E/E < 8\%$ for PID < 1GeV/c
- Amplitude readout (energy loss)
- Straw tube capacitance: ~ 10-15 pF (9 pF/m)
  impedance: 373 Ω
  inductance:1.24 μH/m

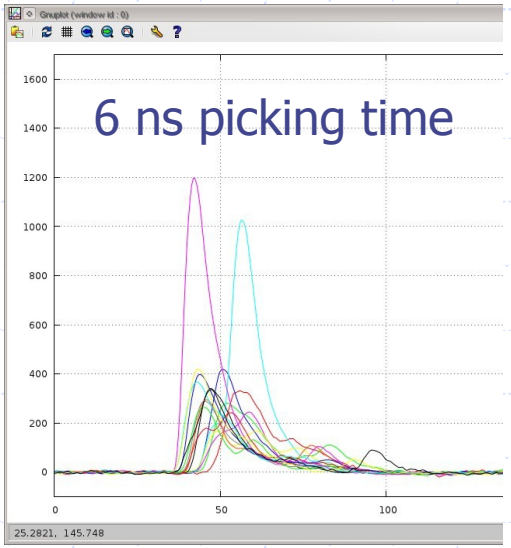


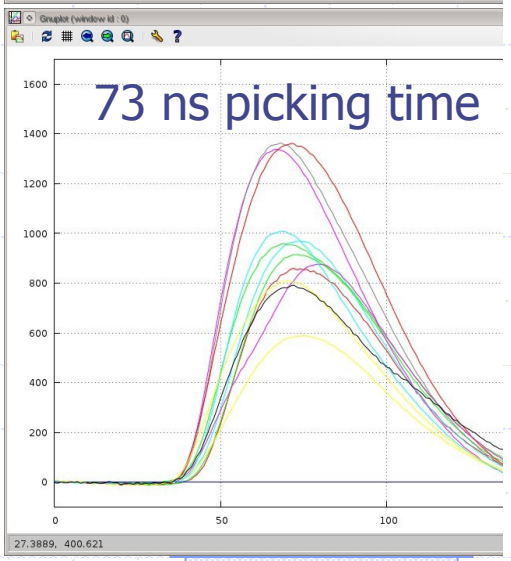
xy-view

Straw tube signal characteristics









Straw tube signals have a wide range of amplitudes and of shapes.

To precisely determine the position, a fast picking time is needed.

To measure energy loss, the signal should be integrated.

This requirements conflicts ⇒ a compromise should be found

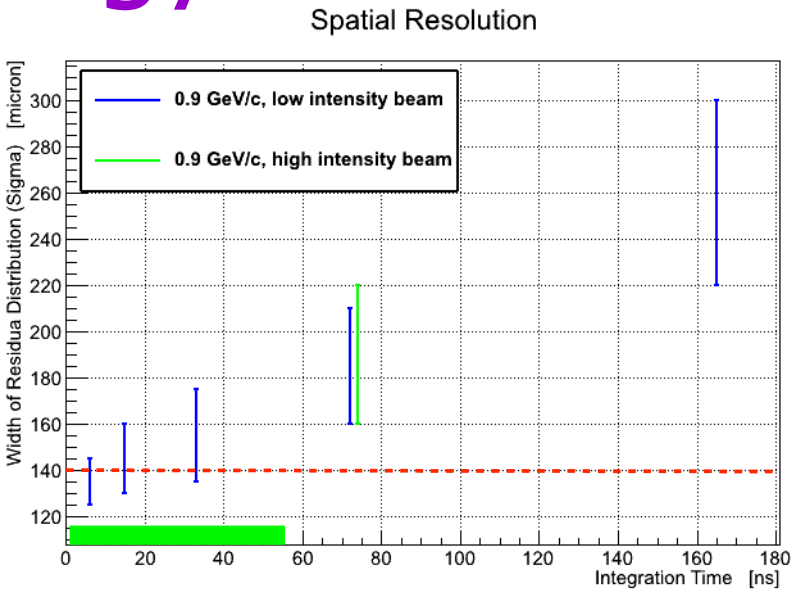
Spatial- and Energy resolution

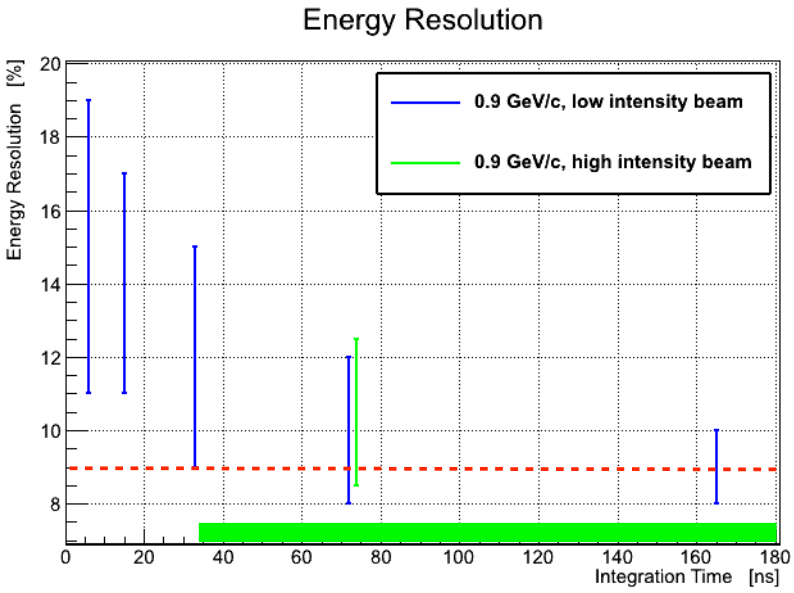
Spreads of obtained results origin from various gas amplification, threhold levels, discriminator type, track length, ….

Demanded spatial resolution: < 150 µm

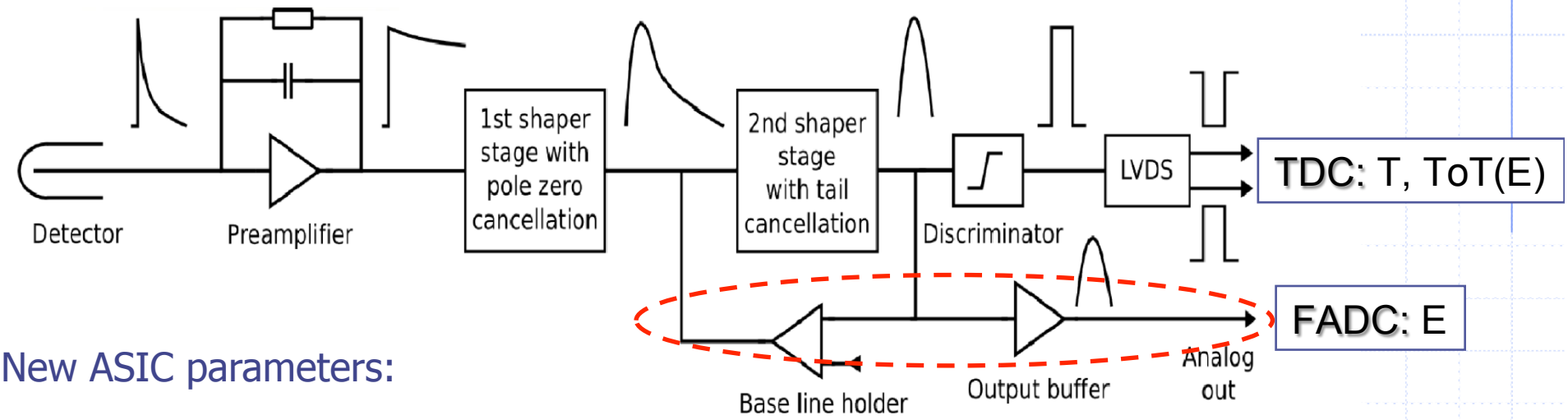
Demanded energy resolution: < 10 %

Results obtained K. Pysz





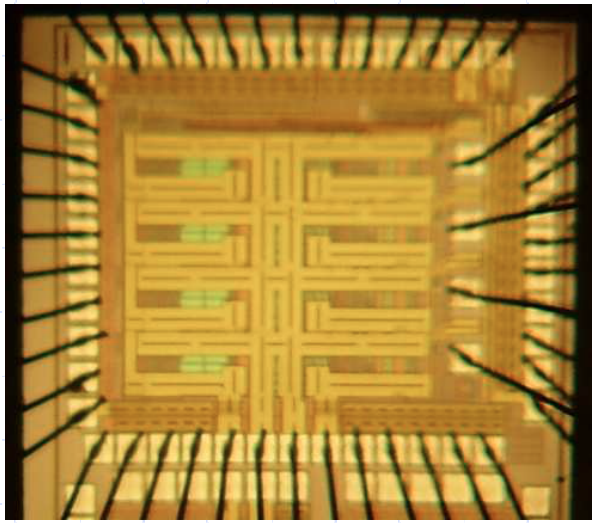
FEE readout concept



New ASIC parameters:

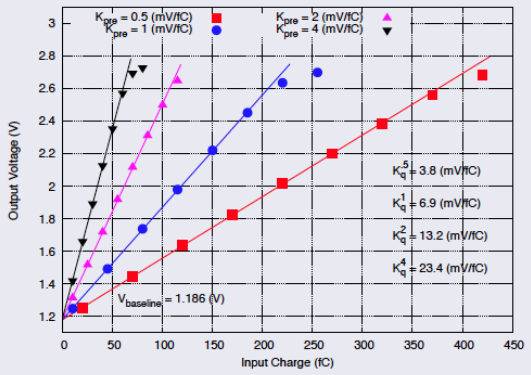
- Variable charge gain: 3 – 24 mV/fC
- Variable peaking time: 20 and 40 ns
- CR–RC2 shaping with Tail Cancellation
- BaseLine Holder – baseline independent on supply/temp. variation and high count rate
- Leading-Edge Discriminator for Time and ToT measurements
- Analog output

- AMS 0.35 µm CMOS
- Four Channels
- Channle Size: 1130Å~200 µm^2
- Power Consumption: 15.5 mW/ch + 12mW (LVDS)

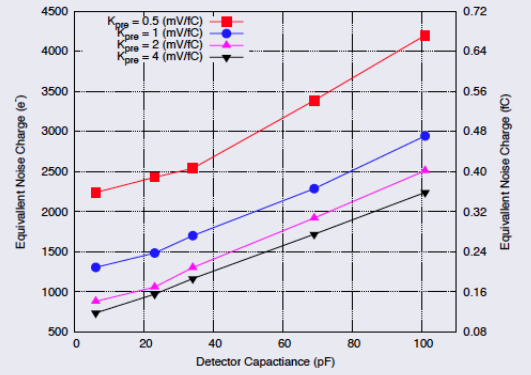


ASIC test measurements

Linearity

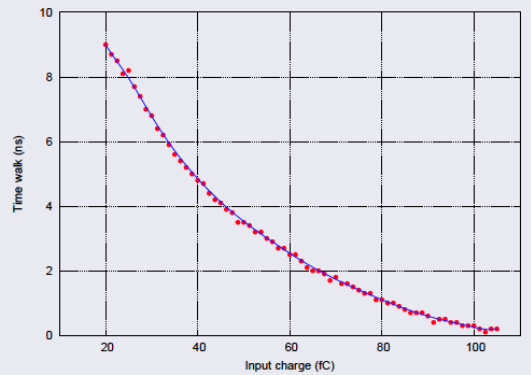


Equivallent Noise Charge

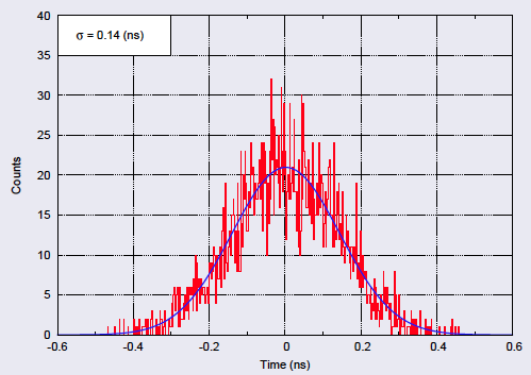


Test measurements with a delta pulse (D. Przyborowski)

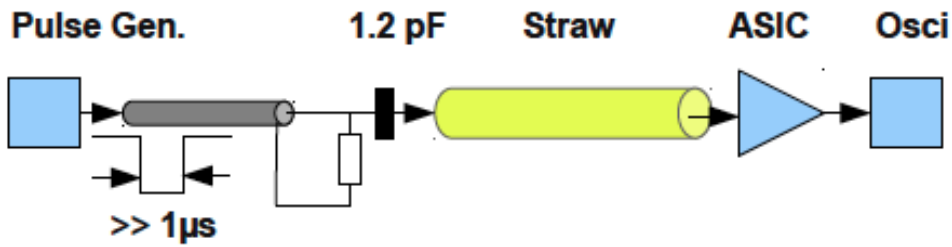
Time Walk



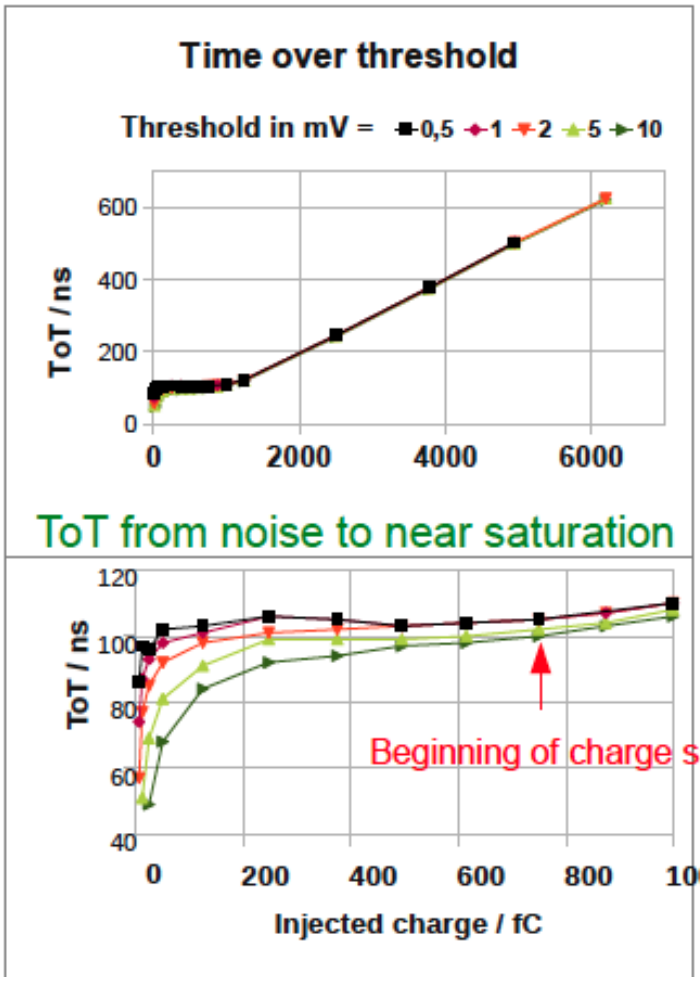
Jitter



ASIC input signals simulated by a pulse generator



Pulse rise time = 2.5 ns
Charge = 1.2 pC/V
Amplitudes from noise to saturation



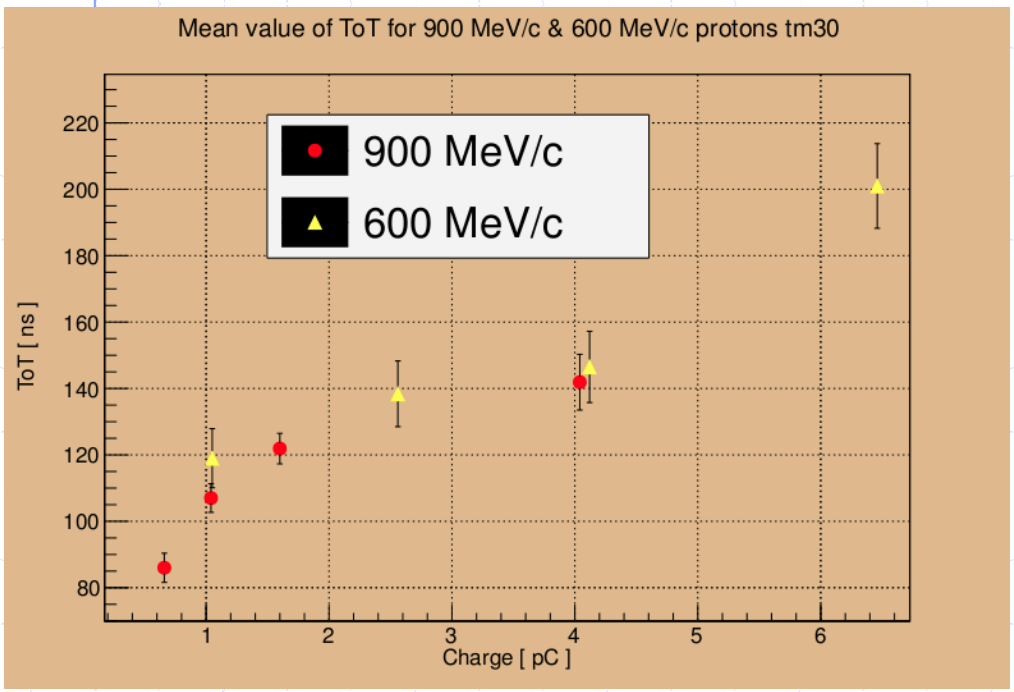
- Useful range of input charges is approx.
  1/3 of the dynamical charge range
- The dynamical range increases
  with increasing threshold.

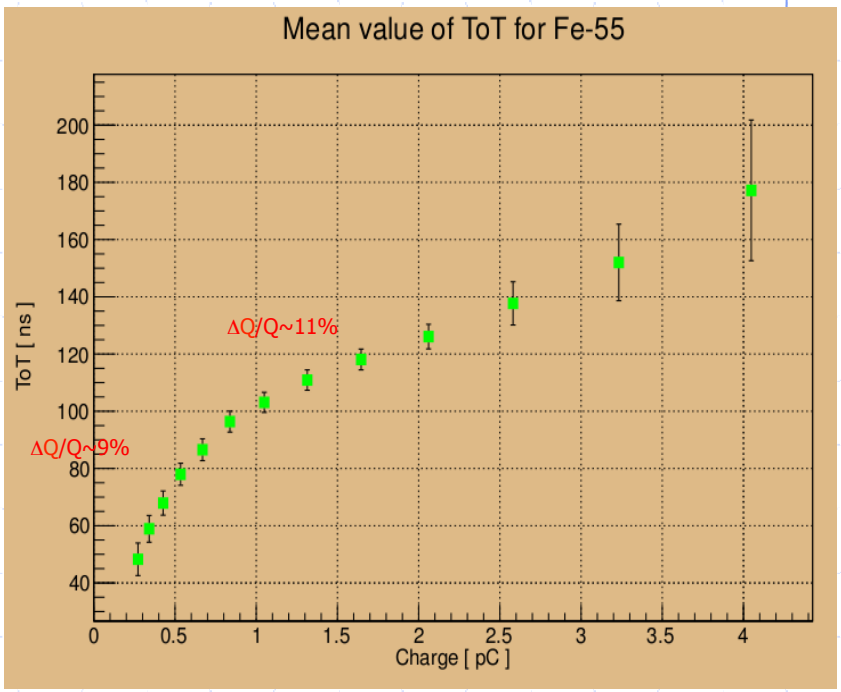
For rejection of the Landau tail:
The truncated-mean technique requires
good resolution also for large signals

Tests done in Jülich by H.Ohm

TOT with real ST signals

Measurement by P.Salabura
J.Biernat





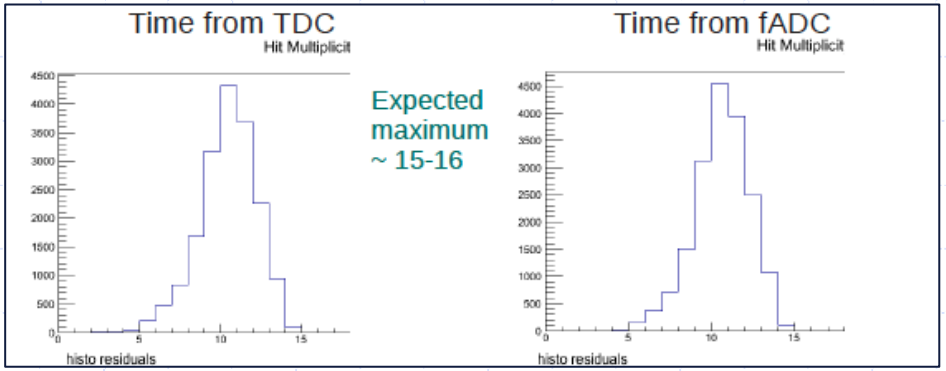
Total charge

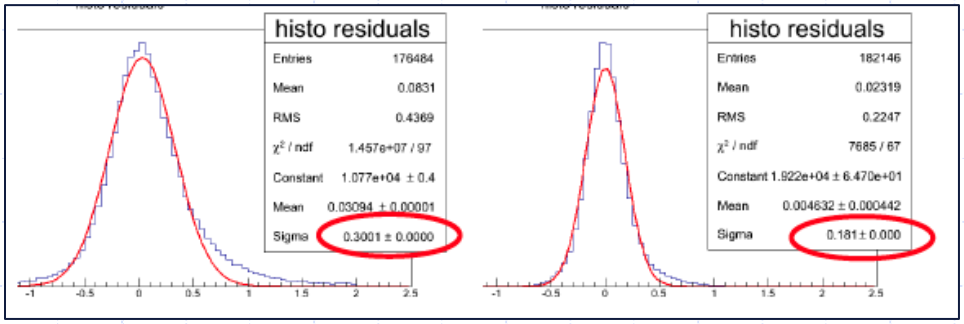
- ~ few percent resolution below 1875 V: for higher HV resolution degradation due to preamp saturation
- TOT vs charge dependence: typical shape for quasi-Gaussian pulses

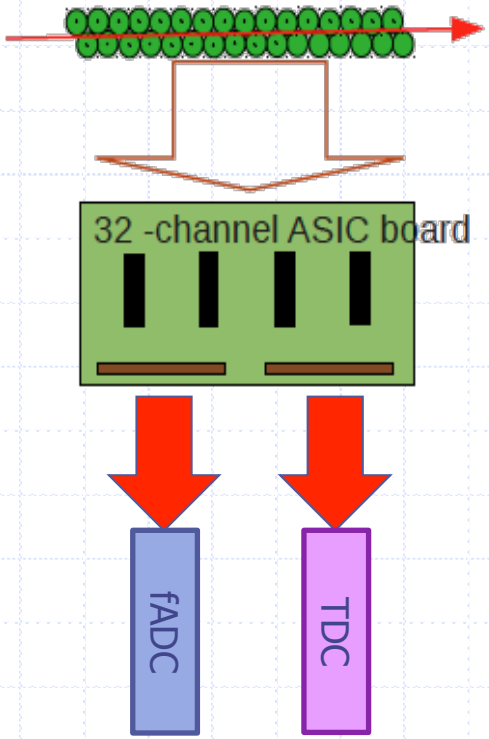
Test beam results

ASIC performance @ 900 MeV/c and 600 MeV/c
Beam intensity 100 – 500 kHz/straw
Data collected in fADC + TDC

900 MeV/c





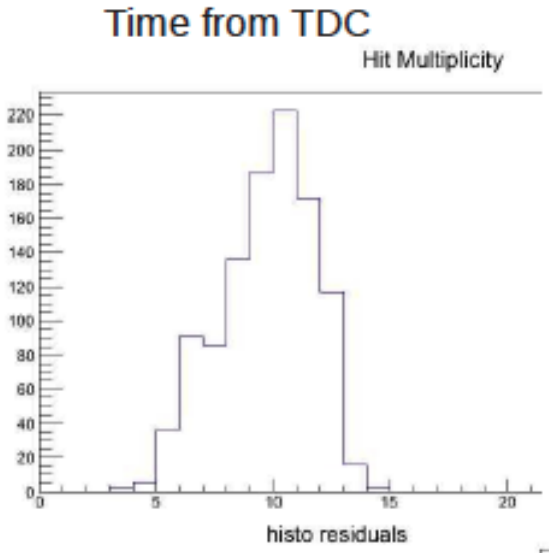


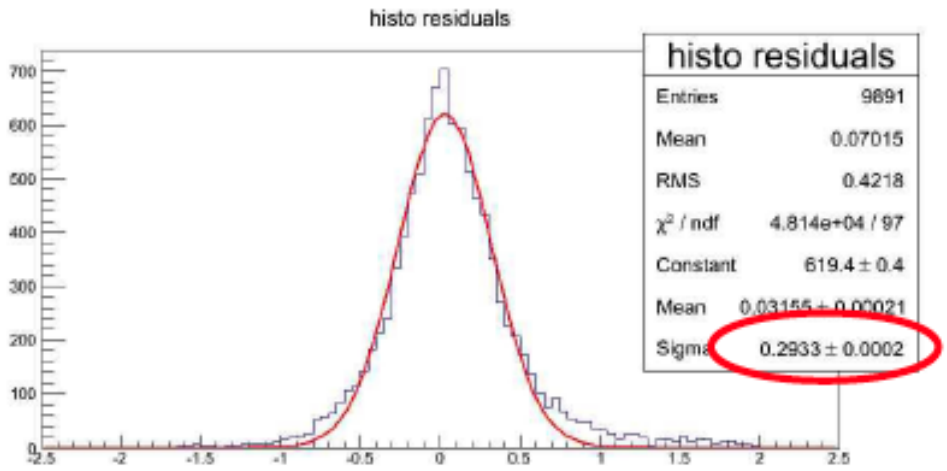
- Efficiency is a bit low. Threshold too high?
- Spatial resolution not yet at the level of discrete electronics

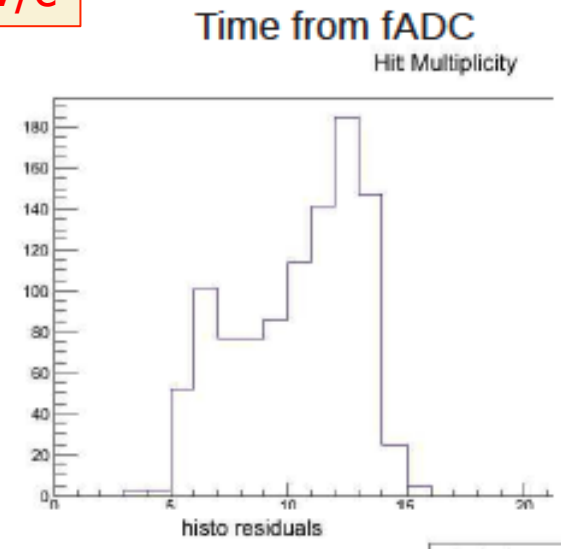
Resultst by K.Pysz

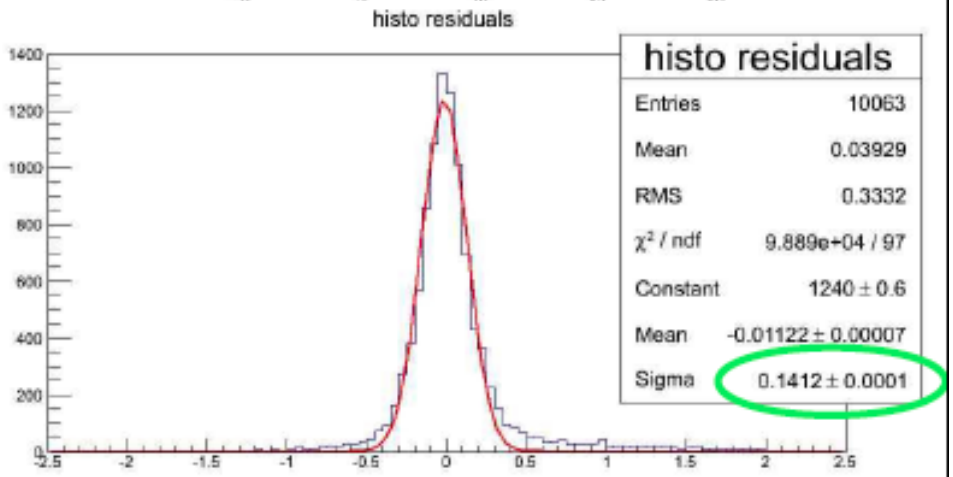
Test beam results

p_beam = 600 MeV/c



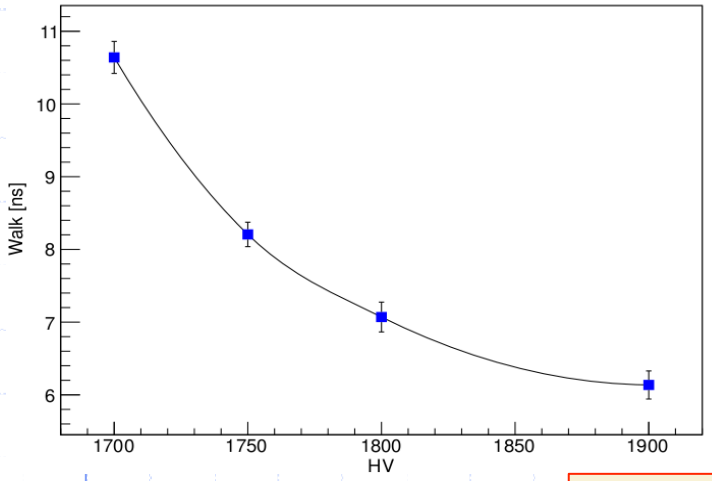


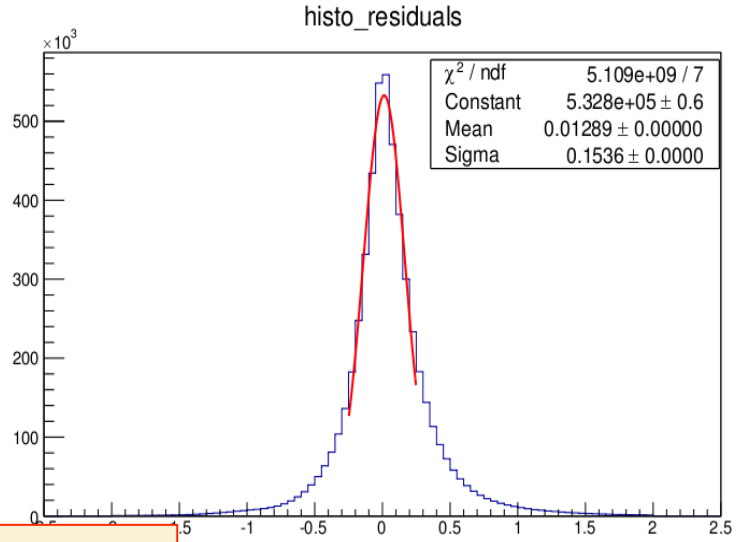




Resultst by K.Pysz

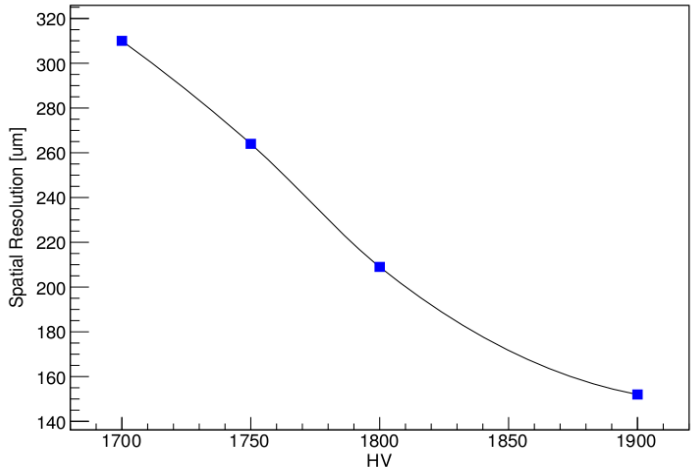
New Tracking results



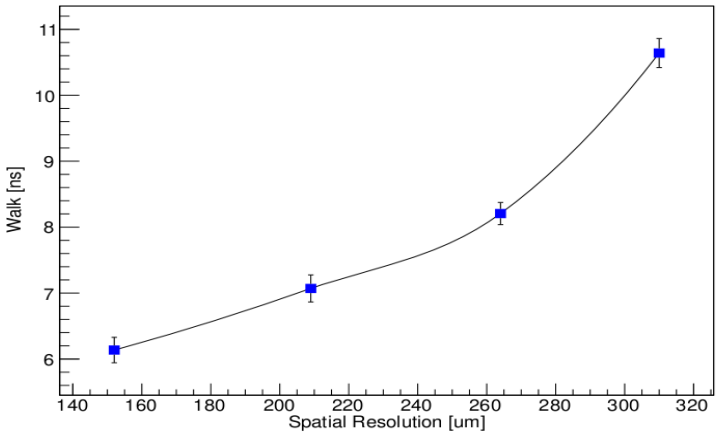


p_beam = 900 MeV/c

Spatial Resolution vs HV



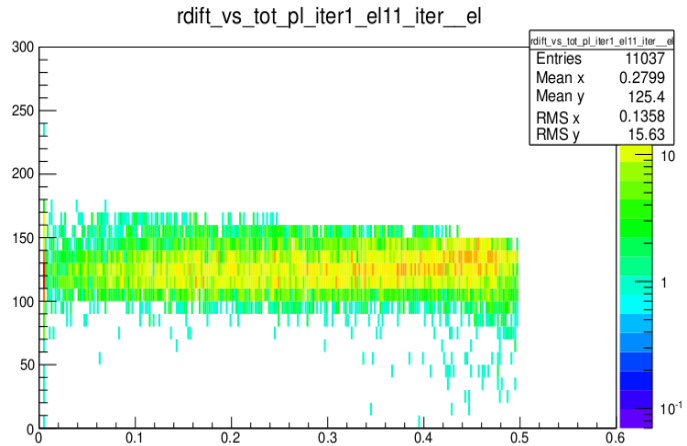
Spatial Resolution vs Walk

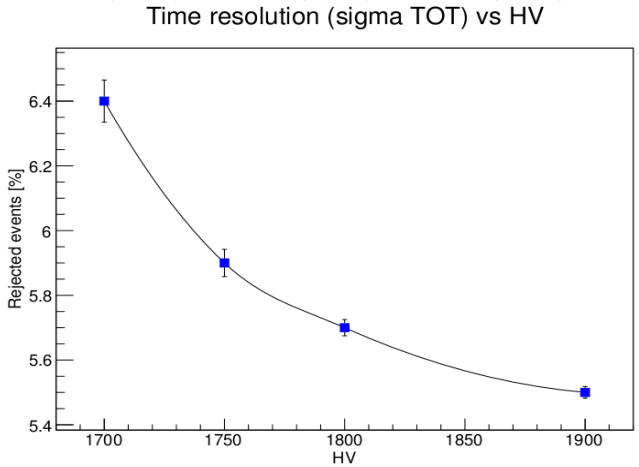


Resultst by J.Biernat

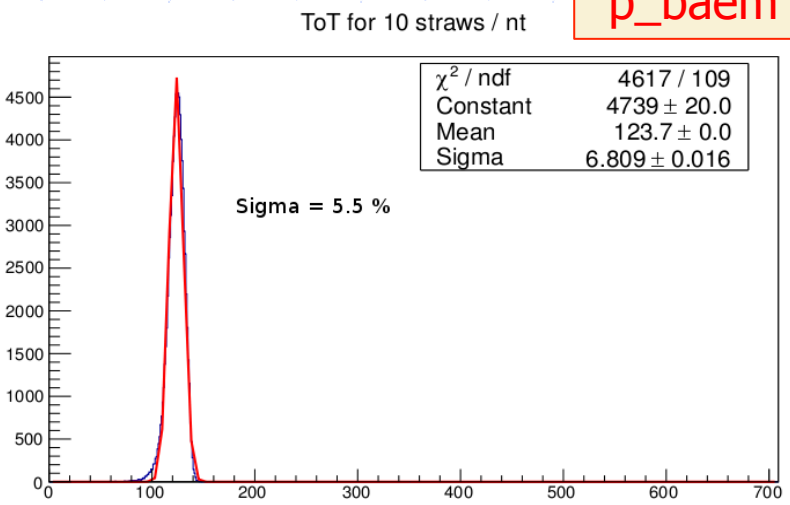
Energy measurements

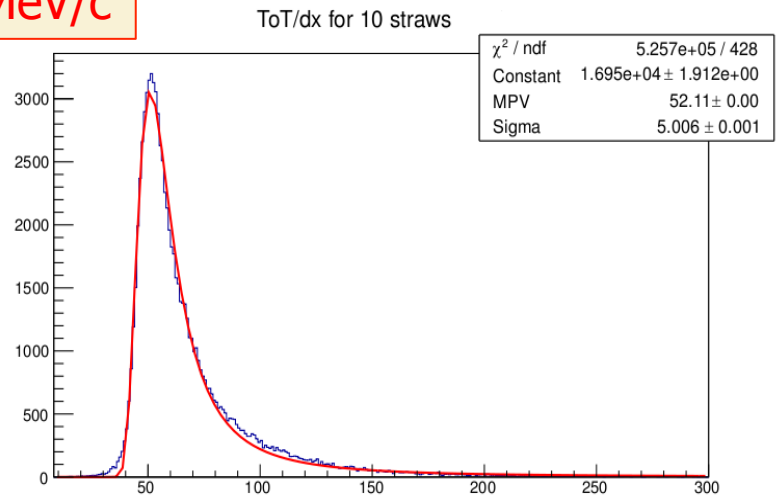
Resultst by J.Biernat





p_baem = 900 MeV/c





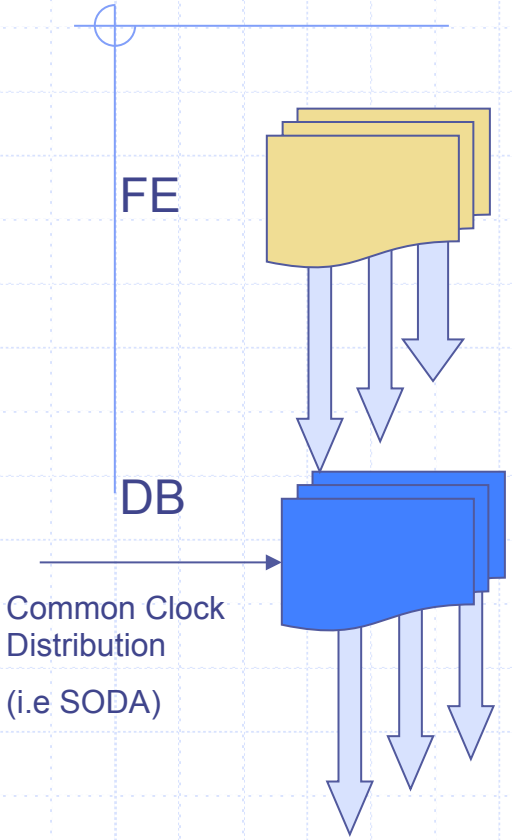
II Version of STT ASIC

The following STT ASIC parameters have been fixed:

- nr of channels: 8
- outputs: we will keep both LVDS and analog
- noise: ENC of about 1.5fC is acceptable
- gain: new values to avoid preamp. saturation. The best option corresponds to the setting "1mV/fC" in the present ASIC
- detector capacitance: 15-25 pF
- tail cancellation: we will keep the present capabilities of setting two time constants in very wide range
- uniformity of base line between channels (and therefore threshold seetings.

A new production of 100 ASICS will be realized this year. The technology will remain CMOS 350 nm.

STT readout chain



FEE anlog:

- Preamp+ Shaper+ BLR + Discriminator
  Analog output needed for dE/dx measurement

Digital Boards:

- Multihit TDC : Time measurement + TimeOverThreshold (TOT) for charge measurement OR/AND signal after shaper as input to FADC
- binning 0.5-0.8 ns
- Zero suppression & Hit detection. Slow /Run/Data flow control

Data Concentration :

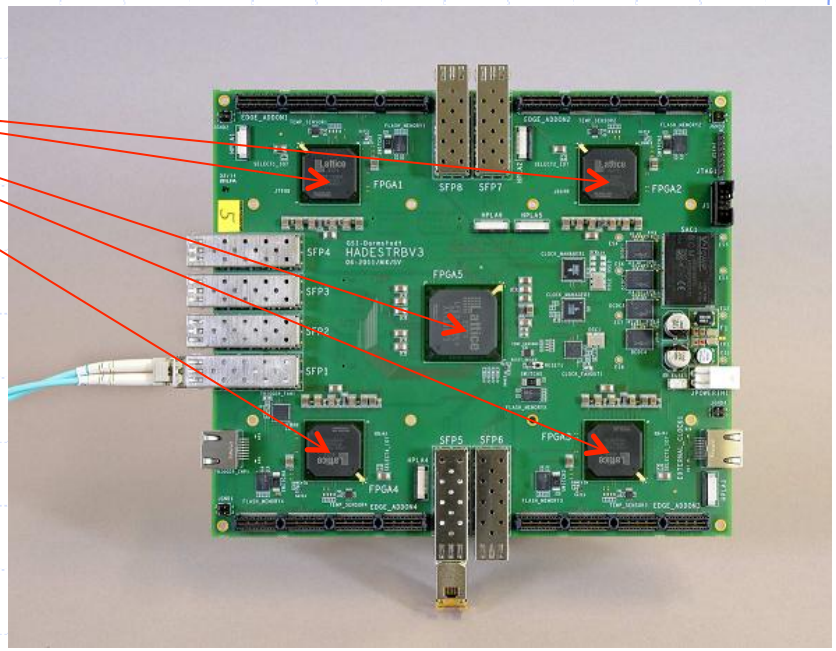
- gathering and sorting of hits marked by time stamps in epoques (i.e 500 μs bunch)
- nGbit/s Optical serial link

Trigger Readout Board

by M.Palka

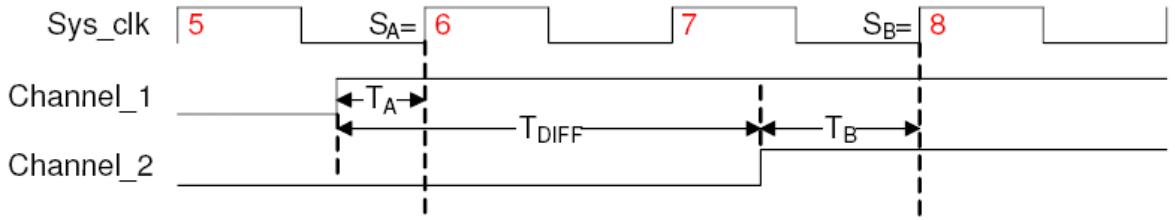
5x Lattice ECP3 150 FPGAs
- 4 edge devices up to 60 TDC ch
- 1 central for control
- Flash ROMs for each

8x 3.2GBps optical links
- 4x 208pin QMS connectors
  - ✓ Small Addons
- 2x80pin connectors
  - ✓ Large Addon (i.e. ADC)

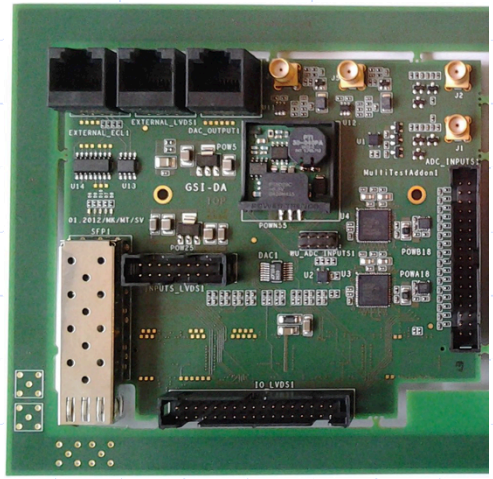


12 TRBs will instrument 1 STT chamber

FPGA TDC basic concept



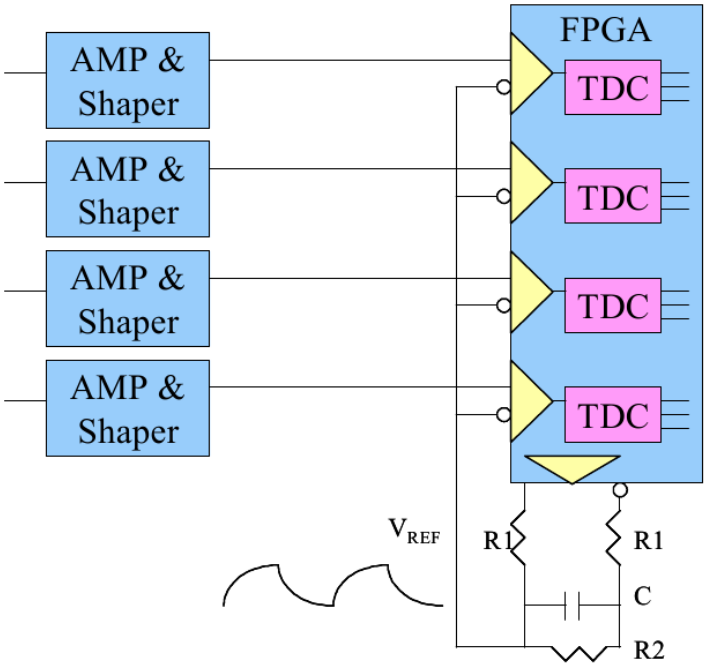
Dedicated Addon



by M.Palka

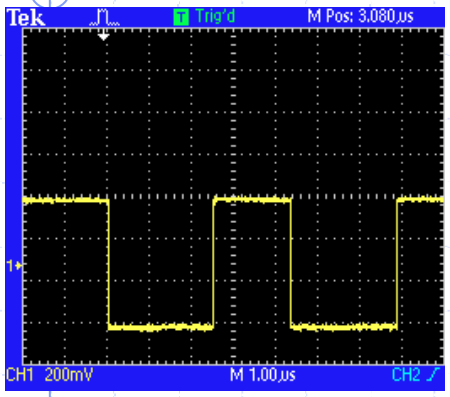
Multi-Test AddOn has been built to test new concepts of:
- Q2W + FPGA (2 different concepts)
- ADC + FPGA
- "standard" 100 MHz ADC
- additional optical connection

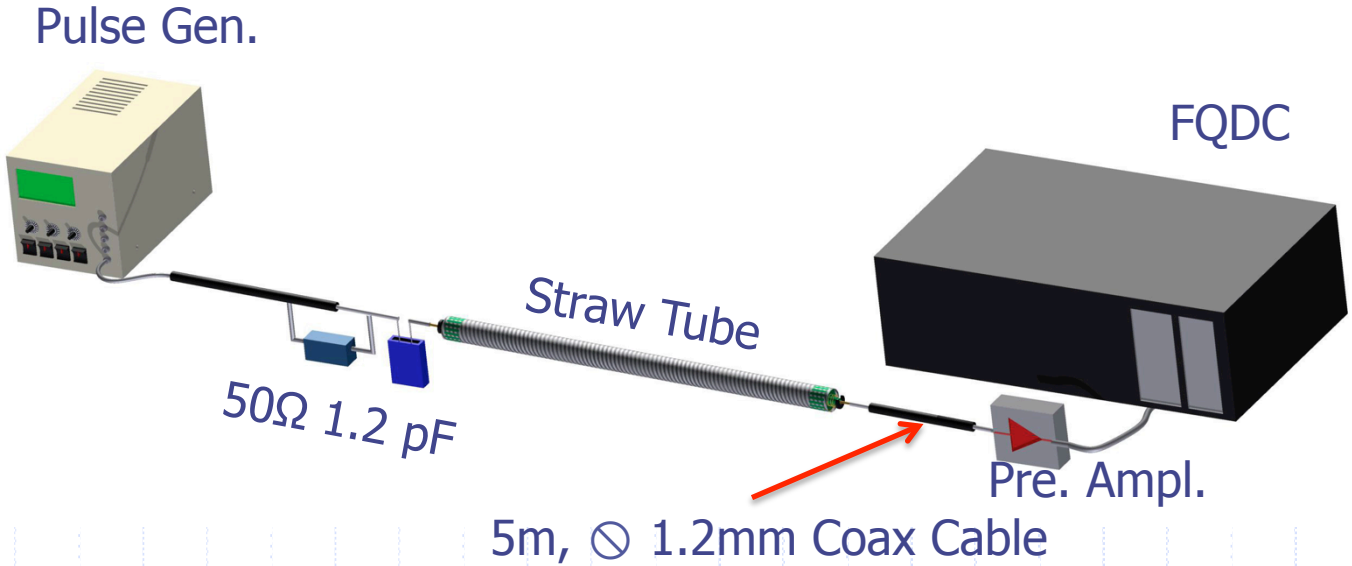
Scheme of FPGA ADC functionality implementation

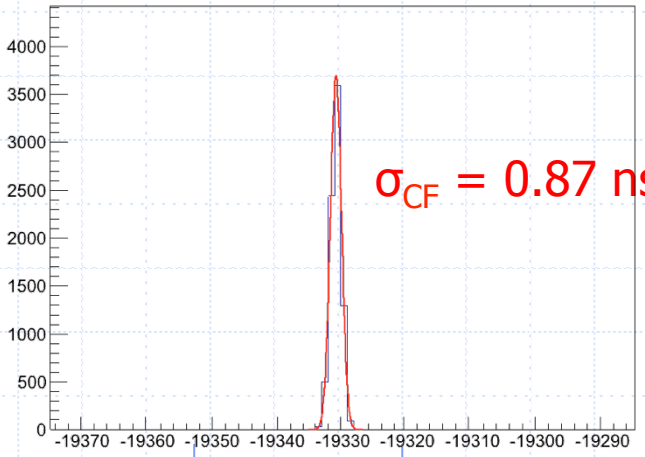


An alternative approach

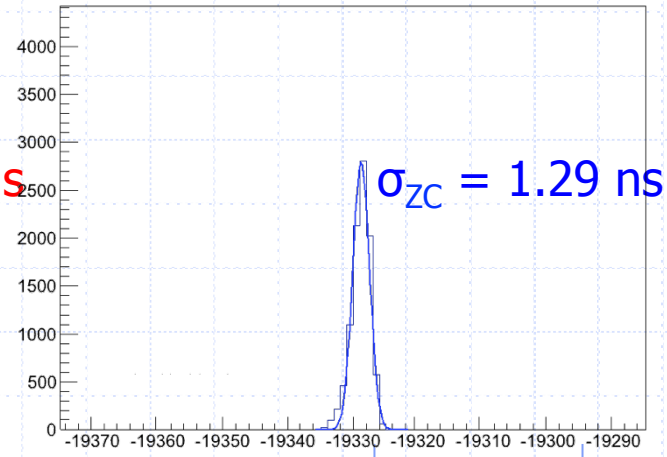
Measurement done by T. Preuhs







σ_{CF} = 0.87 ns



σ_{ZC} = 1.29 ns

Conclusions

1. The right parameters for measuring simultaneously and precisely time and energy are under definition.
2. Integration of STT output signals over 40 - 60 ns assures required spatial resolution as well as demanded energy resolution for PID.
3. The results of the tests of the new FEE are consistent with those obtained earlier with discrete component electronics.
4. Energy measurement improvement by means of Time over Threshold (ASIC) is still on-going.
5. Trigger Readout Board v3 is suitable for STT signals allowing both Time and Amplitude measurements.
6. Alternative options for the FEE are still under investigation.