A 64-Channel ASIC for TOFPET Applications

Manuel D Rolo, Ricardo Bugalho, Carlos Gastón, Gianni Mazza, Angelo Rivetti, Richard Wheadon, Jose Carlos da Silva, Rui Silva, Joao Varela

LIP - Laboratorio de Instrumentacao e Fisica Experimental de Particulas
INFN - Istituto Nazionale di Fisica Nucleare sez. Torino

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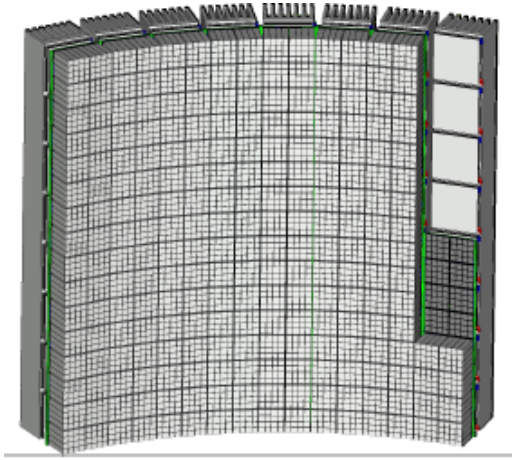
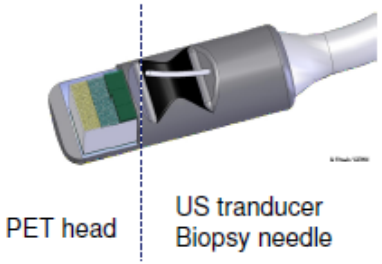
Readout IC for Time-of-Flight PET

Framework: **EndoTOFPET-US project** (JNM NSS/MIC 2012 Joint Session talk JNM-2): Development of a novel multimodal tool for the test of new biomarkers for pancreatic and prostate tumors



External PET plate

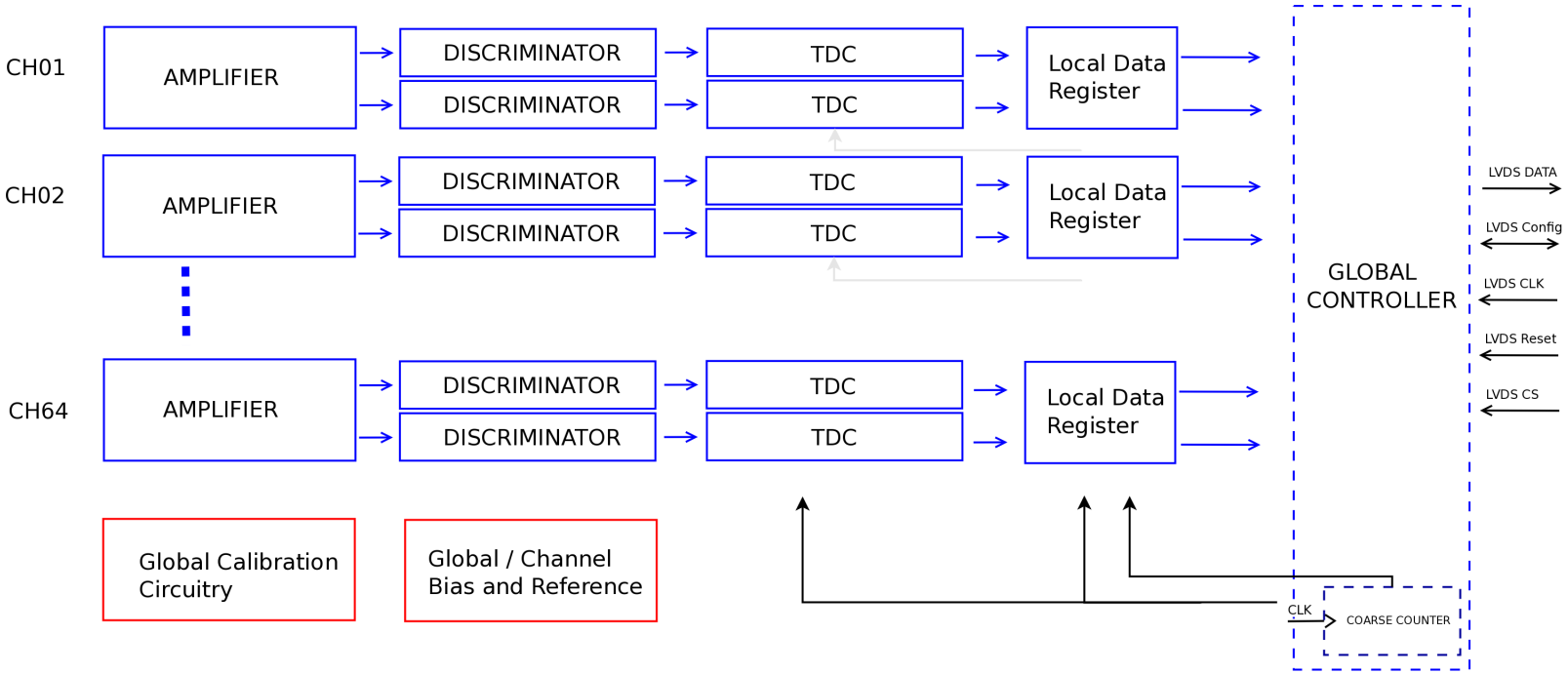


Endoscopic probe

- Combined **TOF-PET (200 ps time resolution)**, ultrasound imaging and endoscopic biopsy
- Extraction of TOF information: Need to trigger the time-of-arrival of the first photoelectron(s) to reduce the effect of the scintillation light statistics
- Readout chain of the external PET plate is based on LYSO crystals and SiPMs - **customized readout ASICs developed**

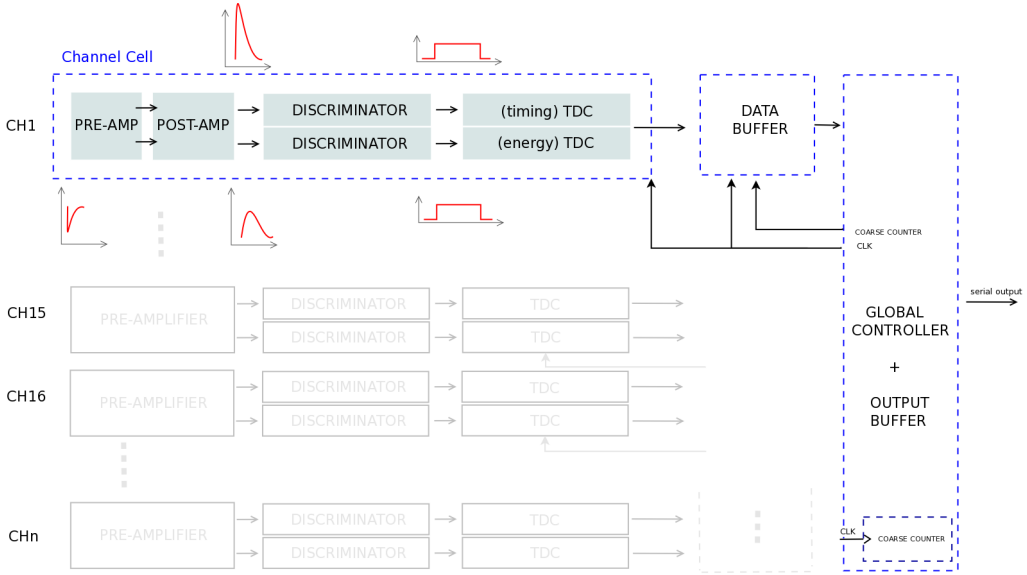
Overview of the chip architecture

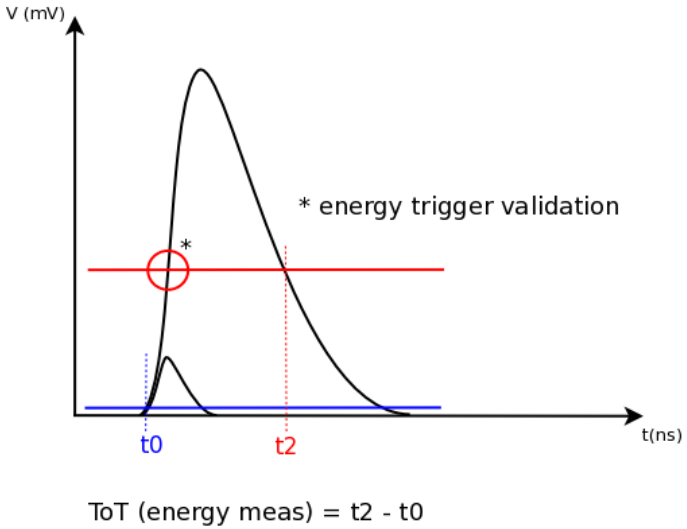
The TOFPET ASIC consists of a 64-channel analogue block, calibration circuitry, Golden-reference and Bias generators and a global controller.



- LVDS 10 MHz SPI configuration link for bias/channel setting
- LVDS 160-640 Mbps data output interface
- On-chip DACs and reference generators

Overview of the channel architecture

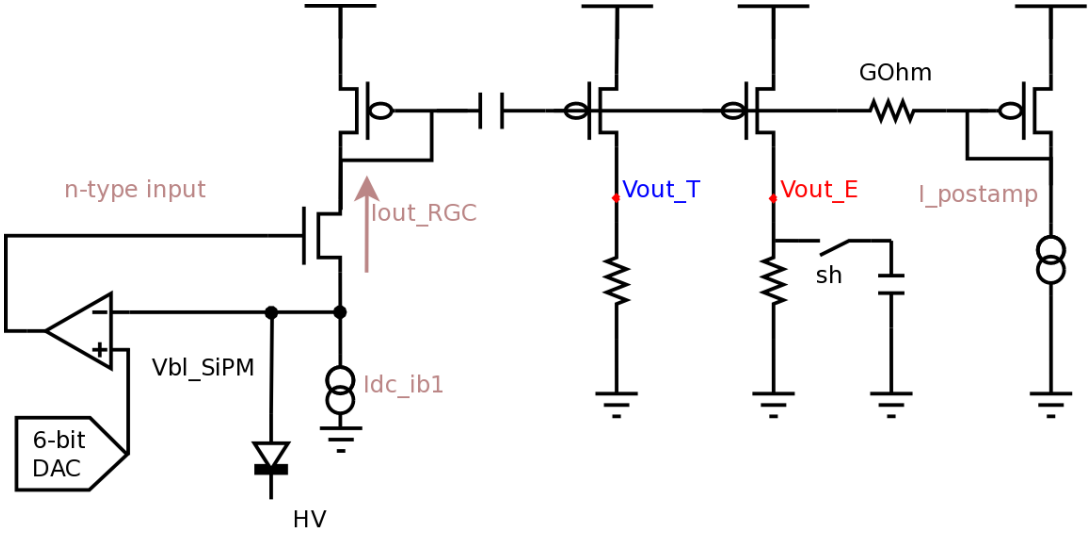


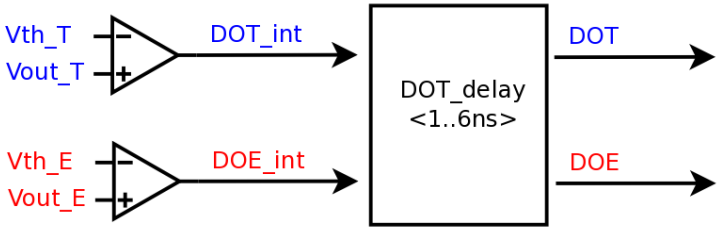


- Time and charge measurements with independent TDCs
- TDC time binning 50 ps
- Charge measured with Time-over-threshold
- Typ. power consumption is 7mW p/channel (**trigger 0.5 p.e.** w/ $SNR > 23dB$ for 9 mm^2 MPPC, 40 KHz event rate, 1MHz DCR)

Front-End

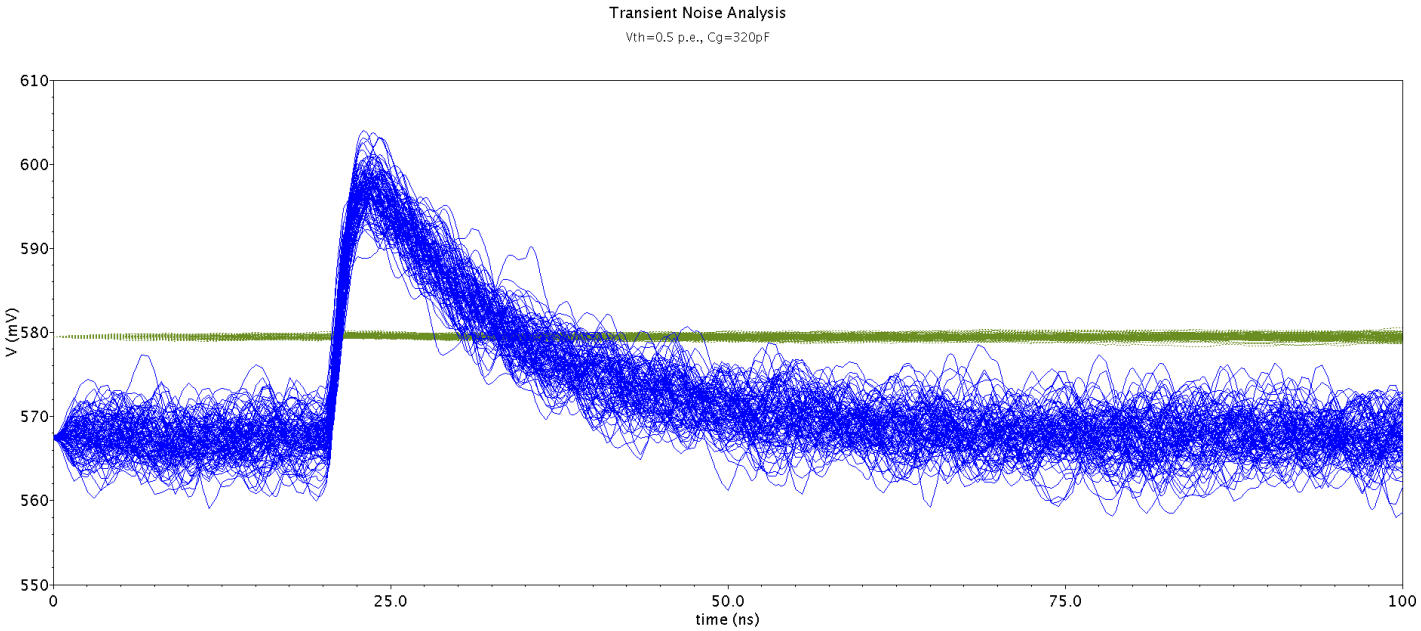
- Low-Zin pre-amplifier, 2 independent TIA branches for Timing and Energy triggers
- Fine adjustment of the HV bias (6-bit over 500mV range) of the SiPM
- Selectable shaping function for Vout_E to avoid re-triggering and correct eventual loss of ToT vs. Qin monotonicity
- Selectable delay line for dark count filtering
- Usable for p-type or n-type (hole, electron collection) devices





Front-end: Figures of merit

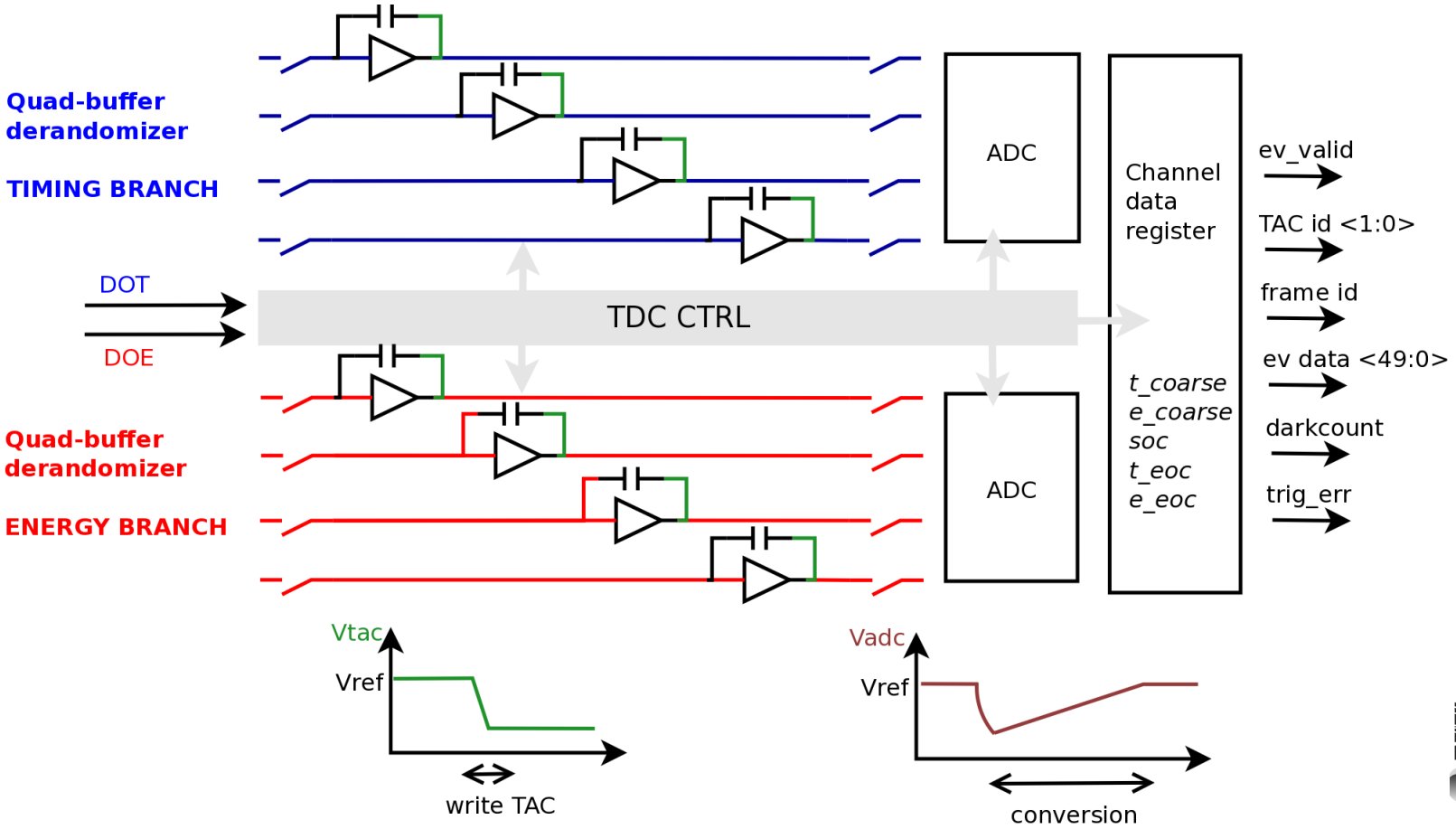
- Zin trimming for line impedance and BW adjustment is independent of SiPM DC bias thanks to closed-loop input stage
- FE contribution to total jitter is less than 25 ps FWHM
- Trigger level can be set down to 0.5 p.e. with SNR above 23 dB (C_g = 320pF - 9mm^2 MPPC)



TDC

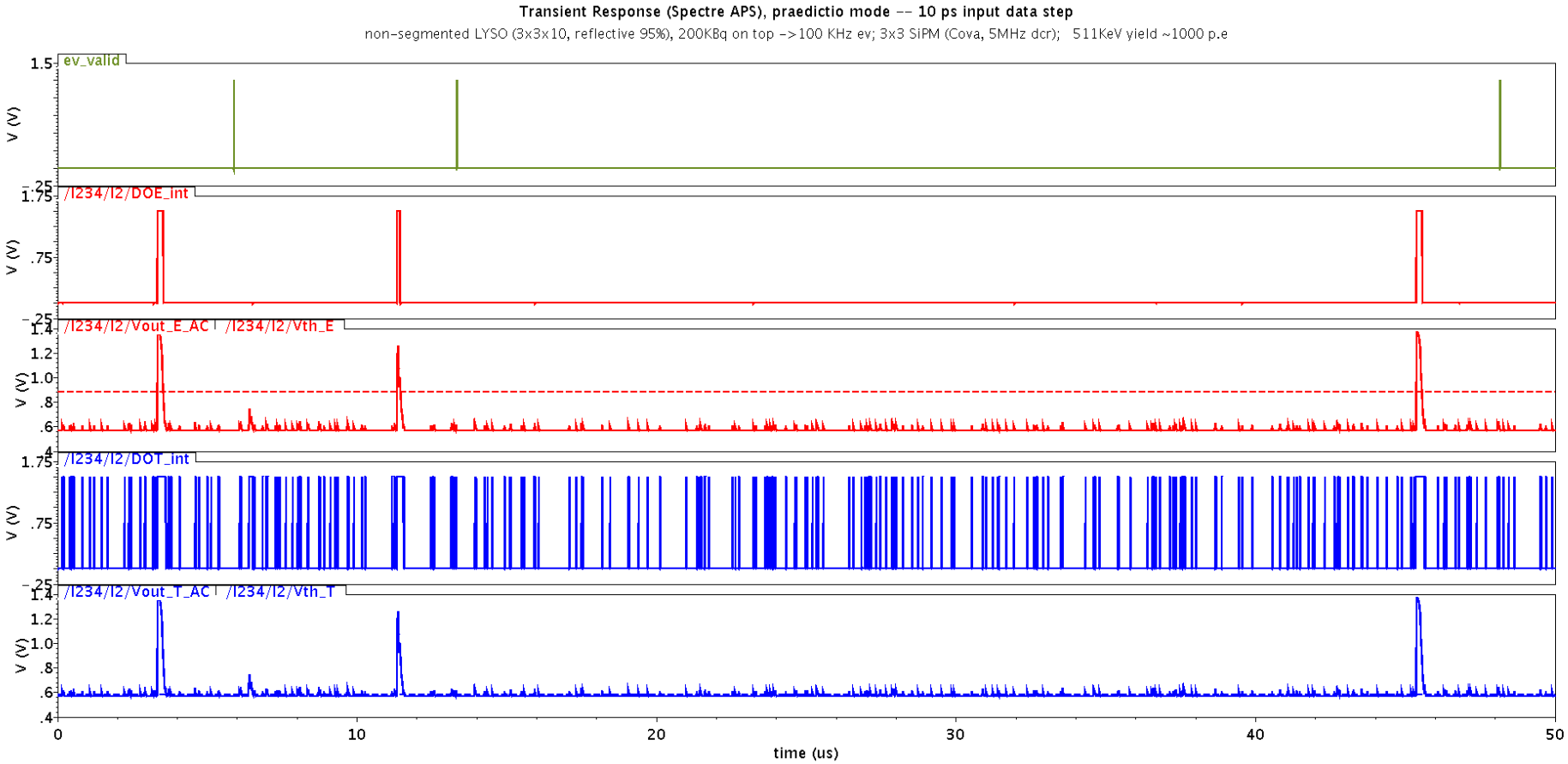
Analogue TDC with 50 ps time binning - based on Time-to-Amplitude Conversion [Stevens89, Rivetti09]

- TDC Control: switching, hit validation, buffer allocation, data reg.
- Time stamp: 10-bit master clock count + Fine time measurement



Geant generated SiPM+LYSO data

Simulation of the whole channel (TDC CTRL simulated at transistor level); input is a test vector with data generated from Geant routines



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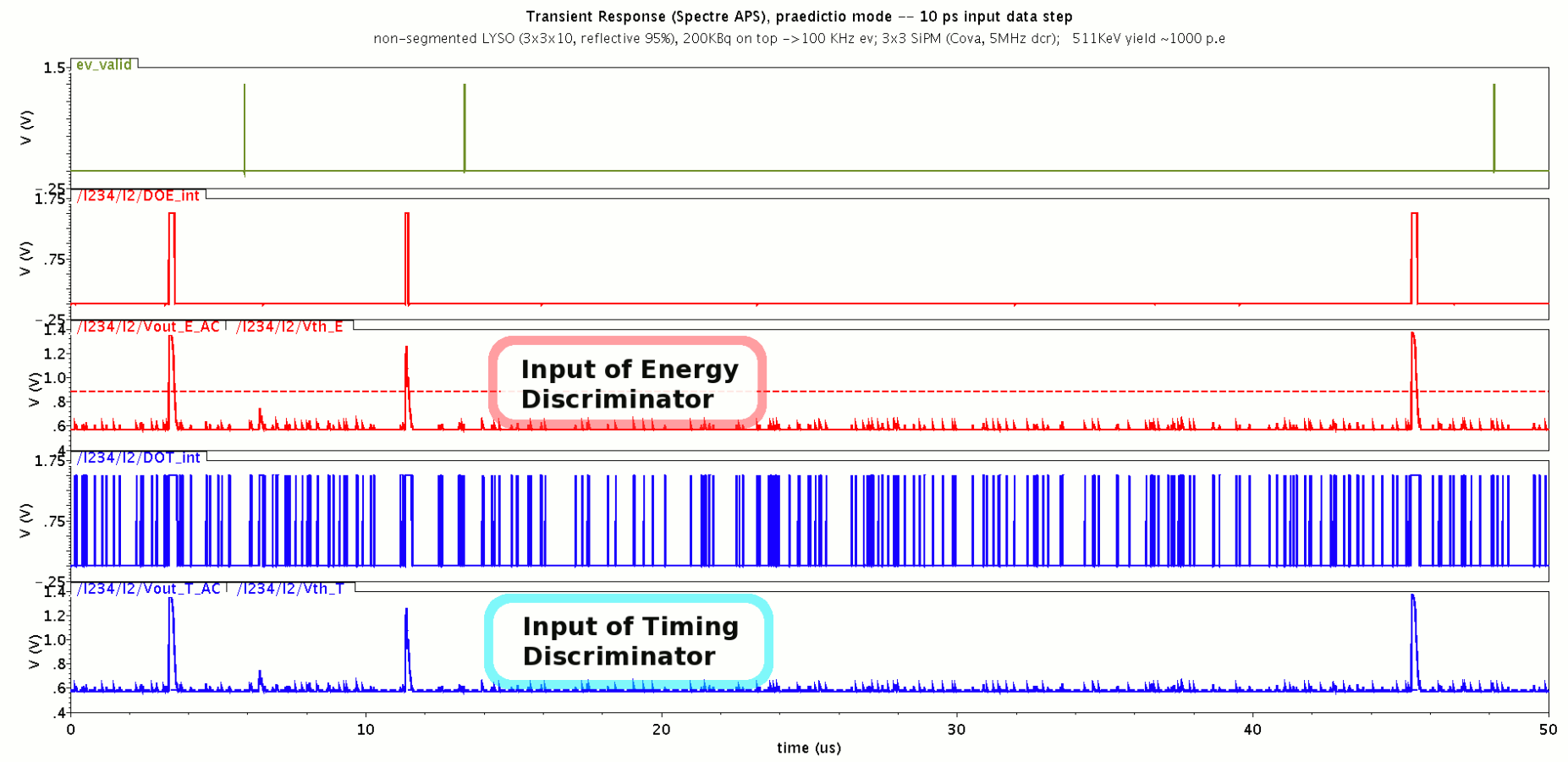

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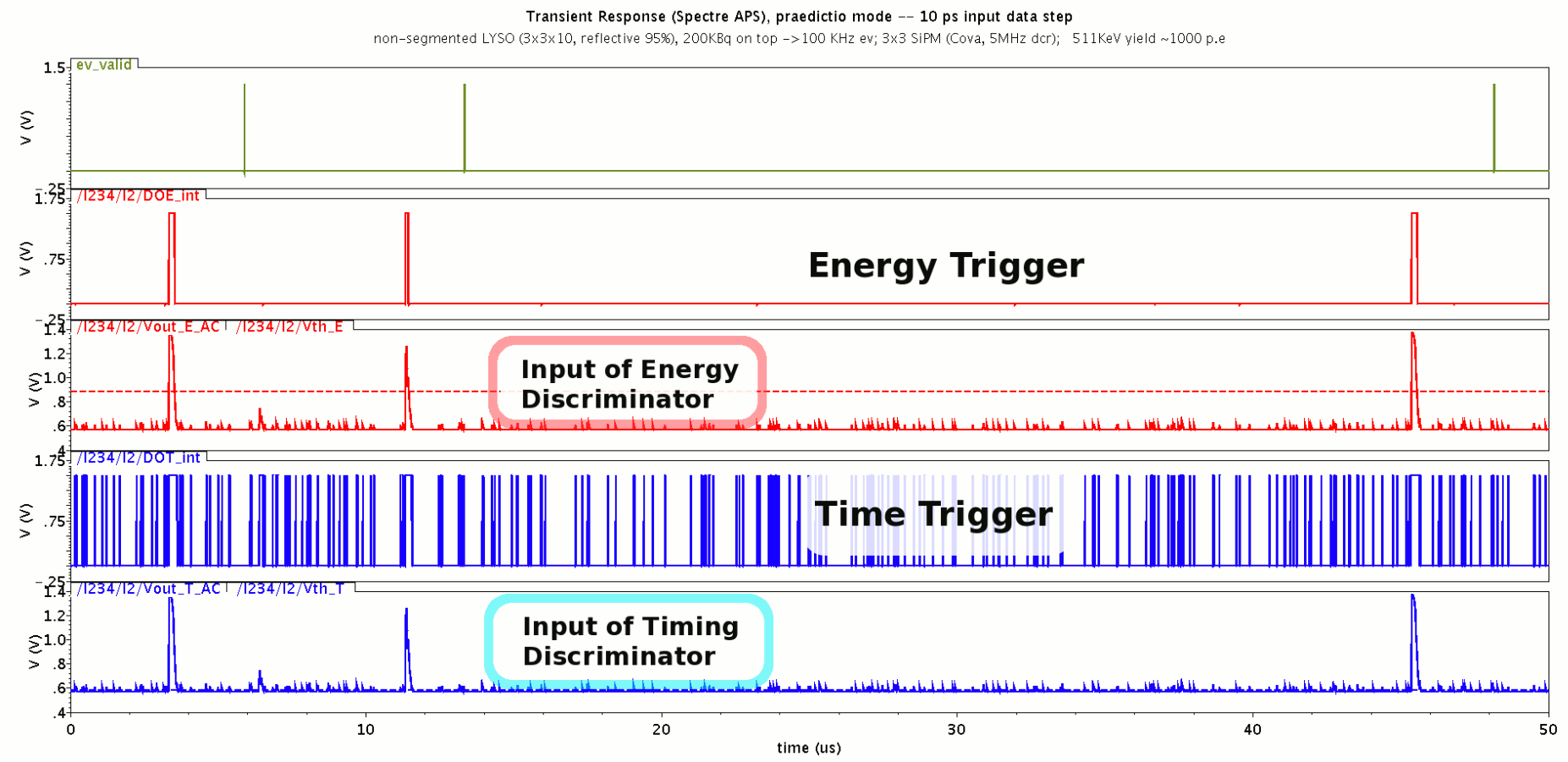

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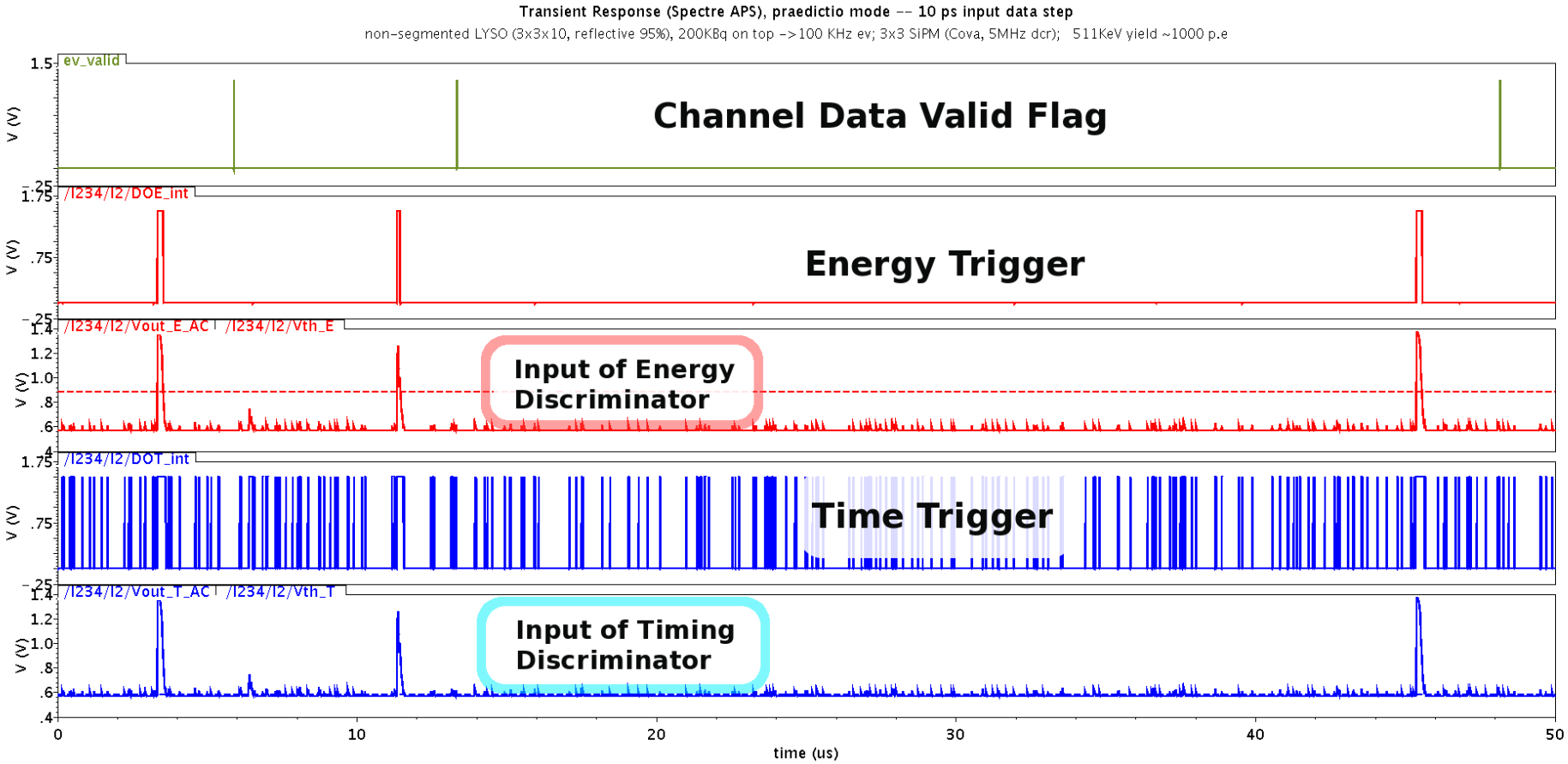
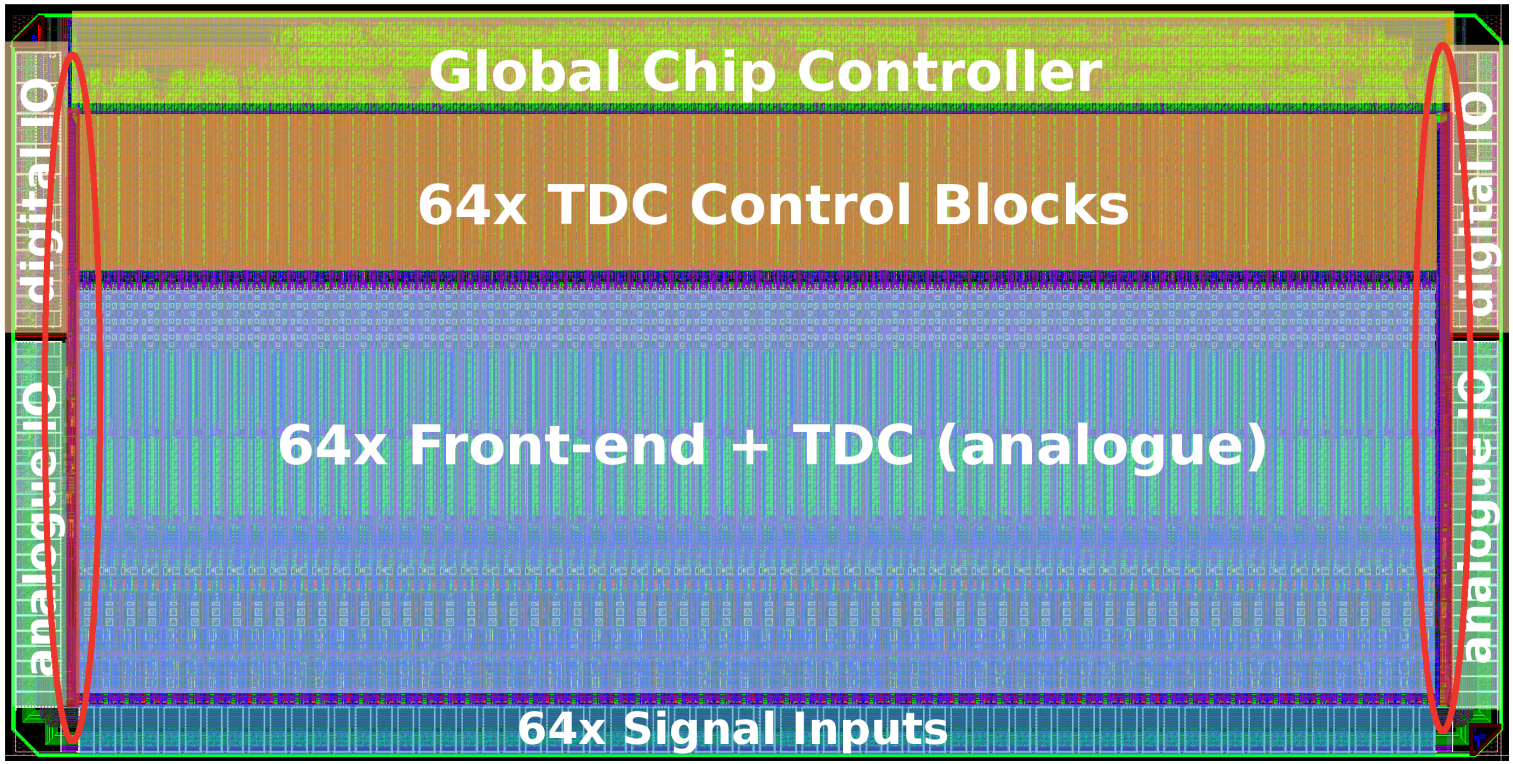


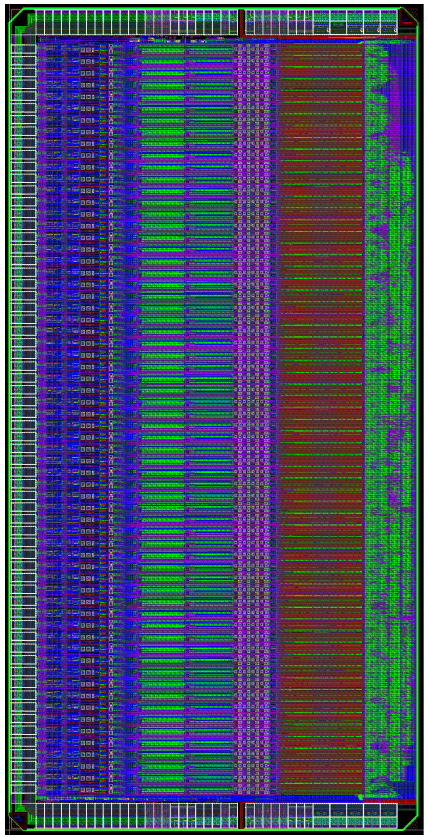
Floorplan of the 64-channel mixed-mode chip

- CMOS 130nm $25mm^2$ 64-channel ASIC
- Highlight shows the allocated area for bias and calibration circuitry.
- One pad-free edge to allow abutting two twin chips into a 128-channel BGA package.



Packaging of a 128-channel SiP

- The TOFPET ASIC has one pad-free edge
- That allows a second (rotated) chip to be abutted
- The compact 7x7 mm SiP can be packaged into a BGA



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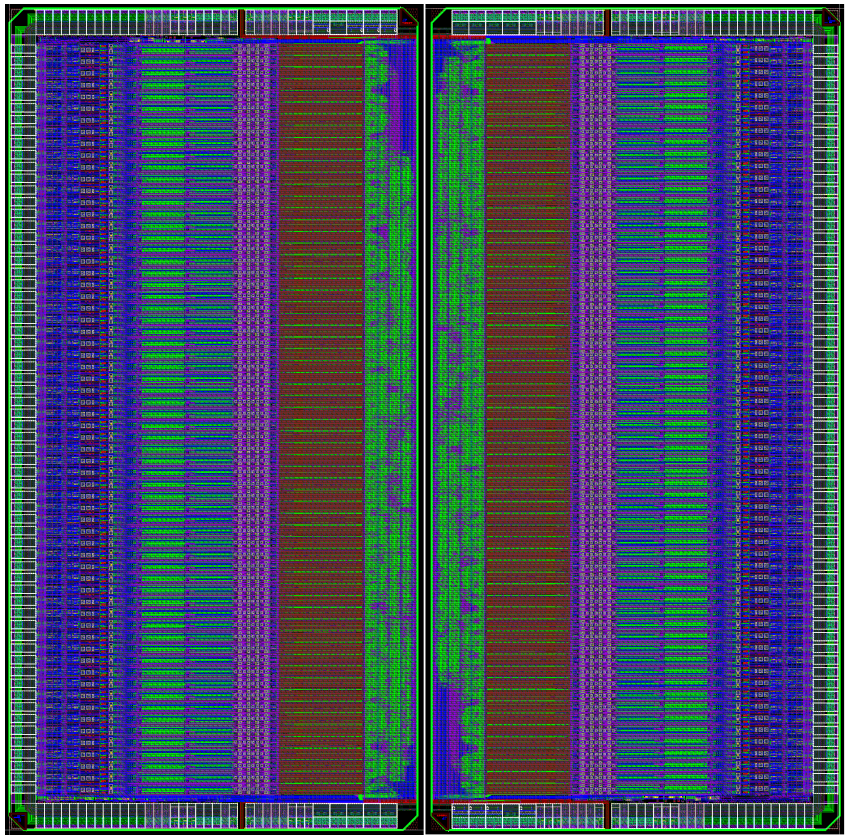

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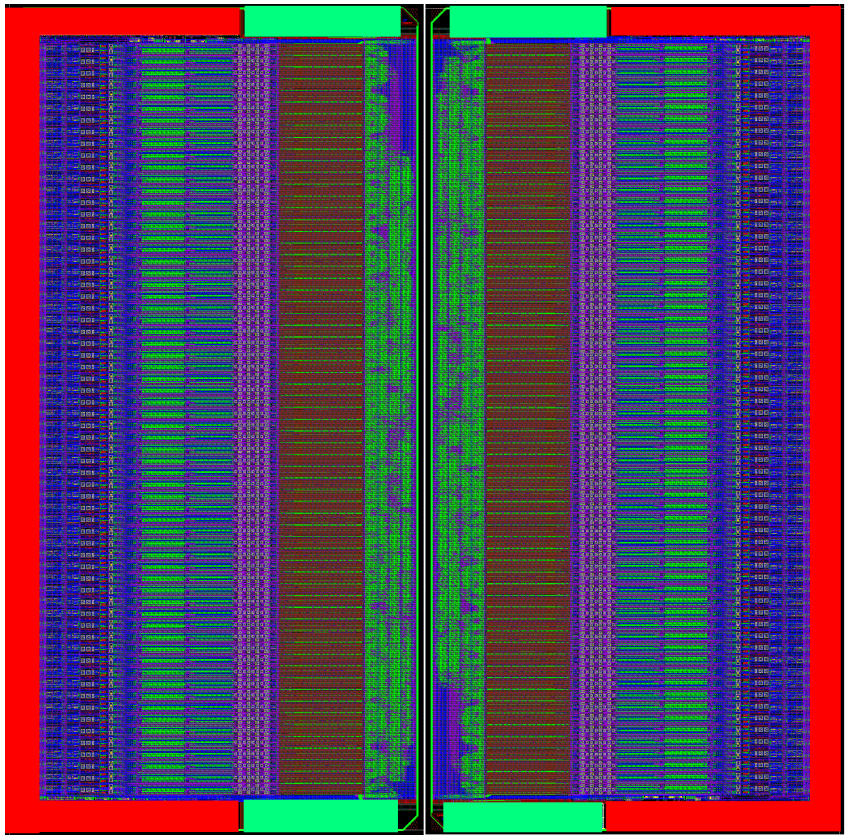
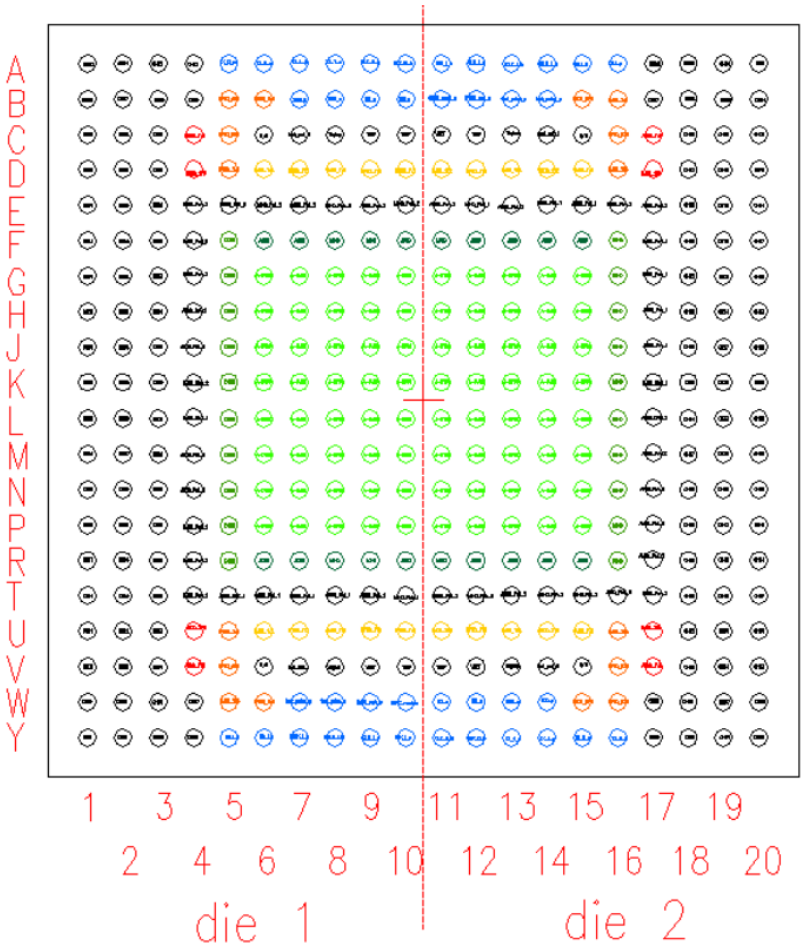
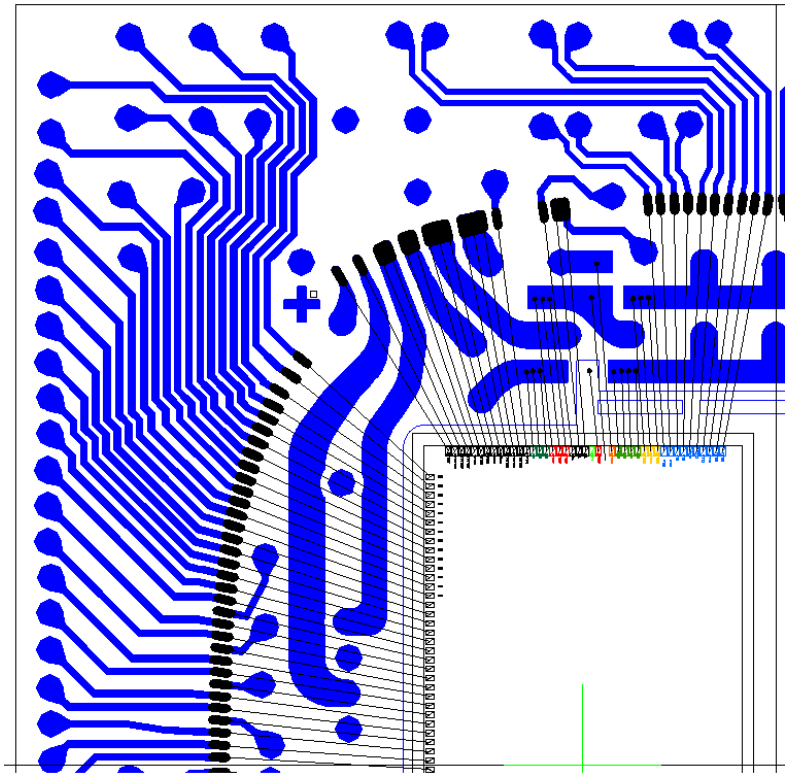


BGA package for the 128-channel assembly

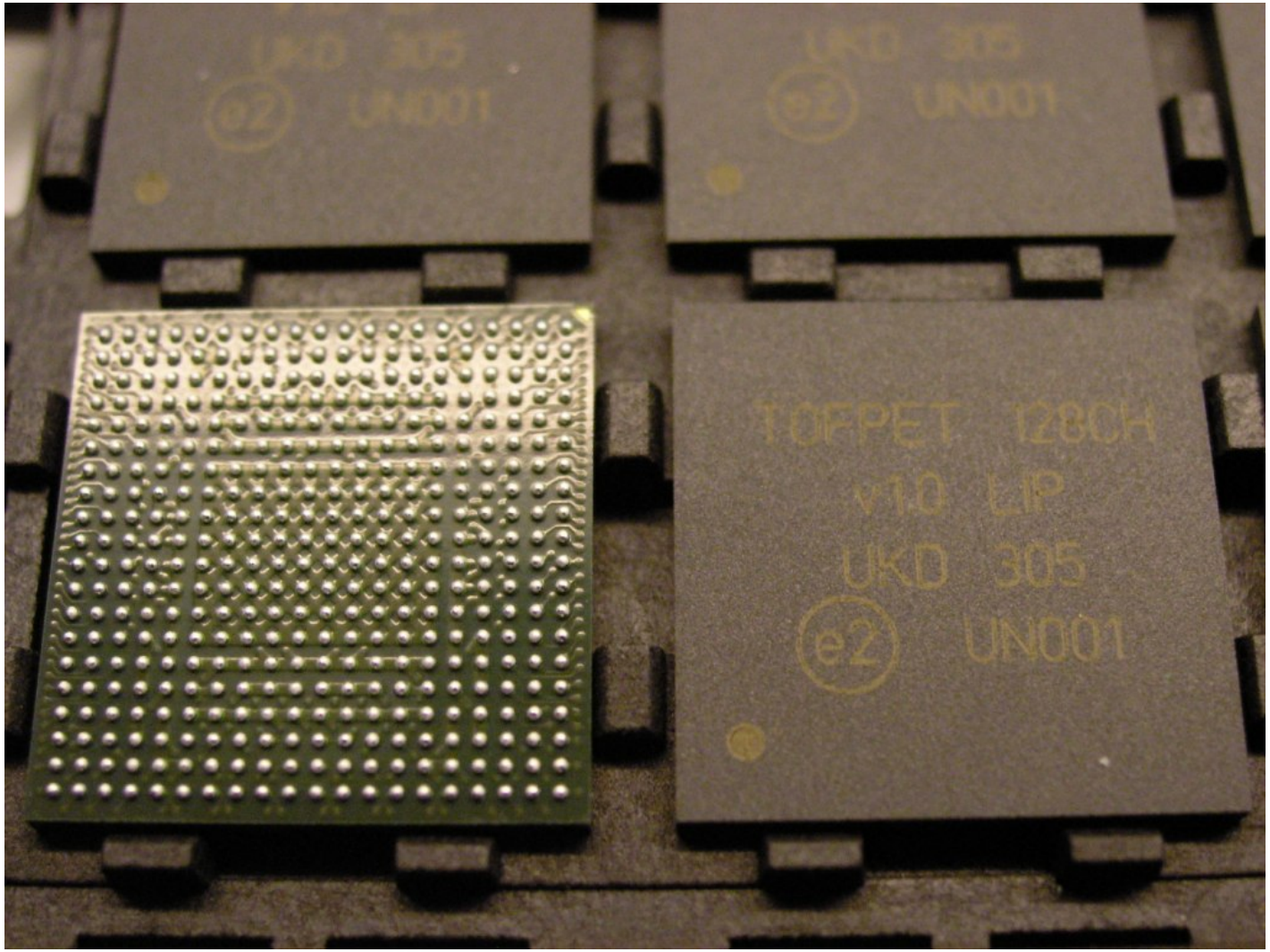
View of the BGA ballout (17x17x1.70 mm 4 Layers PBGA 400) for the 128-channel assembly (left) and corner detail of the package substrate (right):





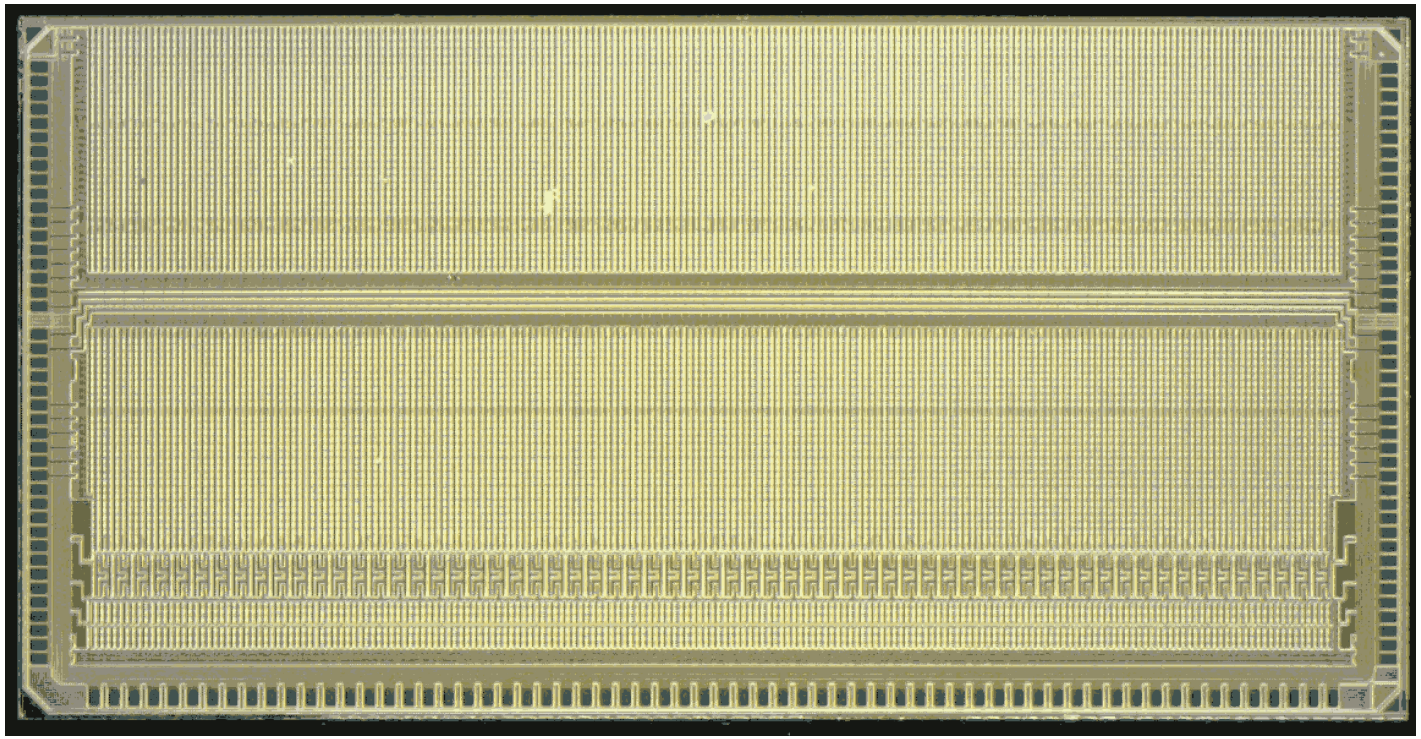
Test Setup @Lisbon (PT)

- Test setup for 128-channel SiP - Characterization ongoing

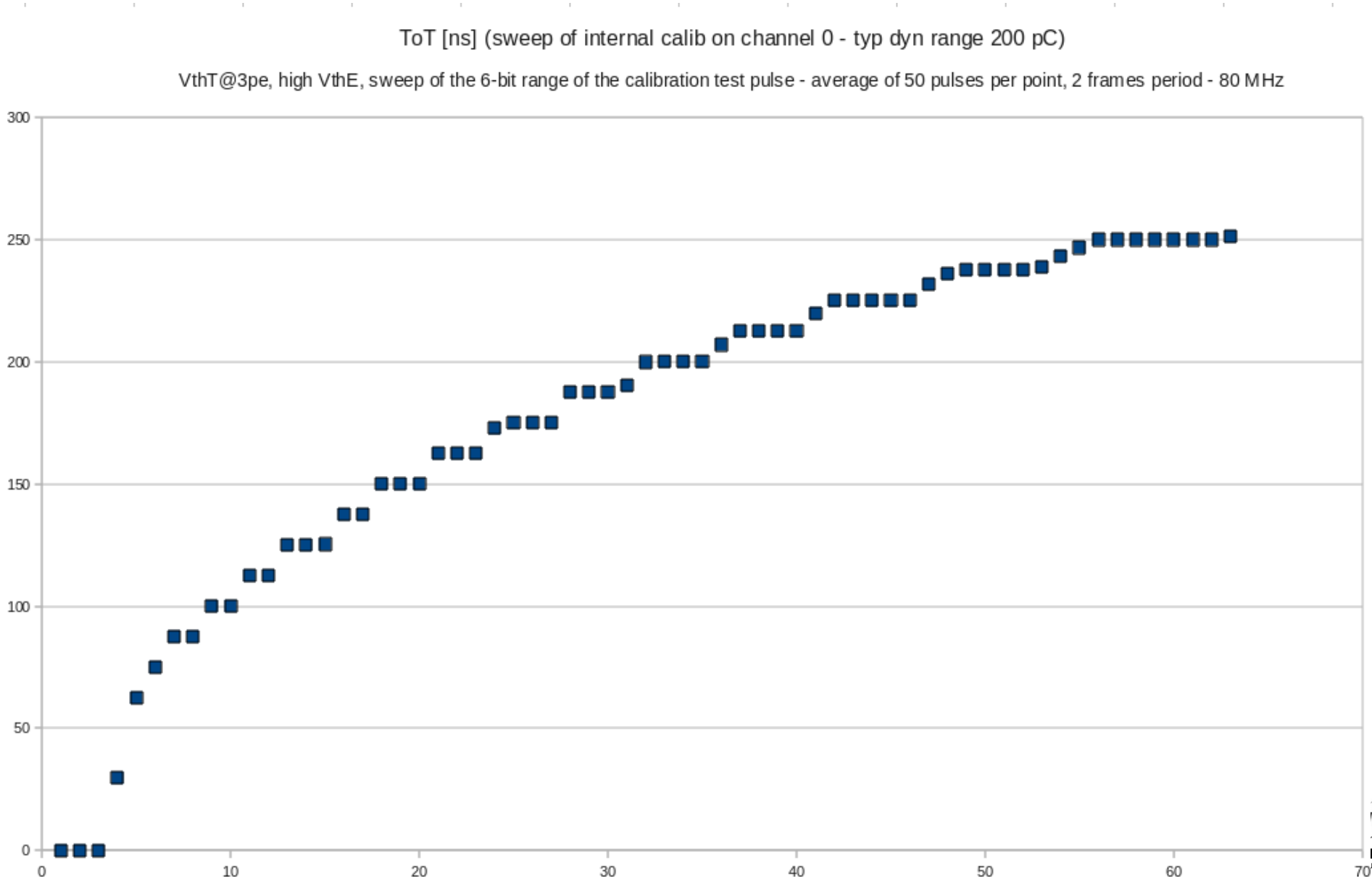


Test Setup @Turin (IT)

- Test setup for 64-channel board bonded chip - Characterization ongoing



Preliminary Results - ToT (internal calibration)

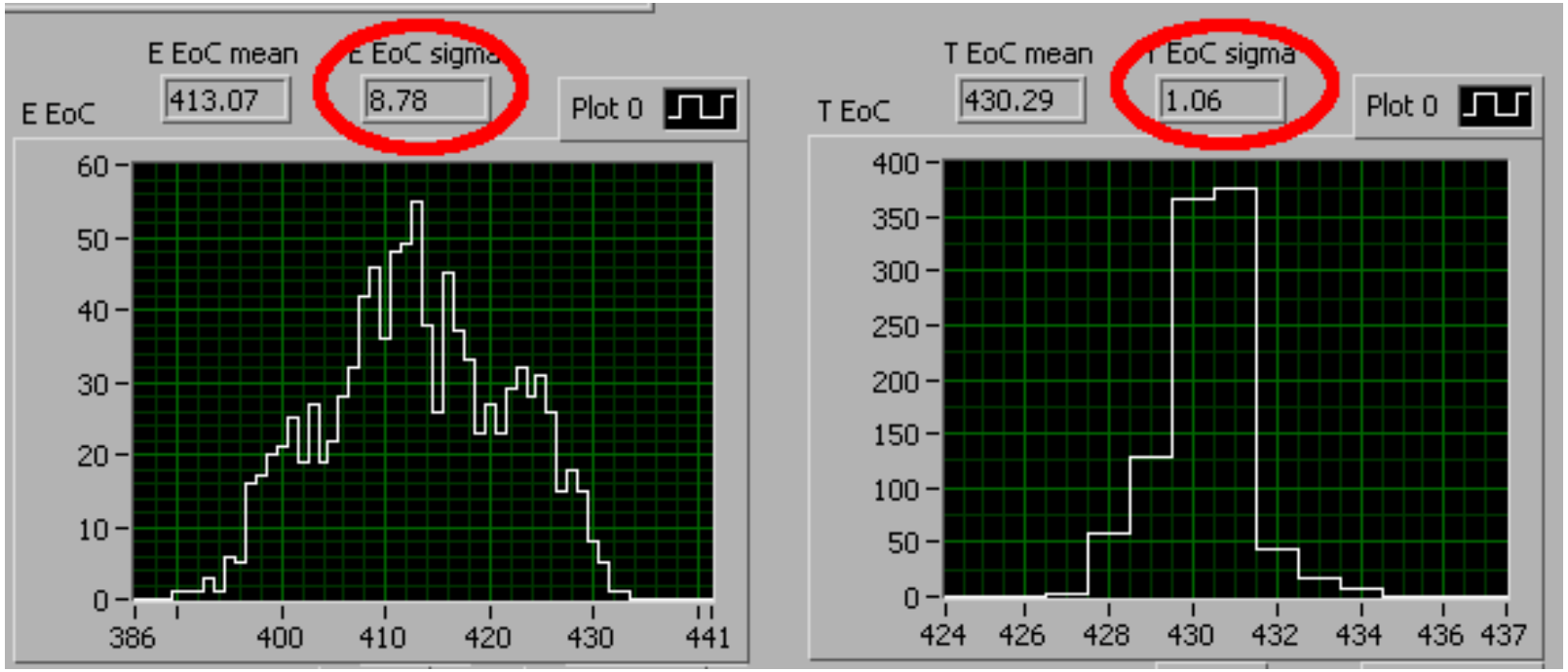


Preliminary Results - TDC sampling noise

- Jitter (FPGA external test pulse) + TDC digitization noise < 1 LSB

Preliminary Results - Front End Jitter

- Jitter (FPGA external test pulse) + TDC digitization noise + + **FE jitter** $\sigma \approx 50\ ps$



Summary and Outlook

- Low power (7mW p/channel), low noise readout IC for SiPMs
- 64-channel ASIC tape-out July 2012, internal CERN Engineering Run
- 112 chips p/ wafer, 4 wafers ready
- Compact 17x17 mm 128-channel BGA package
- Characterization started February 2013, test benches at TagusLIP (Lisbon, PT) and INFN (Turin, IT)

Thank you!

References

[Stevens89] Andrew E. Stevens, Richard P. Van Berg, Jan Van Der Spiegel and Hugh H. Williams
A Time-to-Voltage Converter and Analog Memory for Colliding Beam Detectors
IEEE JSSC vol 24, no 6, 1989

[Rivetti09] A. Rivetti et al.
Experimental Results from a Pixel Front-End for the NA62 Experiment with on Pixel Constant Fraction Discriminator and 100 ps Time to Digital Converter
NSS MIC Conf. Records 2009

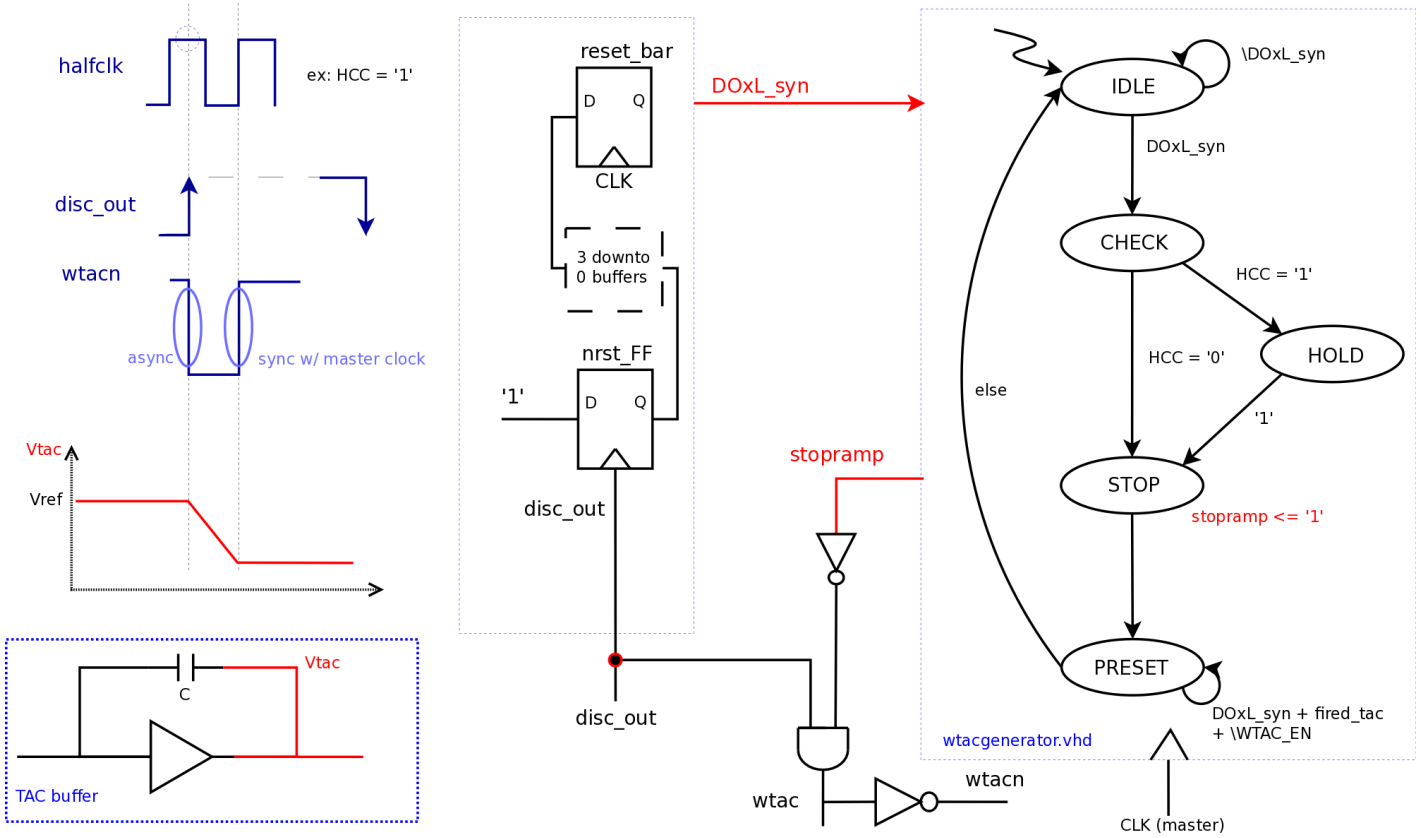
backup slides

Other features of the TOFPET ASIC:

- Data transmission w/ TX training or CLK_out;
- Synchronous/Async. test for the TDC - internal (GCTRL) or external test pulse;
- Monitoring of front-end discriminator output: time, energy, before/after delay line (jitter assessment);
- Usable for p-type or n-type (hole, electron collection) devices;
- Usable with higher light yield crystals (trimmable coarse gain);
- Zin trimming for line impedance adjustment (independent of SiPM DC bias thanks to closed-loop input stage);
- Channel masking for noisy channels;
- Dark-count rate (DCR) and DC+event overlapping measurements;
- Safe-mode power-on

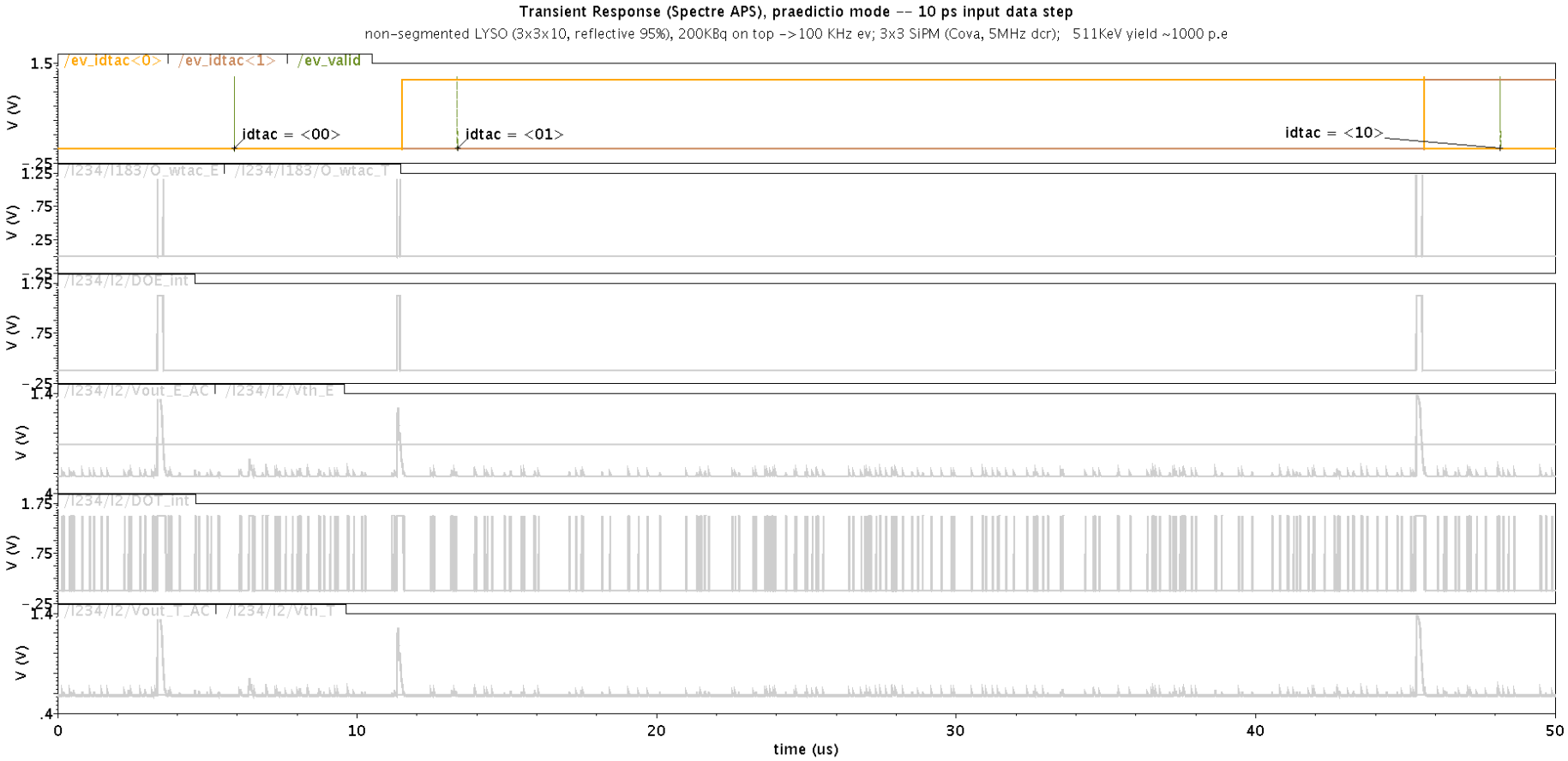
TDC - Time Interpolator

- Phase between trigger and clock edge saved as charge and converted to time domain with a Wilkinson ADC. [Stevens89, Rivetti09]
- 128x time multiplication yields a 50 ps time bin @160 MHz



Geant generated SiPM+LYSO data - TAC ID

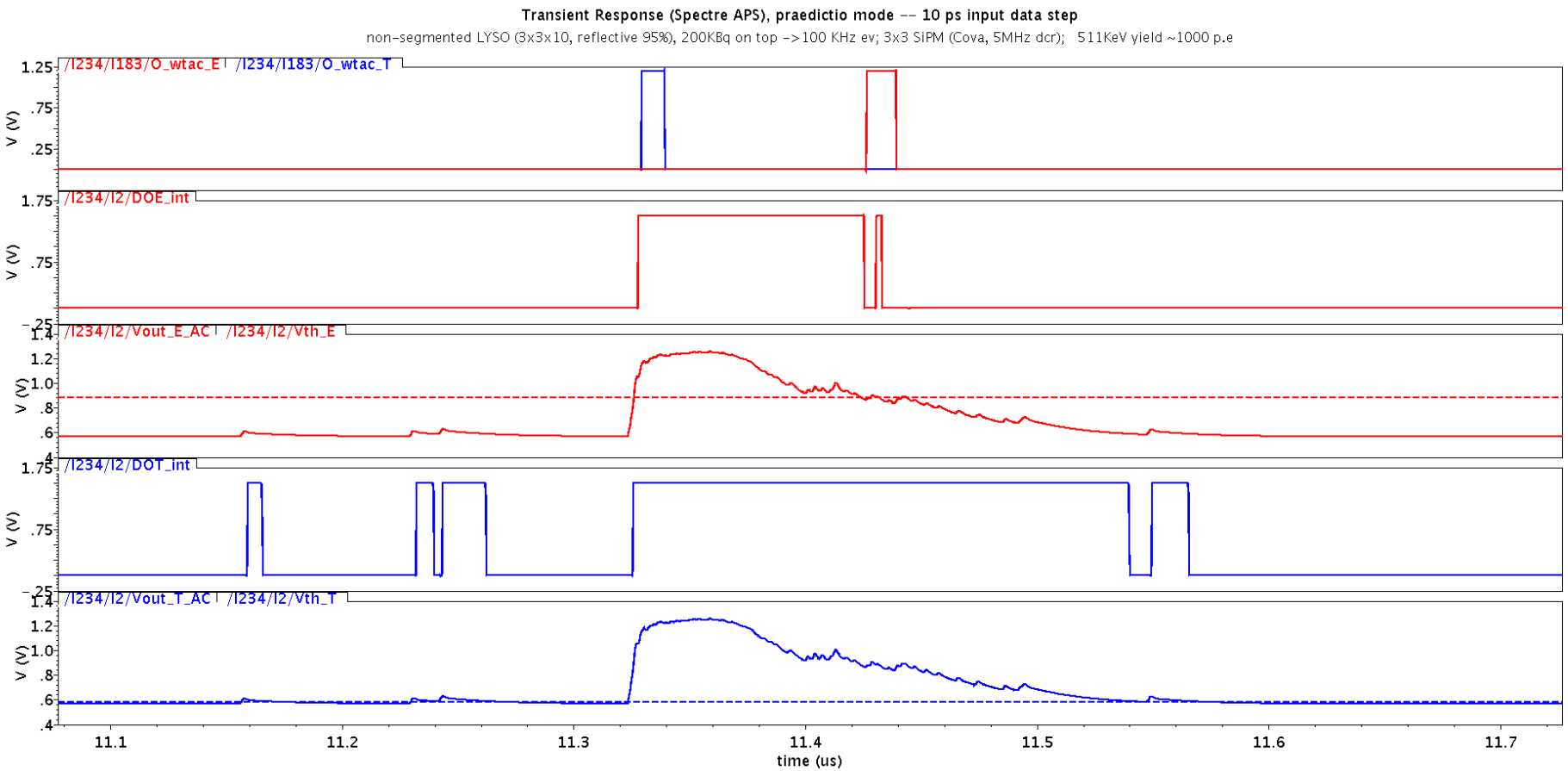
Detail of the channel data register output: id of the TAC written



A low event rate may probably motivate the use of dynamic refresh to the TAC nodes due to the leakage current.

SiPM+LYSO data - detail of event (*praedictio* mode)

Time and Energy thresholds of 0.5 and 7.0 photoelectrons.



Note 1: wtac_T is a write operation after a time trigger - dark pulses masked.
Note 2: Re-trigger of DOE_int due to scintillation statistics and/or spurious pulses is manageable (Vout_E_AC is unfiltered)

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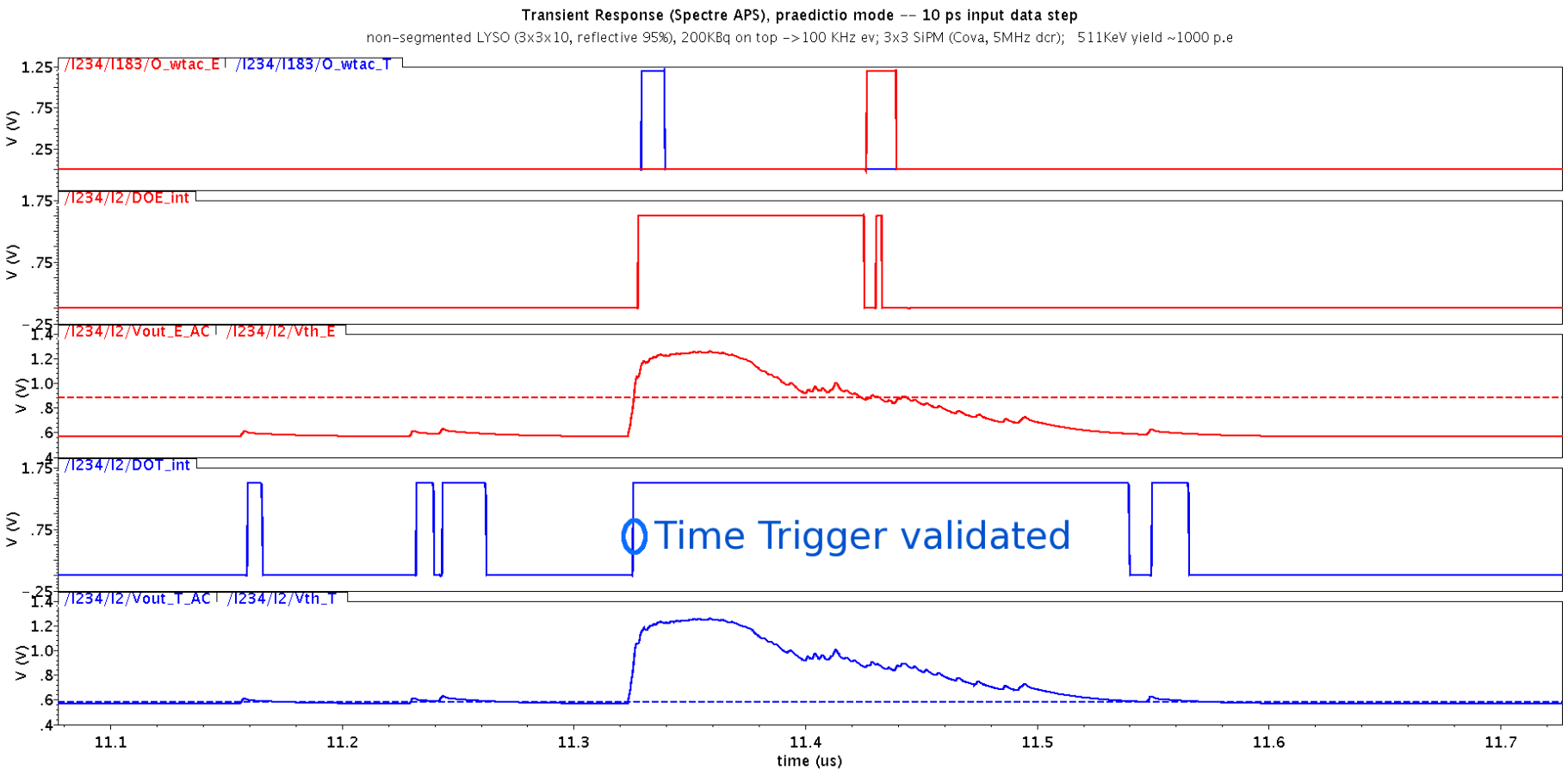

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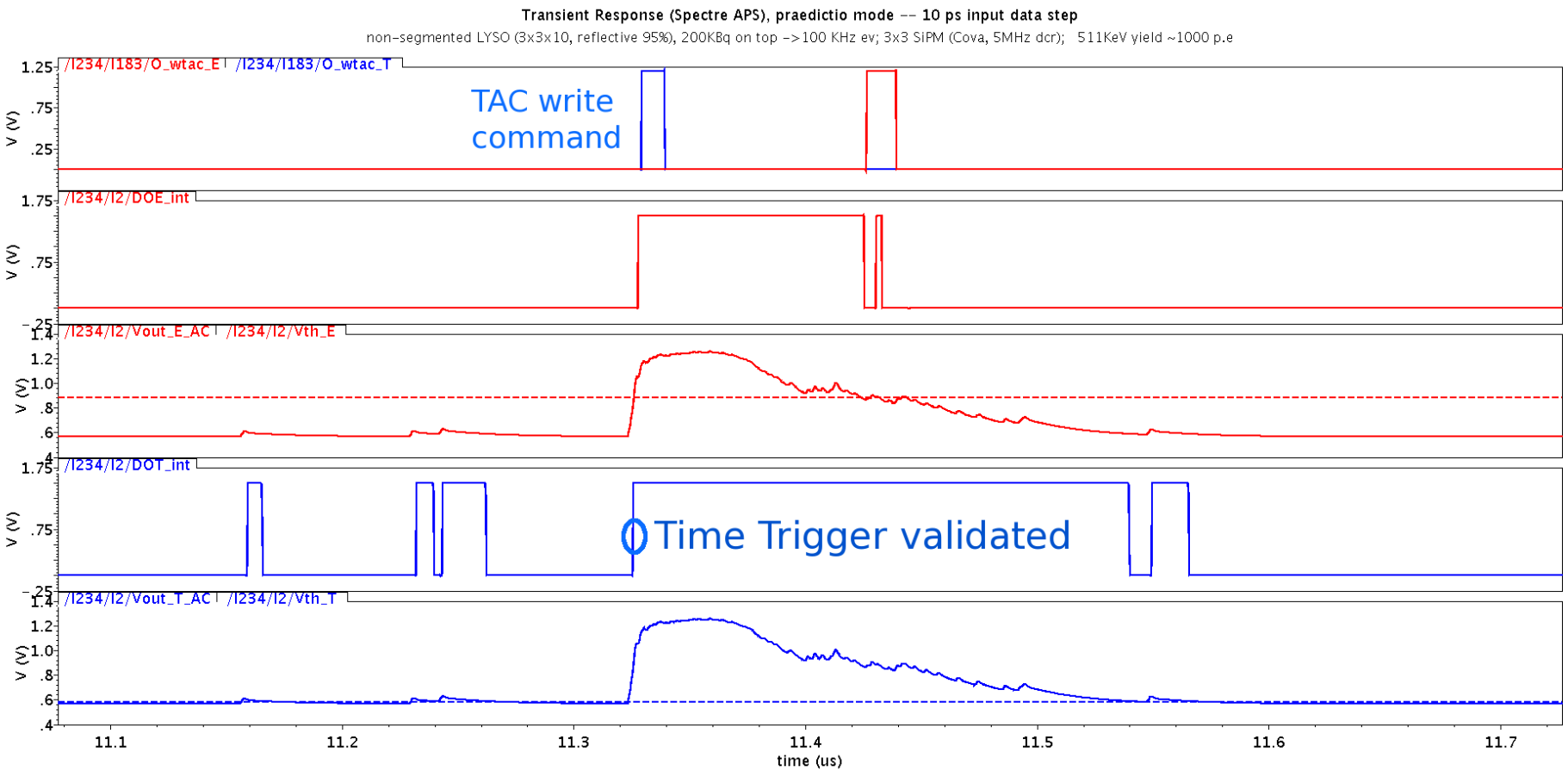

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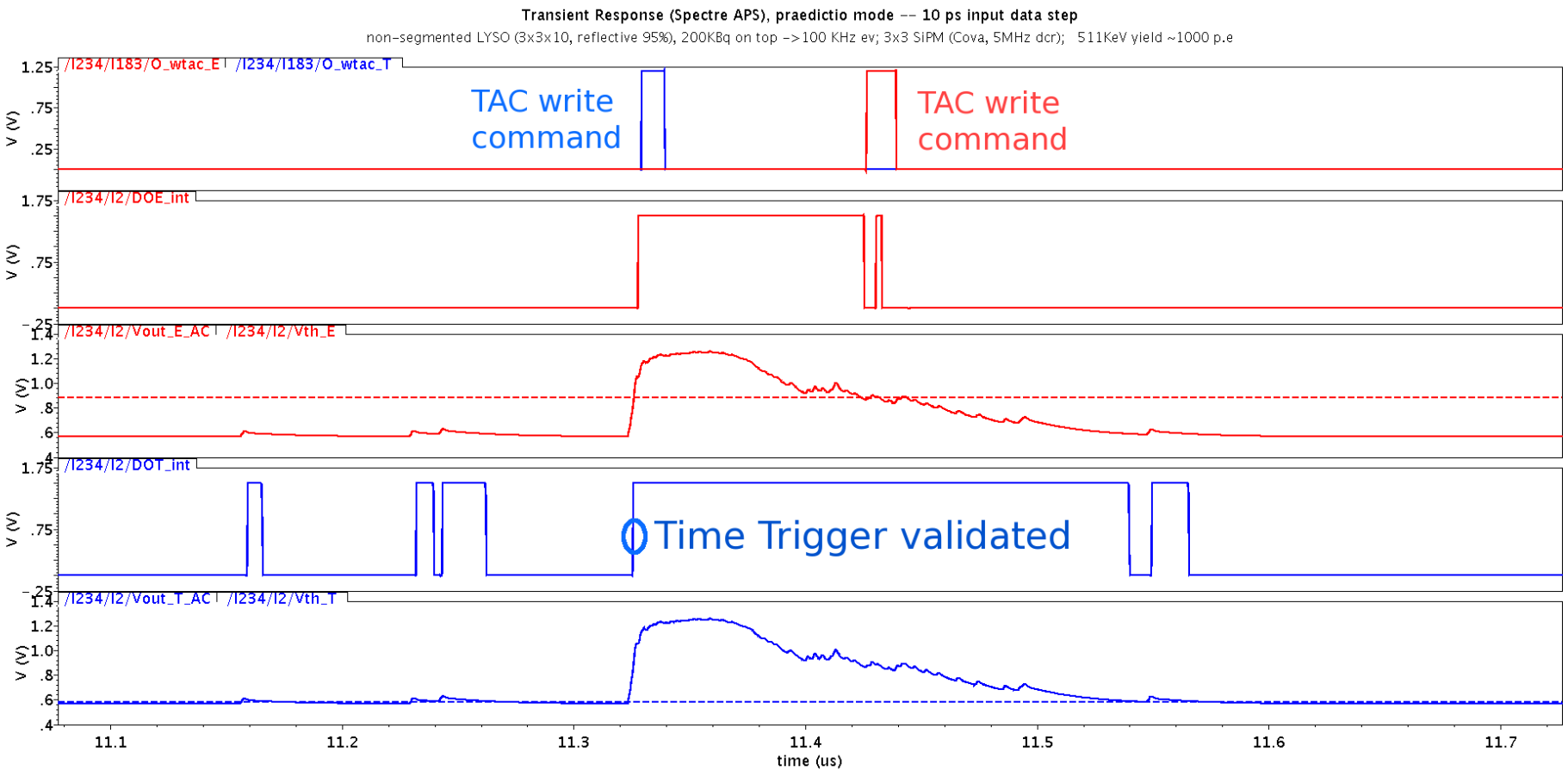
SiPM+LYSO data - detail of event (*praedictio* mode)

Time and Energy thresholds of 0.5 and 7.0 photoelectrons.



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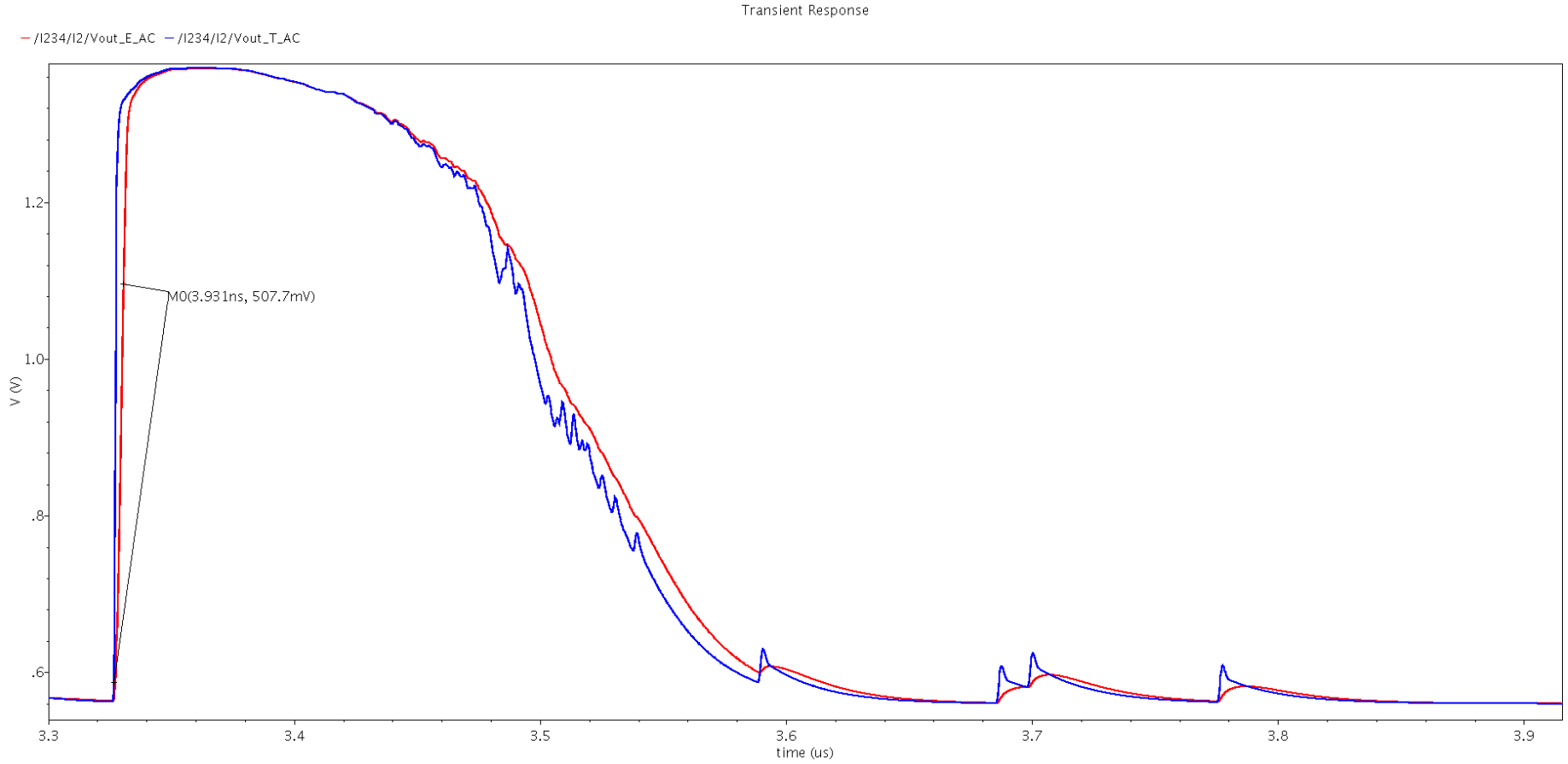
Note 2: Re-trigger of DOE_int due to scintillation statistics and/or spurious pulses is manageable (Vout_E_AC is unfiltered)

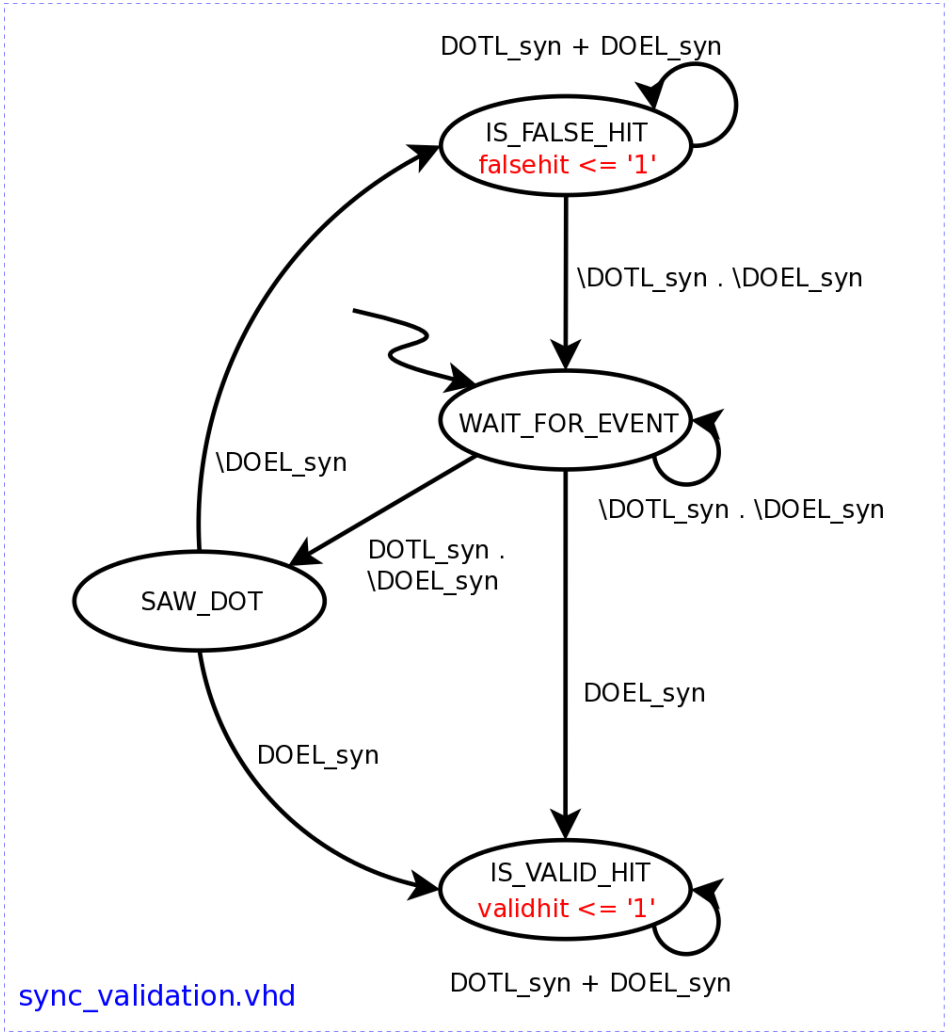
SiPM+LYSO data - detail of event (shaped pulse)

The energy discriminator input Vout_E_AC can be shaped to avoid re-triggering or to guarantee ToT monotonicity:



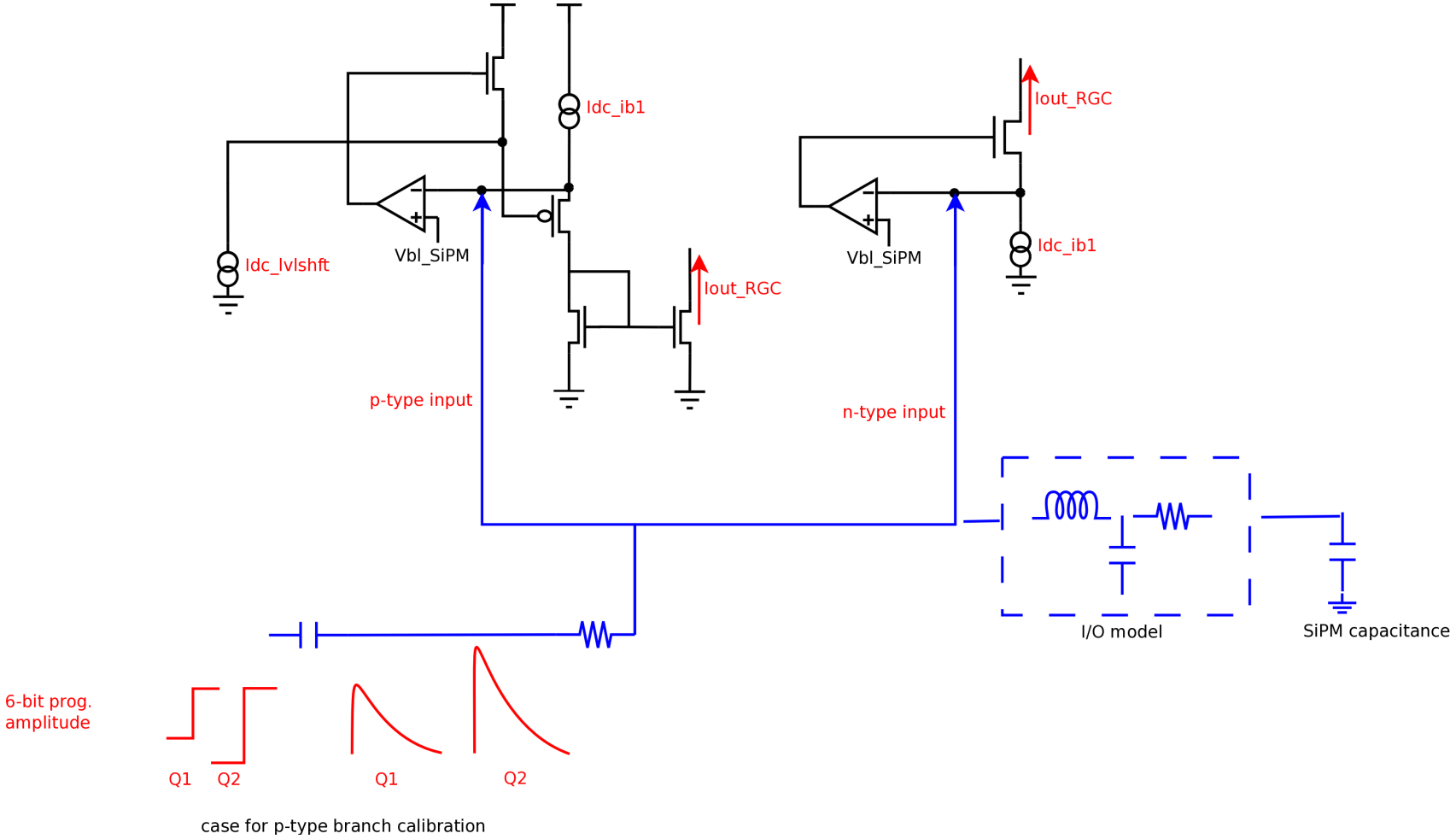
Since the shaping is applied as RC filtering, the rise time is degraded - the delay of the DOT signal has probably to be widened: likely to increase jitter

Rejection of dark pulses



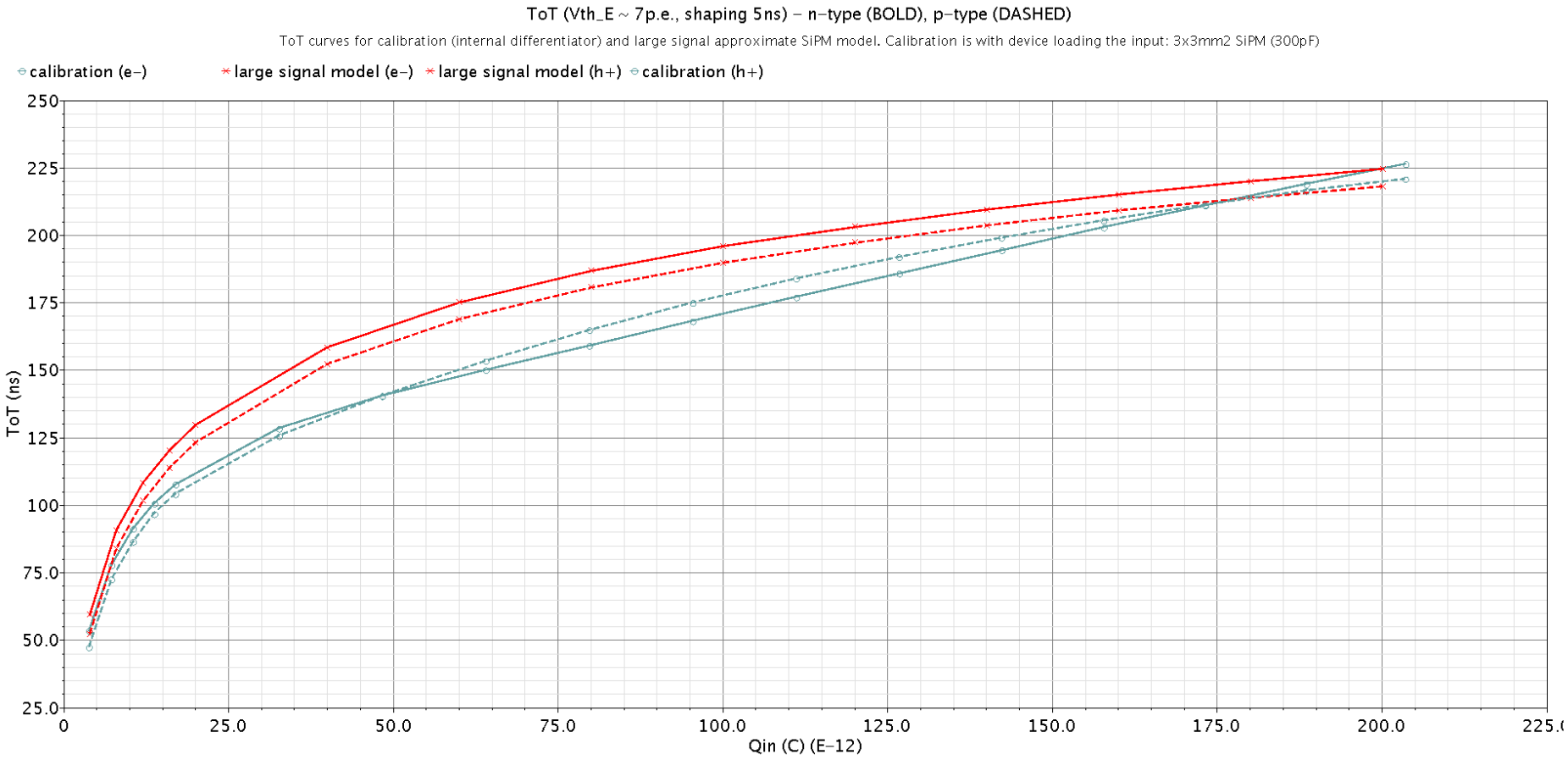
- **SYNC**: The latched and synchronous versions of time (DOTL) and energy (DOEL) triggers are polled every clock (acceptance gate up to 1 clk)
- **ASYNC**: a configurable gate (DOE-DOT) generated by analogue circuitry issues external falsehit and validhit flags - spotting of dc+event overlap
- **PRAEDICTIO**: a delayed version of the DOT is masked unless there is an energy trigger

Calibration mechanism

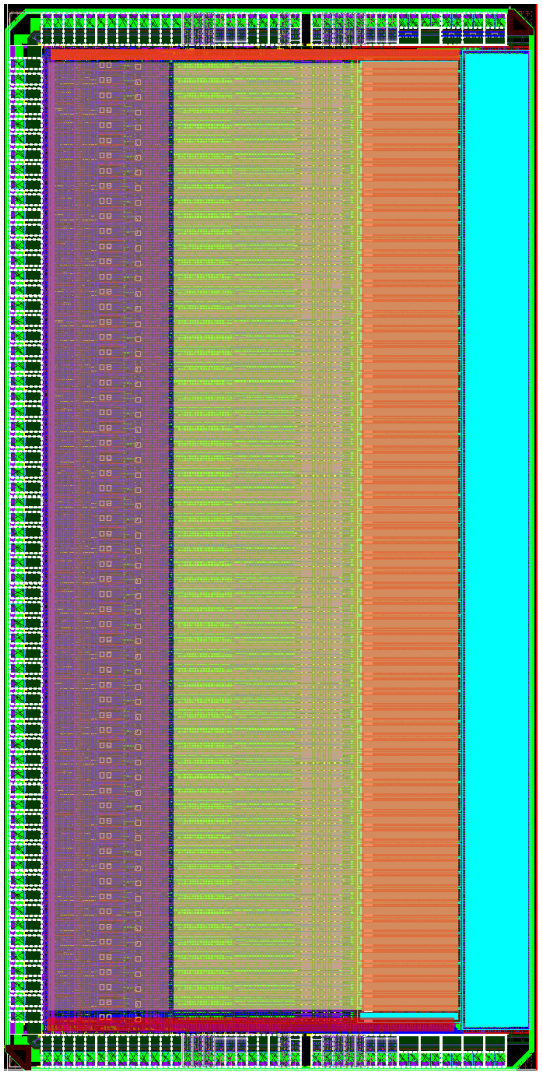


A 6-bit global DAC (current-mode, 20mA conso.) generates a variable amplitude (positive, negative) test pulse, from which an exponential decay is obtained with an RC differentiator.

Time-over-Threshold: internal calibration generator vs. spectre ideal current source



Top floorplan



Front-end

TDC analogue

TDC digital

GCTRL

BIAS cells, golden refs, calibration

- Pre-amplifier, post-amplifier, input Vbl DAC (digital-to-analogue converter), power planes are driven in/out off the chip by dedicated IOs.
- Use of triple-well on sensitive/noisy circuits; Digital block (TDC_CTRL + GCTRL) laid in an island isolated by a 20 μm BFMOAT ring (undoped, highly resistive substrate)
- Two regional pad-rings with independent bias and ESD circuitry.

Bias Reference generators, Safe-mode power-on

Internal biasing is configurable by SPI.

- External bias: VREF for TDC, 2 golden reference voltages for internal current/voltage bias generators;
- Each Bias cell is configurable with a 6-bit DAC;
- GCTRL imposes a default configuration vector (tackles SPI problems, noisy power-on, ...) for a testable chip:
  - SiPM Vbl = 650mV
  - Vth_T = 4 p.e.
  - Vth_E = 7 p.e.
  - n-type input
  - nominal 5k TIA gain
  - 'praedictio' mode active
  - TDC - 1 buffer for synchronization (metastability)
  - 5ns shaping of Vout_E
  - ...