The Data Acquisition for the PANDA Phase-0 Experiment at MAMI

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- EMC Meeting, Bochum -

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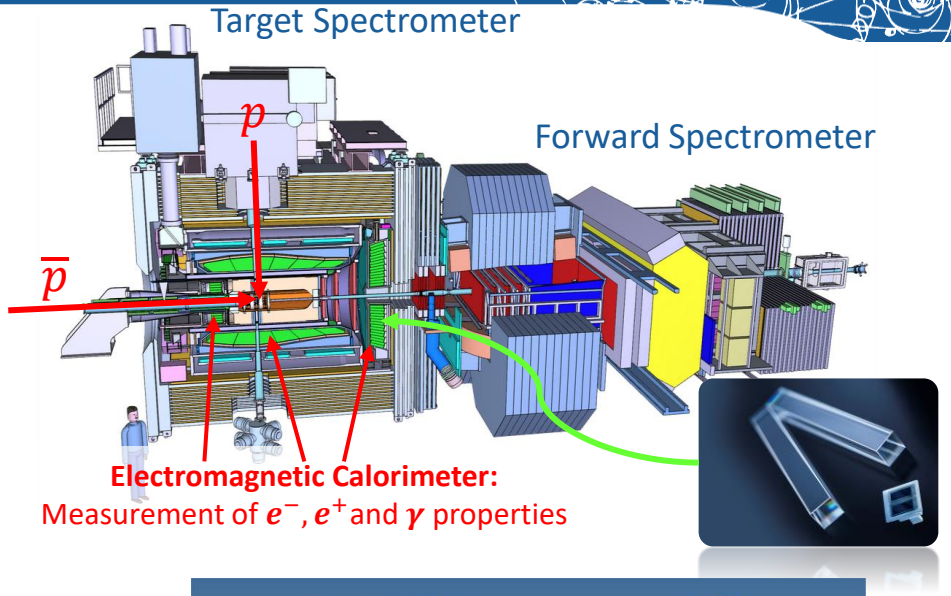
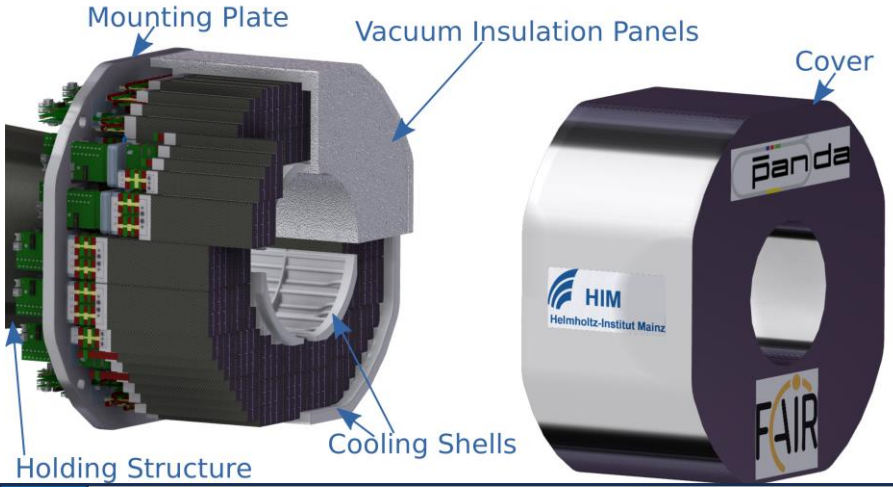
Outline

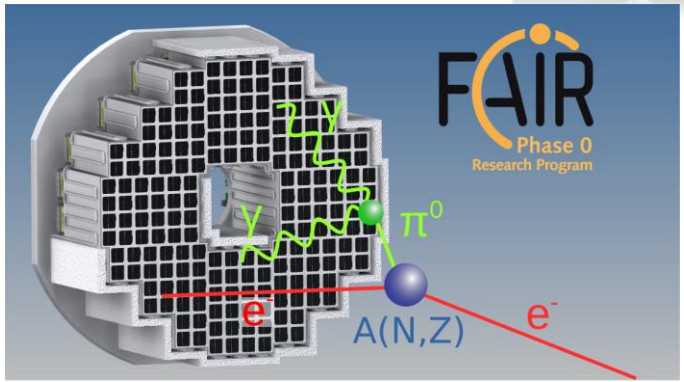
1. The PANDA Phase-0 Experiment at MAMI
2. The Data Acquisition Concept
3. Network Topology
4. Feature Extraction (Benchmarks)
5. Time Sorted Hit Packaging and Triggered Readout

FAIR, PANDA and FAIR Phase-0

- Facility for Antiproton and Ion Research (FAIR)
- **antiProton ANnihilation at DArmstadt (PANDA)**
  - **1.5 GeV/c – 15 GeV/c** ($\Delta p/p \sim 10^{-4}$)
  - Fixed target experiment
  - $\mathbf{2 \cdot 10^7}$ $\bar{p}p$ annihilations/second
  - Excellent particle identification
  - Radiation tolerance of the materials







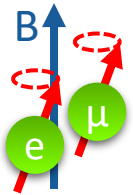
A FAIR Phase-0 Experiment at the Mainz Microtron

The $g_\mu - 2$-Puzzle

$g = \frac{\mu_s}{\mu_L} = \mathbf{2}$, point-like spin-$\frac{1}{2}$ particles (Dirac-Theory)

$a_l = \frac{g_l - 2}{2} = \mathbf{0}$, anomalous magnetic moment

Radiative corrections → $a_l \neq 0$



$$a_\mu^{\mathrm{SM}} = 0.00116591782(43)$$

$$a_\mu^{\mathrm{Exp.}} = 0.00116592061(41)$$

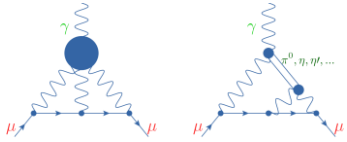
$4.2\,\sigma$

FermiLabs, 2021

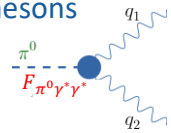
Standard Modell Calculation

$$a_\mu^{\mathrm{SM}} = a_\mu^{\mathrm{QED}} + a_\mu^{\mathrm{EW}} + a_\mu^{\mathrm{QCD}}$$

nonperturbative



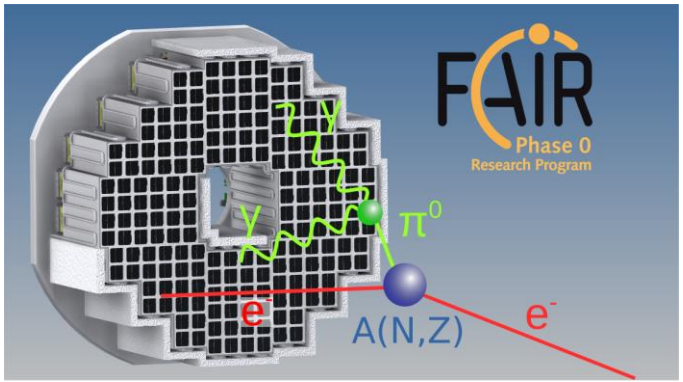
- Hadronic Light-by-Light scattering
- Huge contribution to uncertainty
- Pseudo scalar (PS) mesons π^0, η, η'



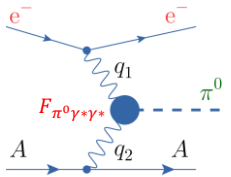
Data-driven approach

$$a_\mu^{HLbL,PS} = \int_0^\infty dQ_1 \int_0^\infty dQ_2 \int_{-1}^{1} d\tau\, w(Q_1, Q_2, \tau) F_{PS\gamma^*\gamma^*}(-Q_1^2, -(Q_1+Q_2)^2) F_{PS\gamma^*\gamma^*}(-Q_2^2, 0)$$

V. Pauk, M. Vanderhaeghen 2014, M. Hoferichter 2018

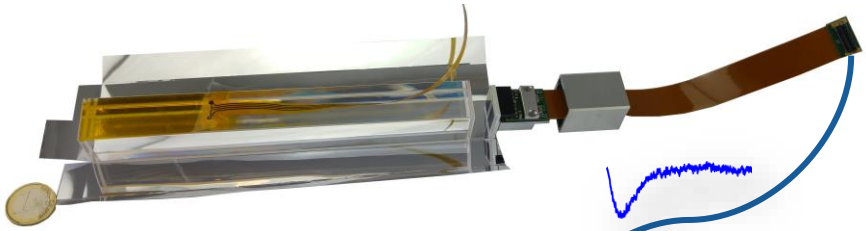


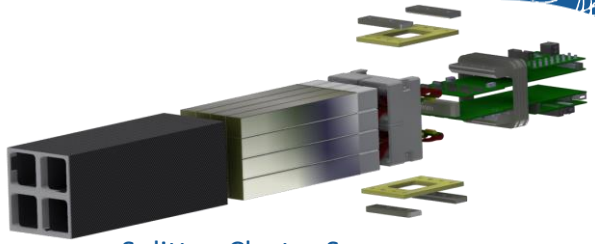
- FAIR Phase-0: FAIR detectors in stand-alone experiments
- PANDA backward calorimeter is completely developed ✓
- Measurement of the double virtual pion transition form factor (TFF) $F_{\pi^0\gamma*\gamma*}$ for spacelike momenta
- Primakoff electroproduction
- A1 experimental hall of Mainz Microtron
- Electron beam on highly charged target



Measurement of the Electromagnetic Transition Form Factor of the π^0 in the Space-Like Region via Primakoff Electroproduction. Letter of Intent, 2020

Signal Digitisation and Processing



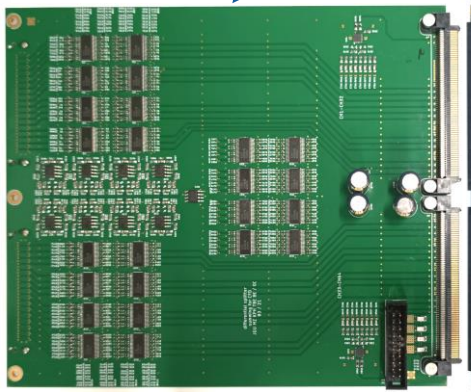


High Voltage and Control

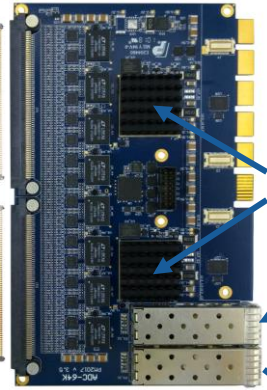
Amplification

Temperature Readout

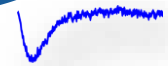
Splitter, Cluster Sum



PANDA SADC

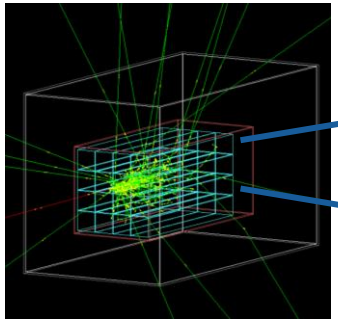


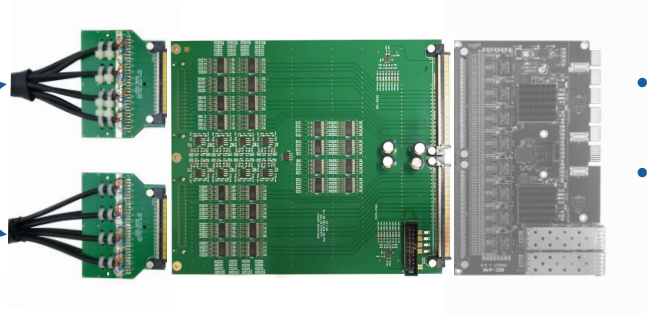
FPGAs



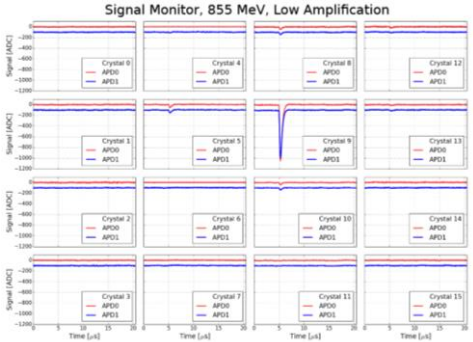
(E, T_0)

Analogue Cluster Trigger





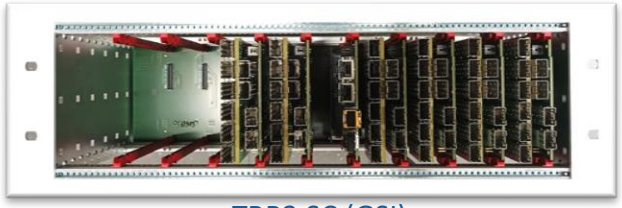
- Splitter, Backplane and CFD tested ✓
- Splitter boards and backplanes in production



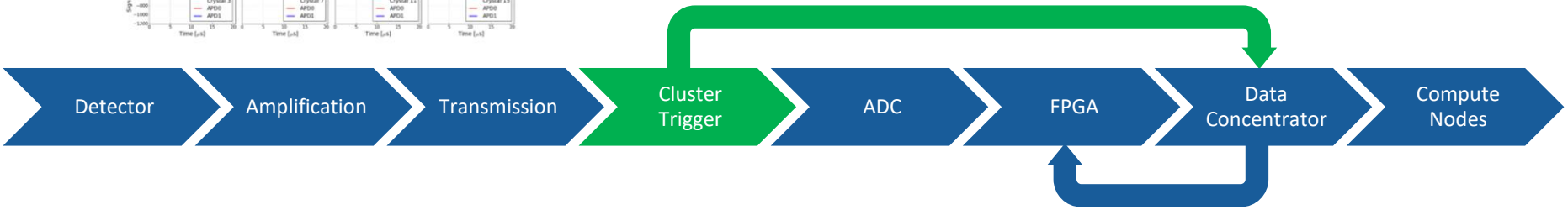
$\sum_{LG=0}^{7}$ → CFD

$\sum_{LG=8}^{15}$ → CFD

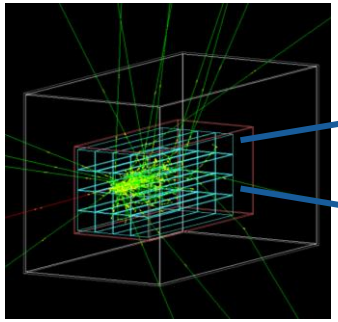
Analogue delay < 200 ns

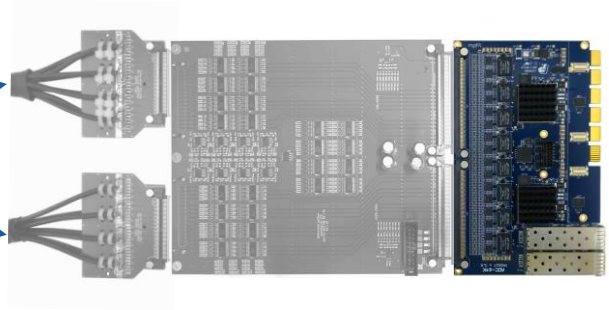


TRB3 SC (GSI)

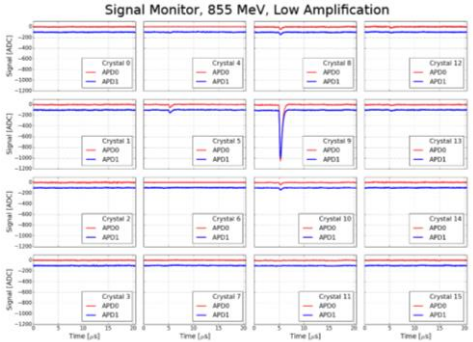


Data Concentrator and Clock/Trigger Distribution





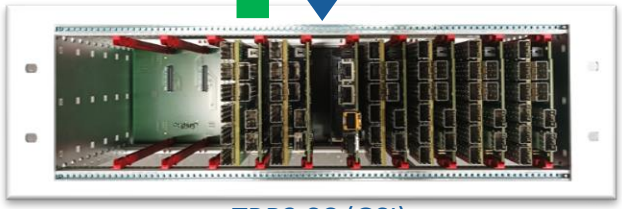
- Digital trigger implemented ✓



$\sum_{LG=0}^{7}$ → CFD

$\sum_{LG=8}^{15}$ → CFD

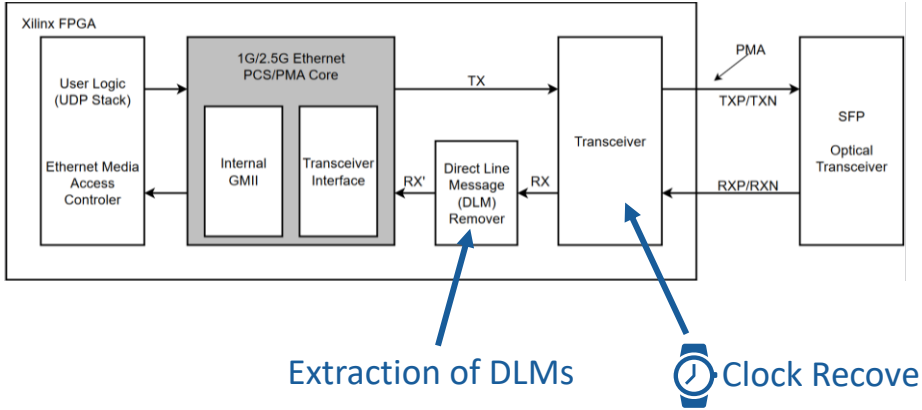
Throughput Time < 200 ns



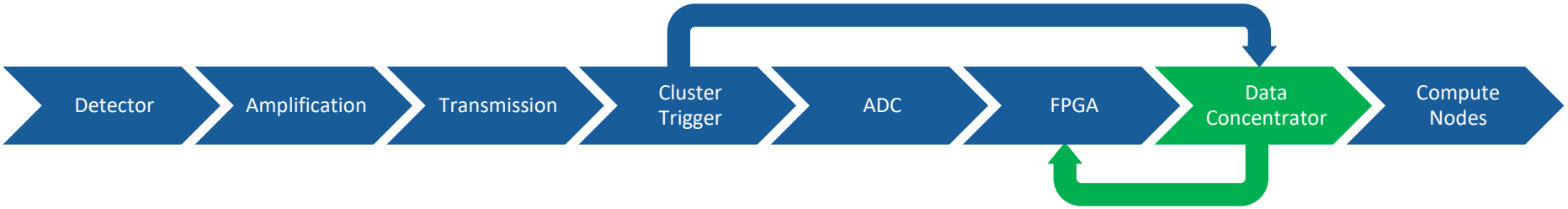
TRB3 SC (GSI)

Detector → Amplification → Transmission → Cluster Trigger → ADC → FPGA → Data Concentrator → Compute Nodes

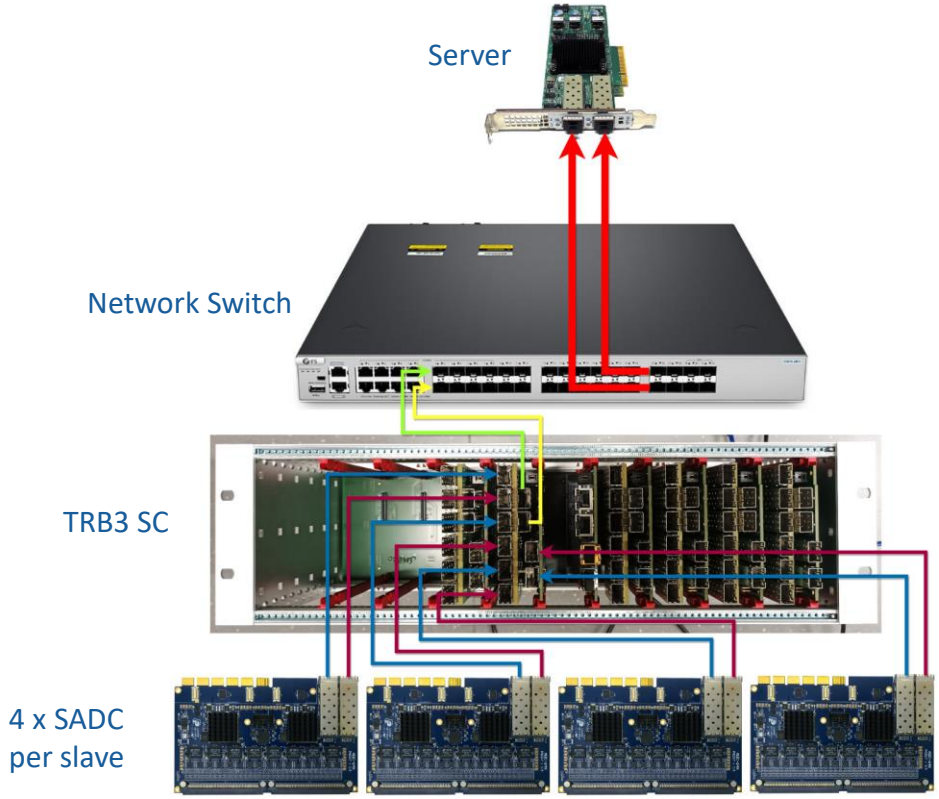
Direct Line Messages (DLMs)



- Need of defined and finite trigger propagation
- Network transport layer (4) is not “direct”
- Utilising control symbols within 8b/10b encoding
- Development of DLM protocol with Michael Böhmer (TU München)
- Many possibilities:
  - Arbitrary payload
  - Different trigger types
  - Synchronous resets
  - …
- Core features implemented on SADC ✓



Network Topology – Working Solution



- 40 SADC (80 x 1 Gbit/s)
- 10 x TRB 3 SC slaves (2 x Crates)
  - 4 SADCs per slave
  - 2 Uplinks
  - 8 Gbit/s → 2 Gbit/s (VLAN)
- Switch: 20 Gbit/s → 2 x 10 Gbit/s
- Network bandwidth reduction factor: 4

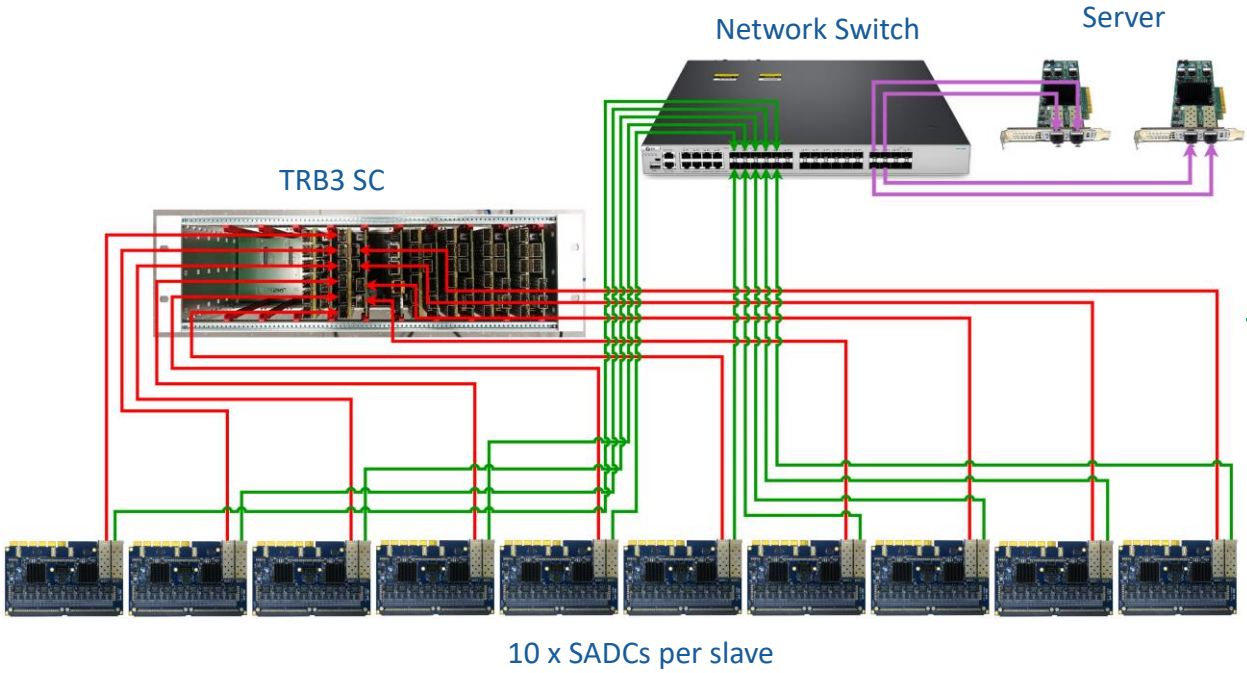
Pros:

- Working solution (VLAN is implemented on SADC)
- No data transfer between FPGAs is needed

Cons:

- Need for second TRB Crate
- (Small) increase of complexity
- Bandwidth reduction (factor 4)

Network Topology – Aspired Solution



- 40 SADC (80 x 1 Gbit/s)
- 4 x TRB 3 SC slaves (1 x Crate)
  - 10 SADCs per slave
- Direct uplink to switch (40 uplinks)
- Switch: 40 Gbit/s → 4 x 10 Gbit/s
- Network bandwidth reduction factor: 2

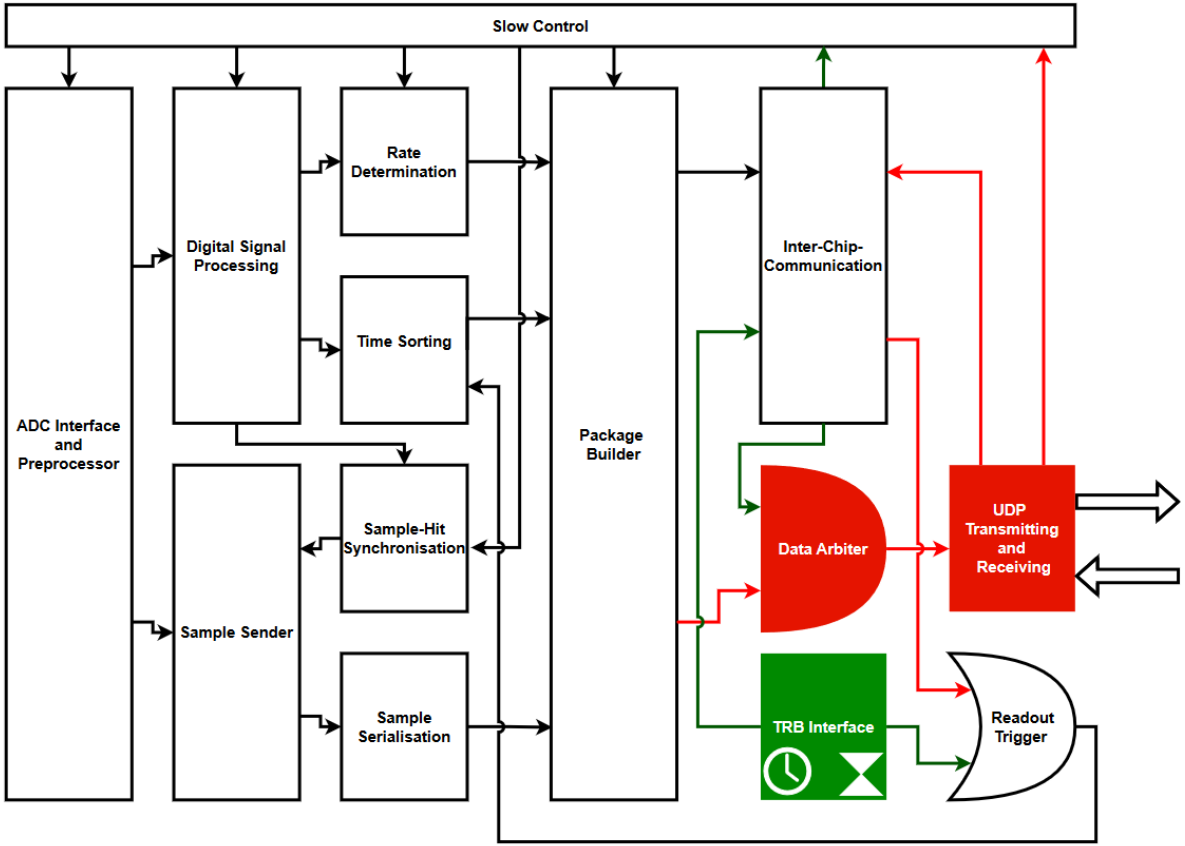
Pros:

- Simplification of network traffic in TRB
- VLAN can be used to optimise layer 2
- Bandwidth reduction (factor 2)
- More hardware backup (second TRB crate is not needed)

Cons:

- SADC firmware is a bit more complex

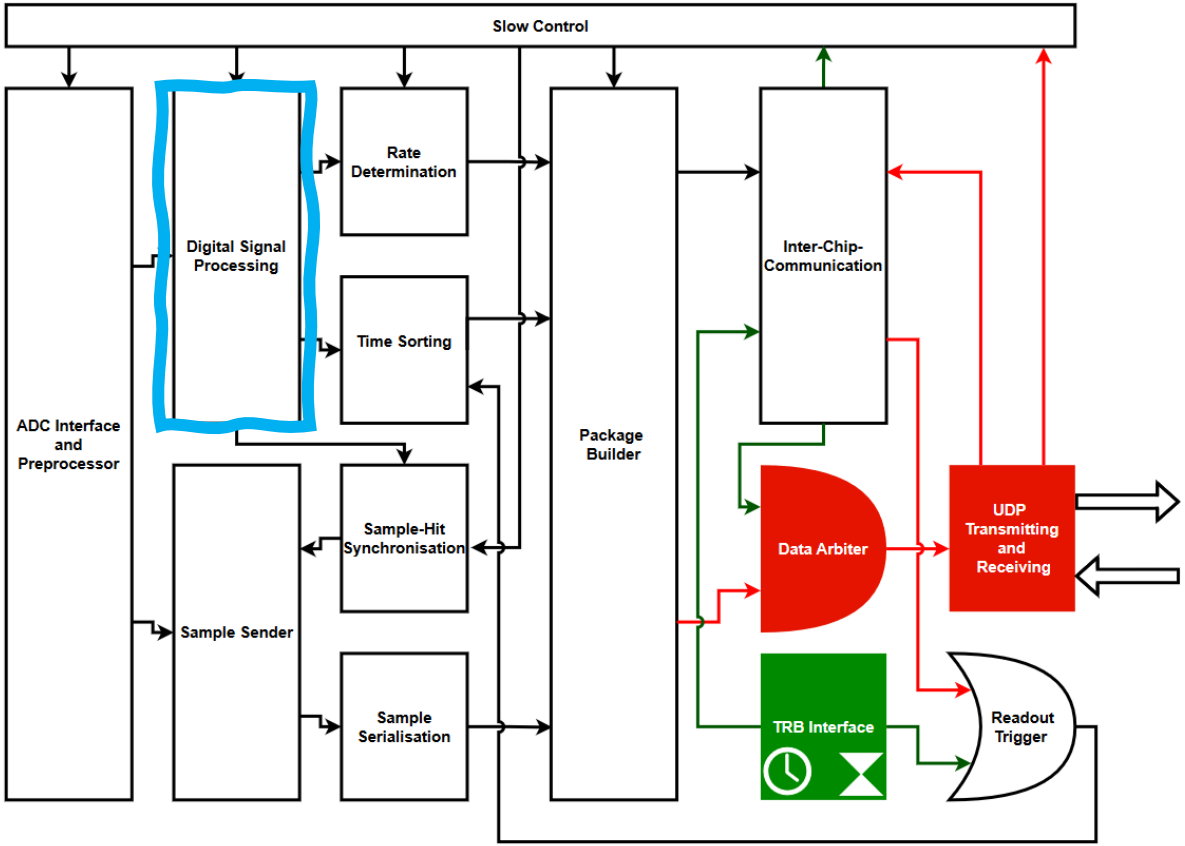
SADC Firmware



- Blocks in black: active on both FPGAs
- Block in green: active on FPGA connected to TRB3 SC
- Blocks in red: active on FPGA connected to network switch

- Same firmware for both FPGAs
- Behaviour is determined by GEO-Address

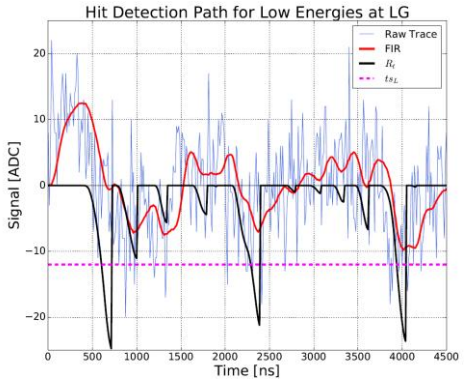
SADC Firmware



- Reminder of feature extraction methods
- Performance of feature extraction

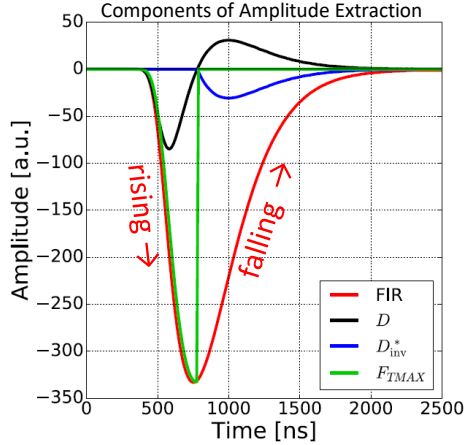
Digital Pulse Identification and Parameter Extraction on FPGA

Identification



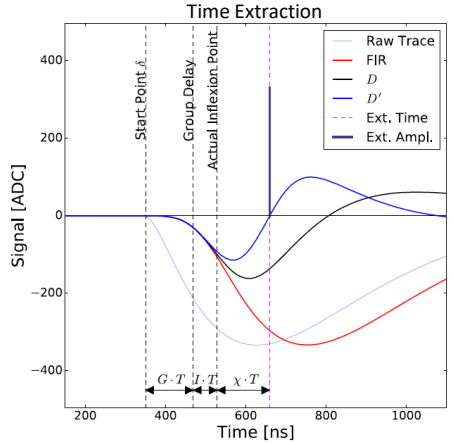
- FIR filter
- Extraction function
- Highly sensitive on pulse shape
- Improvement of detection efficiency (small energies!)

Digital Pulse Shaping



- Derivation → Integration
- Built-in baseline follower
- Elimination of falling edge
- Pileup detection and correction

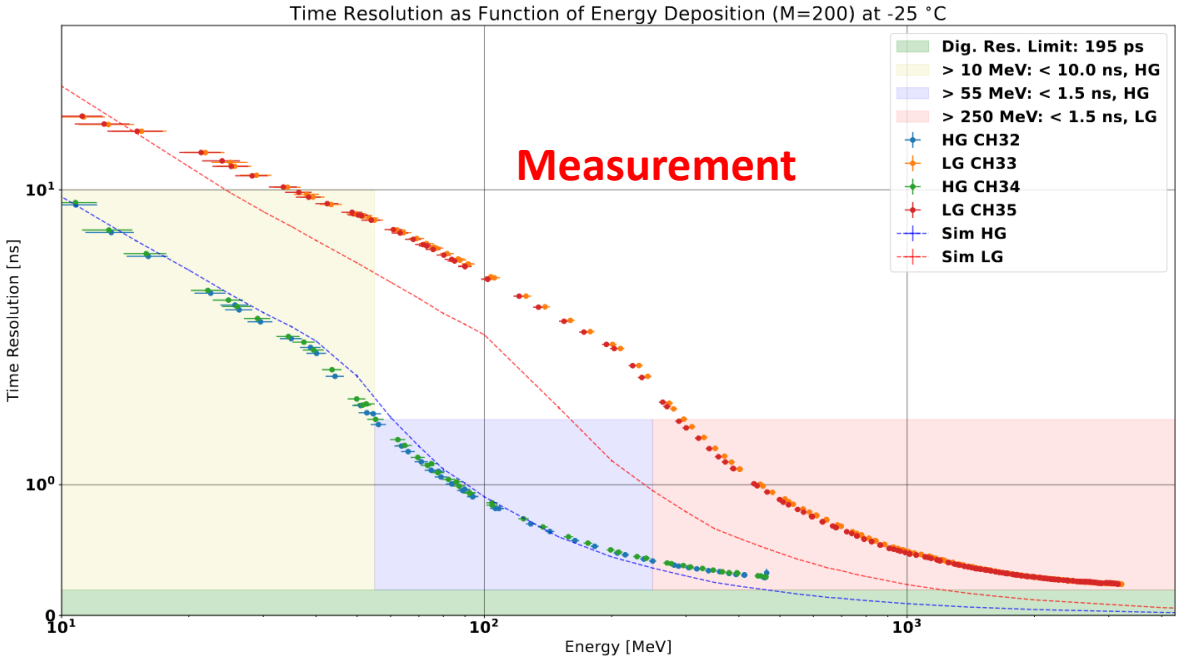
Time

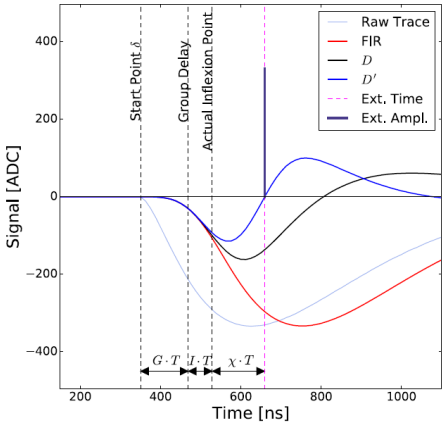


- T_0 at inflexion point ($f''(x) = 0$)
- Discrete derivation → Interpolation

Detector → Amplification → Transmission → Cluster Trigger → ADC → FPGA → Data Concentrator → Compute Nodes

Digital Pulse Identification and Parameter Extraction - Performance



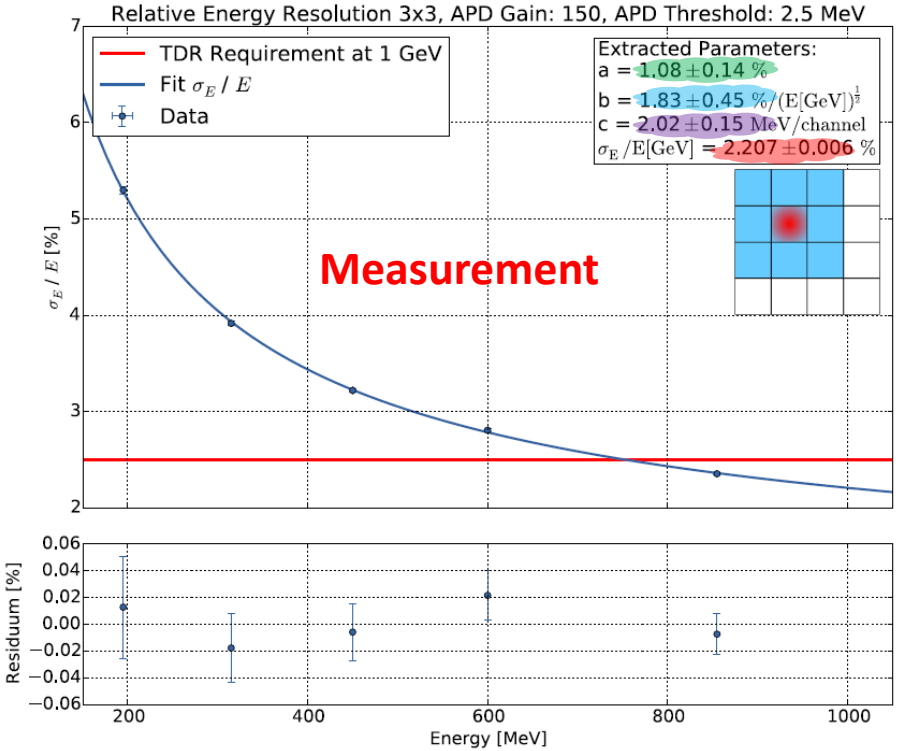


Hit ready																	
Time left			i_0 (34-bit)														
Hit data	Amplitude (16-bit)					Dividend (10-bit)						Divisor (10-bit)					
Assignment	35	34	33	...	20	19	18	...	12	11	10	9	8	...	2	1	0

Table 1. Output of the digital signal processing unit of one ADC channel for one hit.

- Light pulser measurement (2024)
- Measurement in agreement with simulation (High Gain)
- Discrepancy between measurement and simulation for Low Gain due to digital resolution limitations
- But < 1 ns at the relevant region

Digital Pulse Identification and Parameter Extraction - Performance



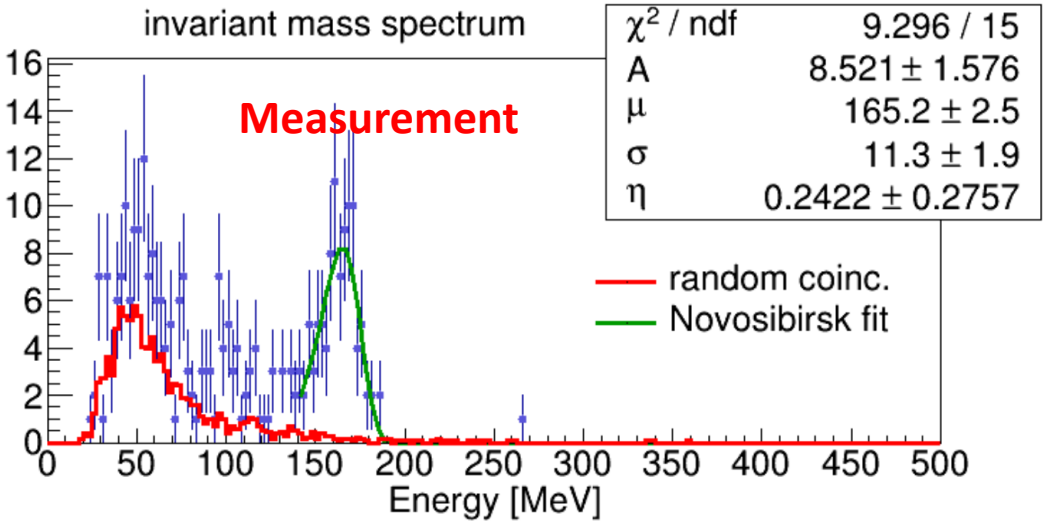
- Relative Energy Resolution (2018)

$$\frac{\sigma_E}{E} = \underbrace{a}_{\text{Constant}} \oplus \underbrace{\frac{b}{\sqrt{E}}}_{\text{Stochastic}} \oplus \underbrace{\frac{c}{E}}_{\text{Noise}} = \sqrt{a^2 + \frac{b^2}{E} + \frac{c^2}{E^2}}$$

PANDA Technical Design Report (TDR) requirements:

- $a_{\mathrm{TDR}} \leq 1\%$ ✓
- $b_{\mathrm{TDR}} \leq 2\,\frac{\%}{\sqrt{\mathrm{GeV}}}$ ✓
- $c_{\mathrm{TDR}} \leq 3\ \mathrm{MeV}$ ✓
- $\sigma_E/E(1\ \mathrm{GeV})_{\mathrm{TDR}} \leq 2.5\%$ ✓

Digital Pulse Identification and Parameter Extraction - Performance



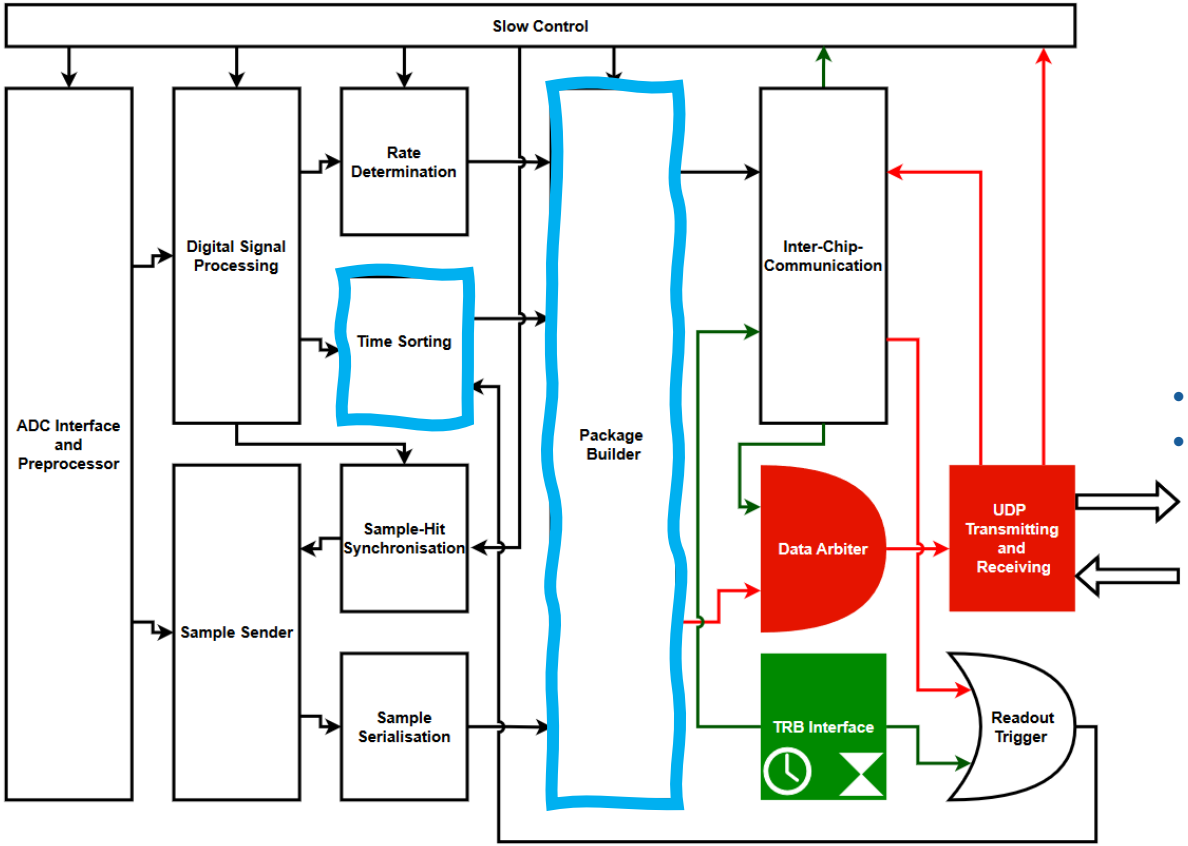
Back then:

- Measurement of neutral pion decay with two 4x4 prototypes in 2022
- Synchronisation with light pulser
- Energy calibration not optimal

Today:

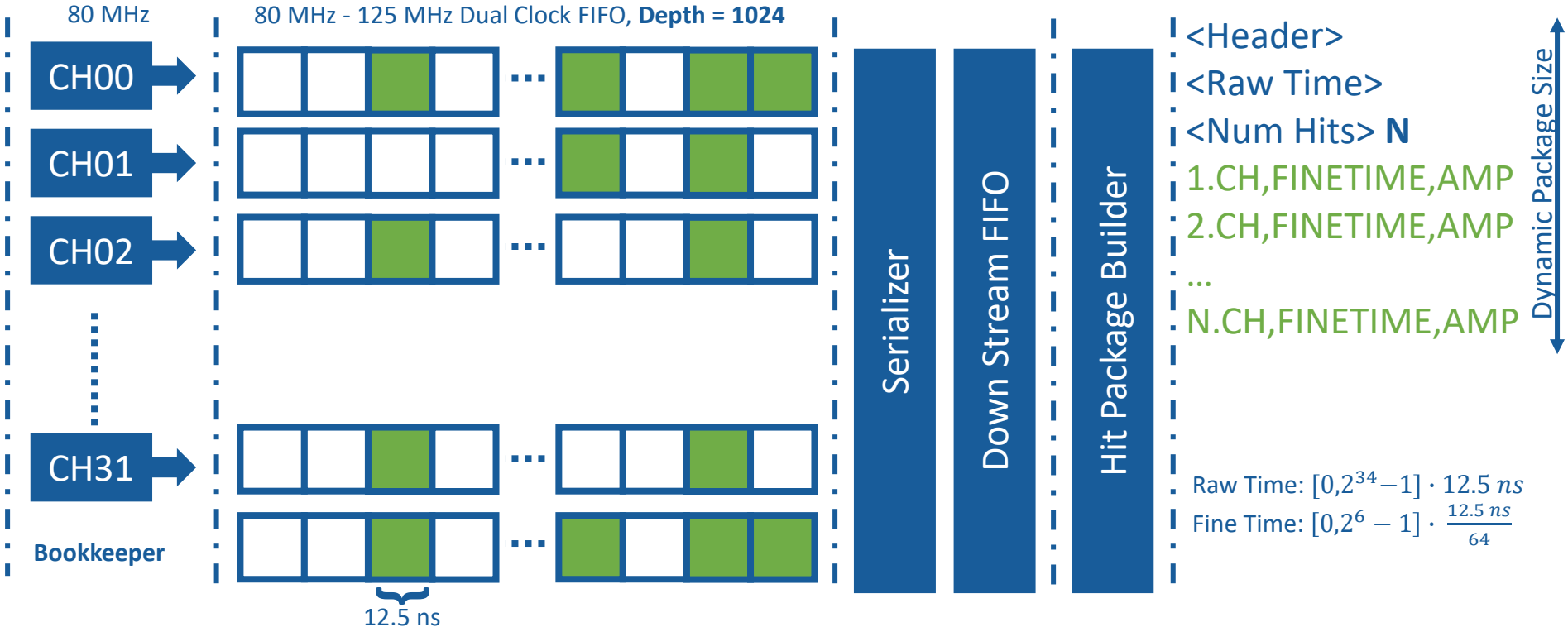
- Now synchronisation with TRB3 SC
- Well calibrated subunits for Phase-0

SADC Firmware



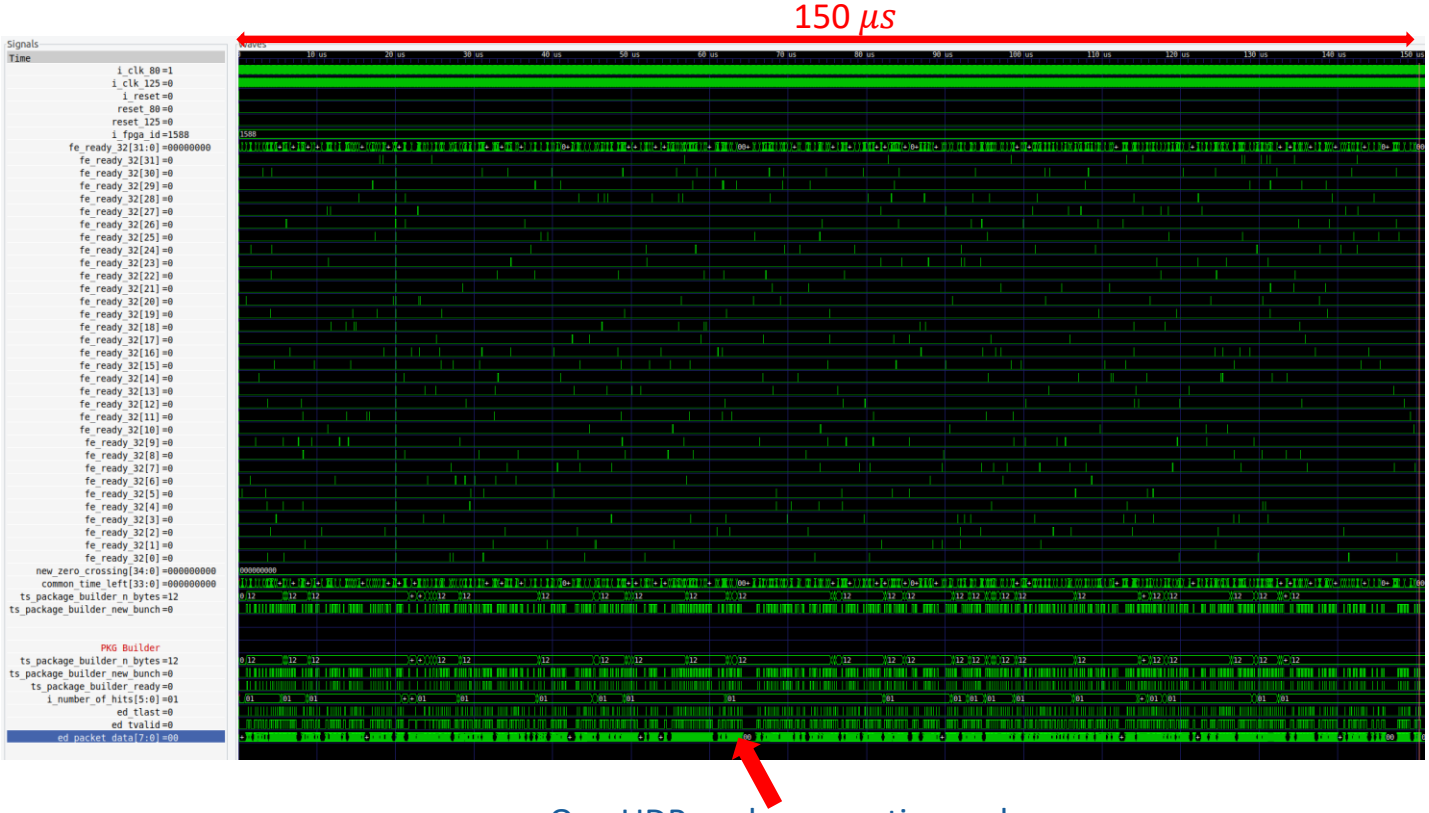
- Optimisation of time sorted hit packaging
- Preparation for triggered readout

Time Sorted Hit Packaging on FPGA



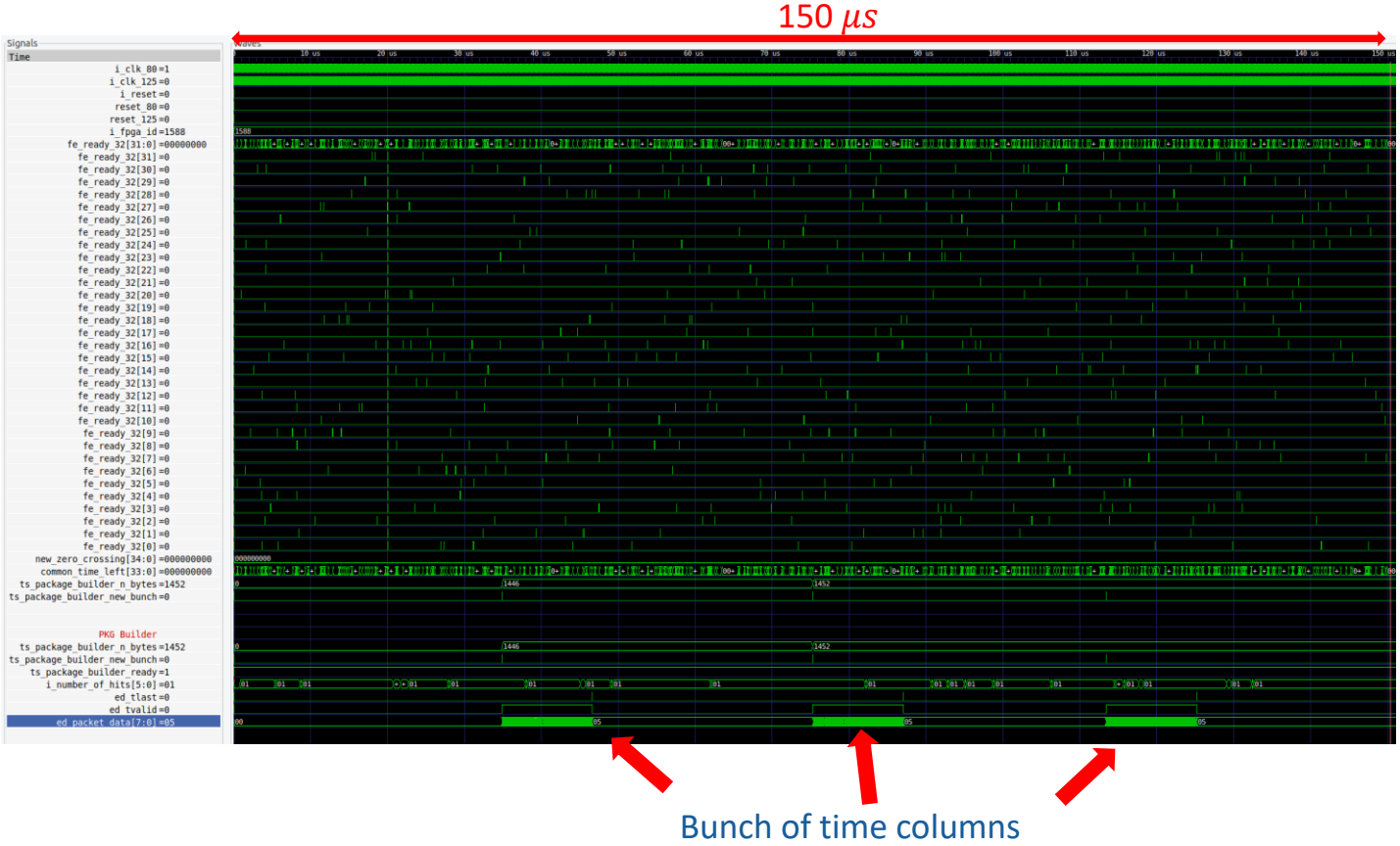
Detector → Amplification → Transmission → Cluster Trigger → ADC → **FPGA** → Data Concentrator → Compute Nodes

Time Sorted Hit Packaging on FPGA



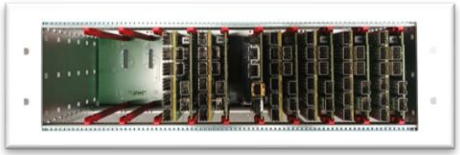
- Working and tested implementation
- Huge improvement for cluster building algorithm in analysis
- Busy TX lane

Time Sorted Hit Packaging on FPGA - Update



- Filling package with time columns up to UDP payload limit
- Or: timeout [0:65535] ns
- Timeout = 0 ns → former case
- Working and tested implementation
- Measured free streaming capability:
  - 310 kHz / channel
  - 19.84 MHz / SADC
  - Trace monitor
  - Rate monitor
  - Config monitor

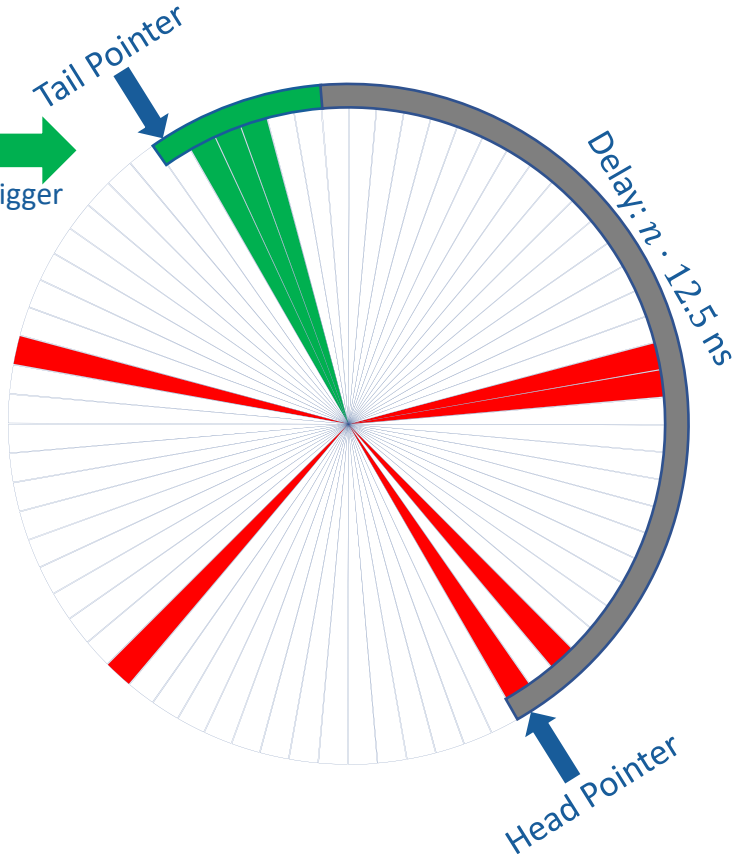
Time Sorted Hit Packaging on FPGA – Triggered Readout



Data Concentrator TRB3 SC (GSI)

DLM

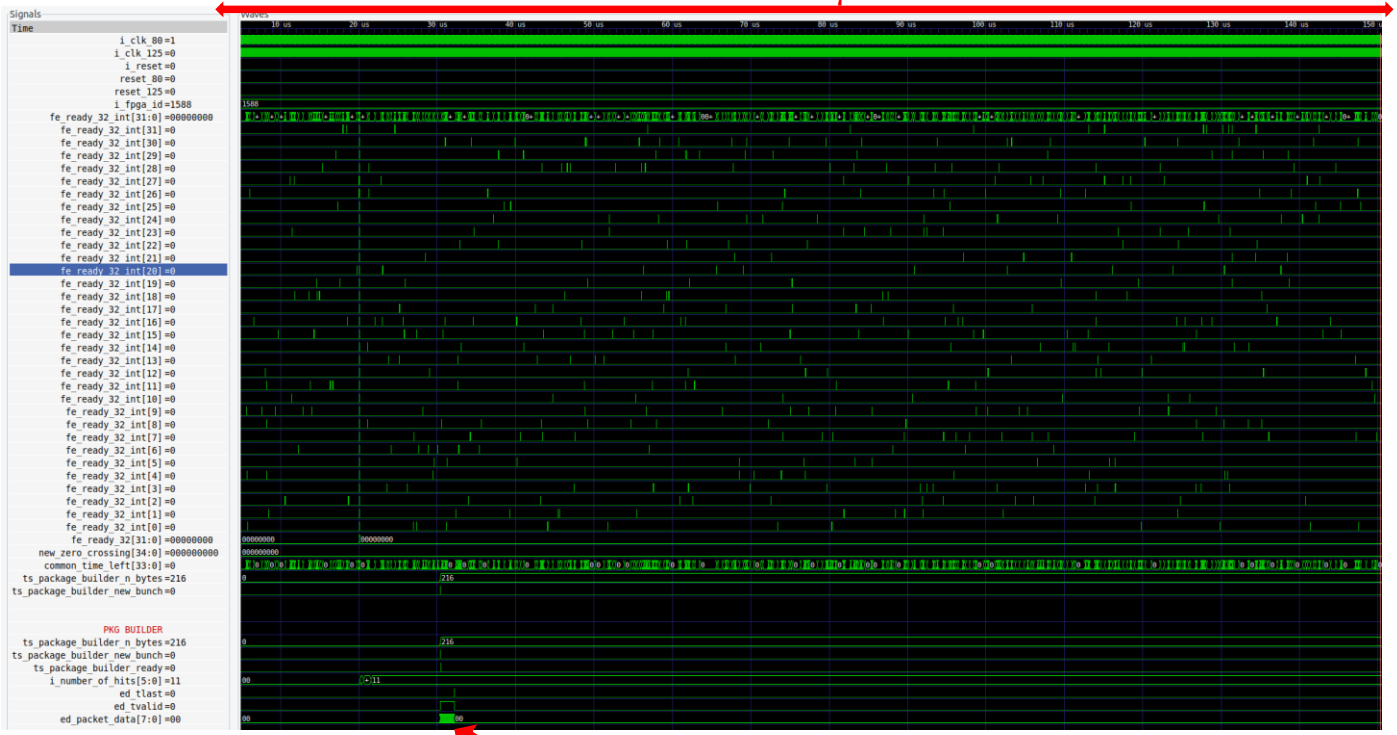
Readout Trigger



- Readout trigger from TRB3 SC
- Configurable delay (trigger → gate open)
- Configurable gate length

Time Sorted Hit Packaging on FPGA - Update

150 μs

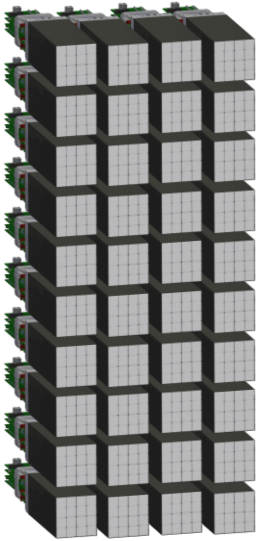


Bunch of time columns within 100 ns gate

- Sending only time columns within gate after trigger
- Dramatically decrease of network load
- System is still internally “free streaming”

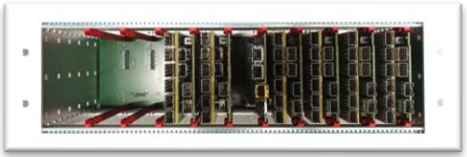
PANDA Phase-0 Data Acquisition Benchmarks

- 640 Crystals
- 1280 APDs

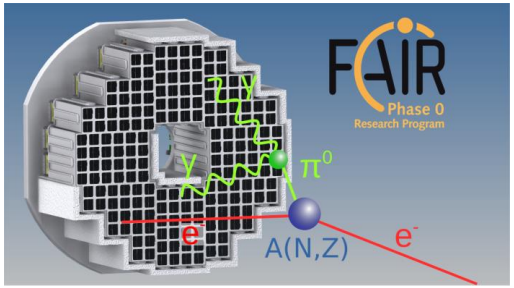


- 40 SADCs
- 2560 Channels

- TRB3 SC
  - Clock
  - Trigger



- Data Throughput

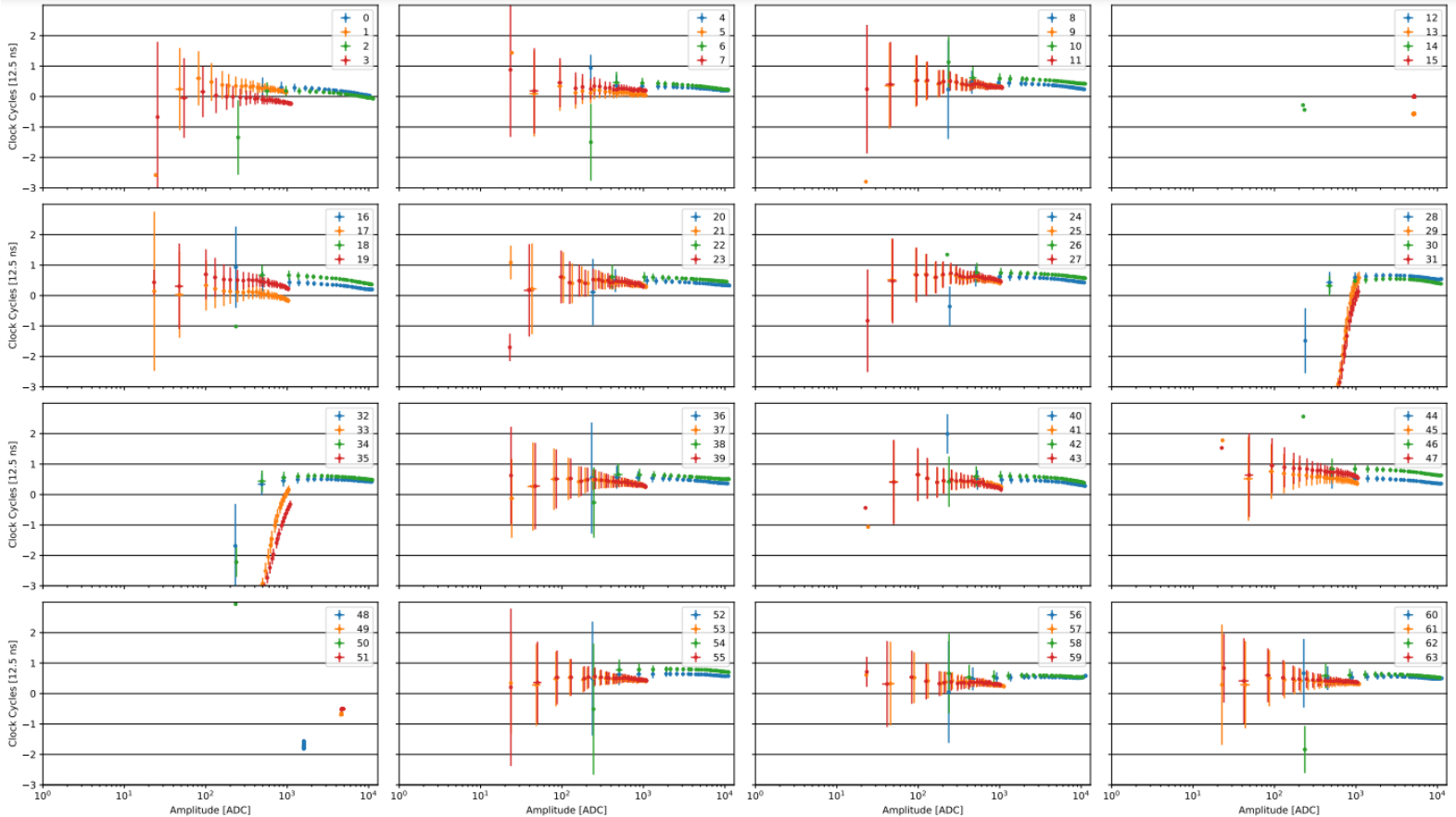


- Exclusive event rate O(mHz)
- Event hit rate ~ 200 kHz/Channel
- Free streaming bandwidth O(40 Gbit/s)
- Trigger rate O(100 kHz)
- Trigger mode bandwidth O(100 Mbit/s)

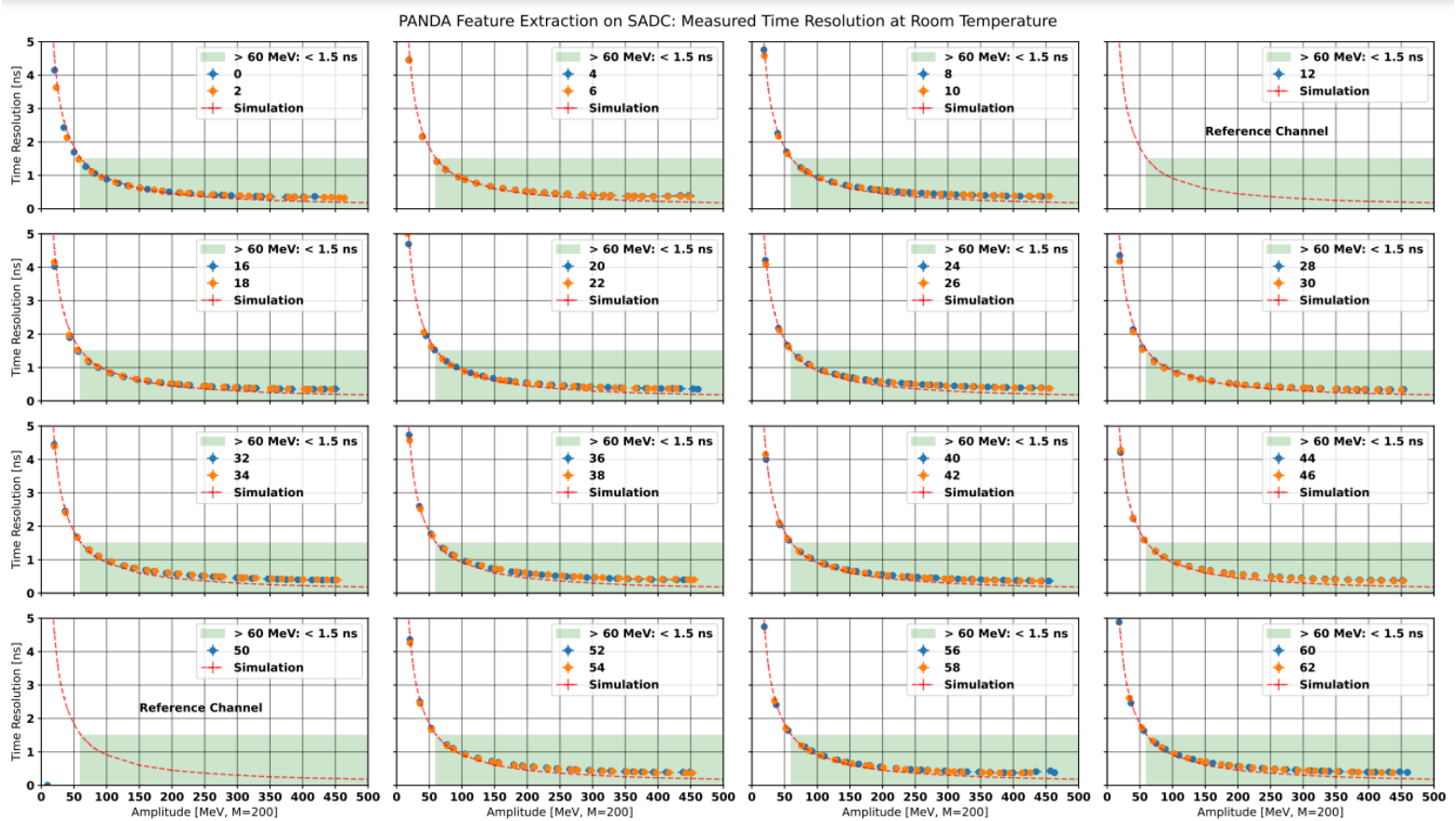
Summary and Outlook

- PANDA Phase-0 at MAMI
- PANDA backward calorimeter used to measure pion transition form factor
- Essential DAQ hardware is in Mainz or at the assembly process
  - Backplane tested ✓
  - Splitter tested ✓
  - CFD tested ✓
- Essential parts of TRB3 SC integration is done ✓
- Update of SADC Phase-0 firmware 2024
  - Improved time sorted hit packaging (free streaming: 310 kHz / channel) ✓
  - TRB interface via “Direct Line Messages” ✓
  - Preparation for triggered readout ✓
  - VLAN ready ✓
  - New internal (auto) request modus for traces, rates and config packages ✓
- Inter-Chip communication implementation is ongoing

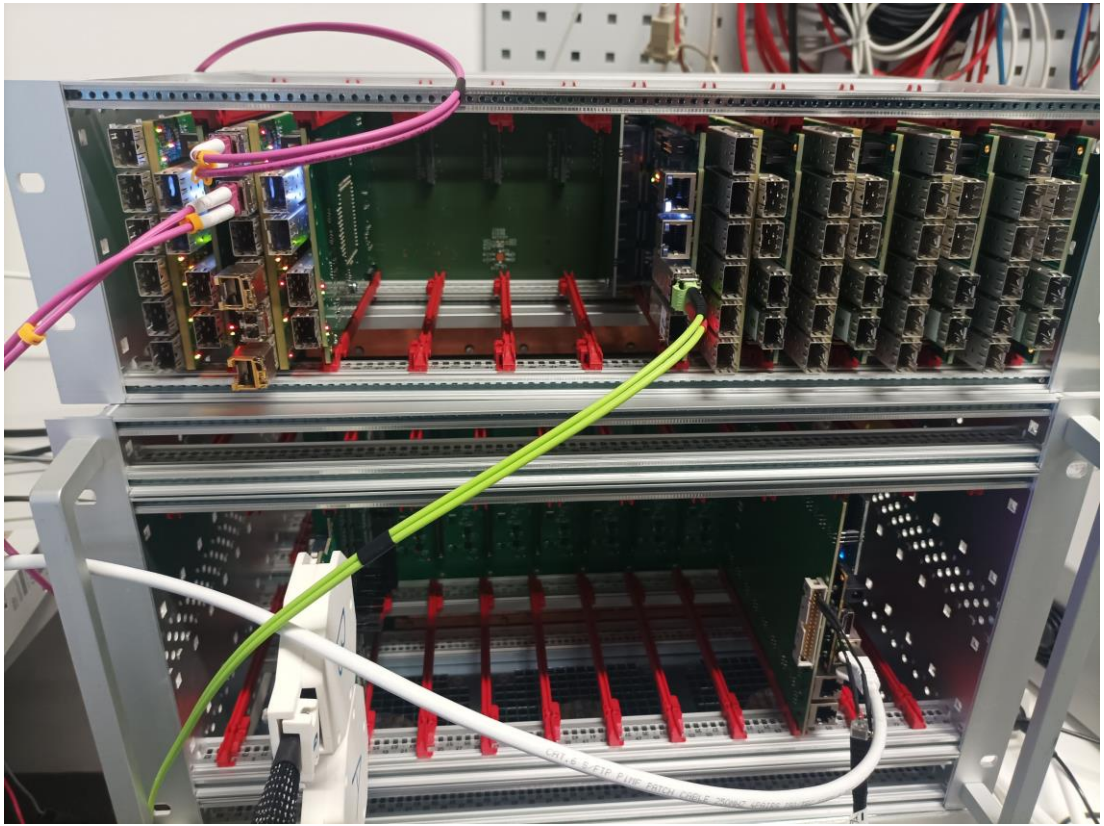
ADC Alignment and T0 Walk



Time Resolution at Room Temperature



Splitter, Backplane, CFD and TRB3 SC



Backplane, Controller and SADC