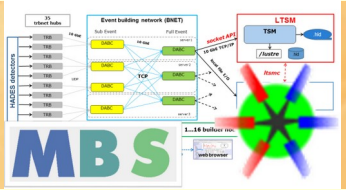



# MBS release V7.0 and recent developments

## *Super-FRS EC Meeting*

## *17-19 January 2024*

M. Reese, J. Adamczewski-Musch, N. Kurz, S. Linev, S. Minami, I. Rusanov
GSI/EEL

18.01.2024

# Introduction

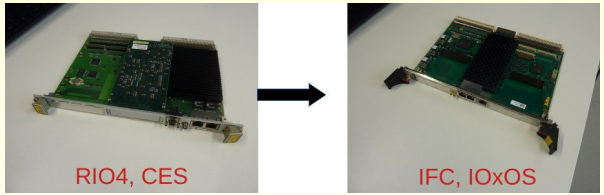
- Overview of MBS V7.0 release, highlight new features
  - New VME platforms: IFC and MVLC
  - White Rabbit timing receiver updates
  - New GSI mass storage interface FSQ
- Ongoing developments on PCIe platform
- About me:
  - PhD in Nuclear Spectroscopy (TU-Darmstadt / GSI)
  - 2016-2023 FAIR Control system: FAIR Timing Receiver (White Rabbit) Hardware and Software
  - Since September 2023: Member of GSI EEL, MBS knowledge transfer, MBS/DAQ support for experiments

# MBS history and status

- MBS is the general purpose DAQ system from GSI for 30 years
- Recent releases: V4.3 (2004), V5.1 (2010), V6.3 (2017)
- Mostly used readout systems:
  - VMEbus + modules (GSI and other)
  - PCIe + optical fibre (gosip) + GSI front-end boards
- See overview talk from 2019 by Nik Kurz (daq.gsi.de)
- New release V7.0 ready in January 2023 – Release notes
  - Installed at GSI MBS cluster at /mbs/v70
  - Default MBS version (mbslogin prod), V6.3 is still available (mbslogin old)

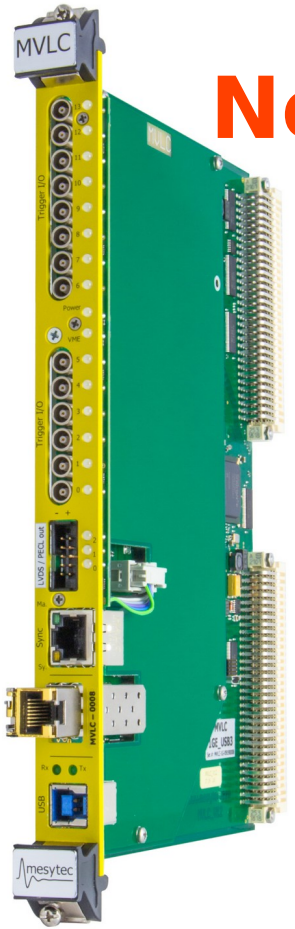
# New platform: IFC PPC linux for VME

- **CES/RIO4 processor discontinued  in 2021**
  (in use with >80 modules)!




- IOxOS IFC:
  - Kernel modules and drivers software for ”jethro” Linux
    - TRIVA trigger module
    - VETAR white rabbit timing receiver + etherbone libs
    - MBS pipe shared memory
  - Example readouts and tests for all known VME modules

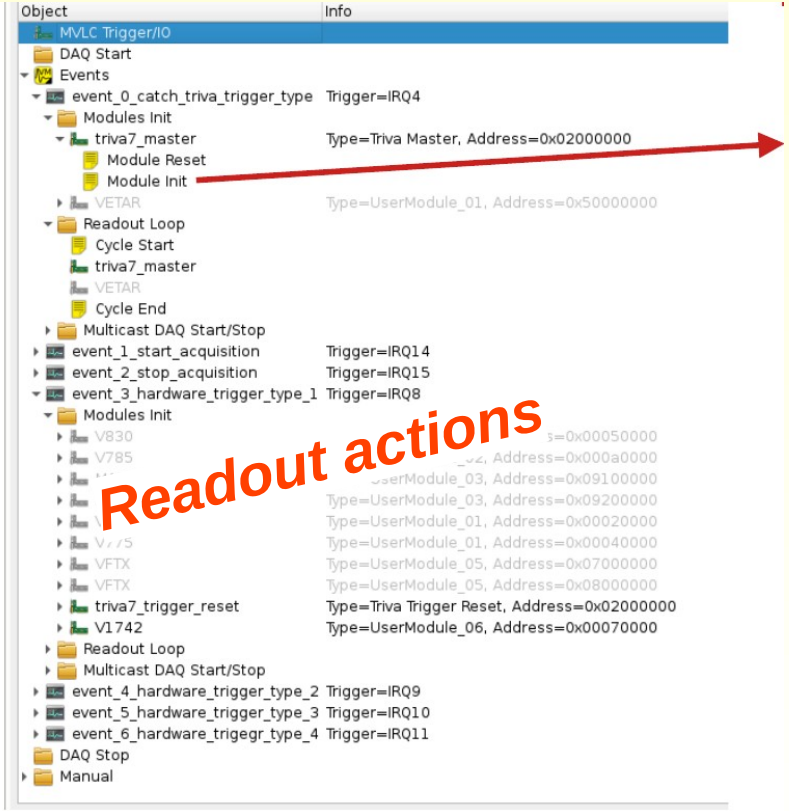
  (J. Adamczewski-Musch, N.Kurz)

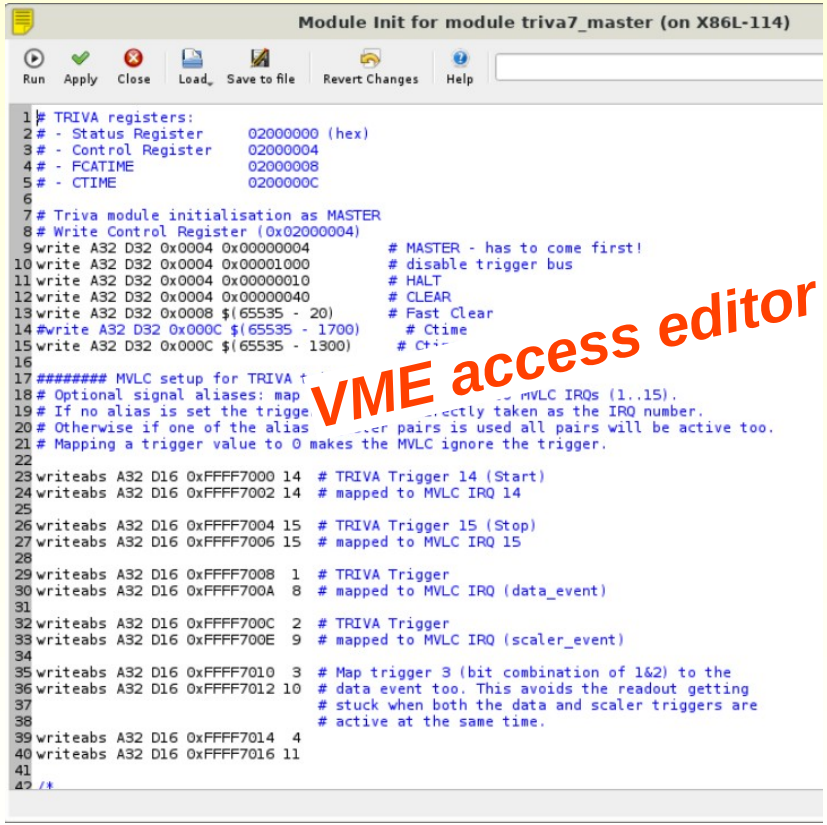



# New platform: mesytec MVLC

- MVLC hardware:
  - VME controller/sequencer with **low (no) latency**
  - Controlled via **USB 3** by any commodity MBS PC (X86L-*)
  - Reduced readout flexiblility compared to VME processor
- MVME software:
  - **prepare initialization and readout sequences**

# MVME software



# Integration of MVLC to MBS

- **Required developments:**
  - ***Control of TRIVA with MBS commands*** (set trigmod, start acquisition,…)
  - Different readout code for different TRIVA trigger types (mvme + mesytec upgrades!)
  - ***MVLC USB data is received by new MBS readout process*** (regular MBS subevents to pipe buffer)
  - Readout of ***VETAR White Rabbit timing receiver*** (produce MBS time stamp format)
  - Adjust readout for all types of VME modules used at GSI (mvme editor)
- **It is now possible to combine multiple branches with mvlc and non-mvlc readout!**

# Integration of MVLC to MBS

- All VME modules used at GSI proved to work
- Performance improvement of **factor 3** compared with RIO4 readout for a typical FRS setup
- No other hardware changes required when replacing RIO4 with MVLC
- **Was used in beam end of 2023**

# White Rabbit timing receivers

Use of **campus wide timestamp distribution via White Rabbit network** of the FAIR control system

- MBS accepted trigger is time stamped and integrated into event data (8 ns/1 ns resolution)
- Time stamp can be used for synchronization/time sorting of “free running” (aka streaming readout) branches
- Works with VME (also MVLC) and PCIe systems

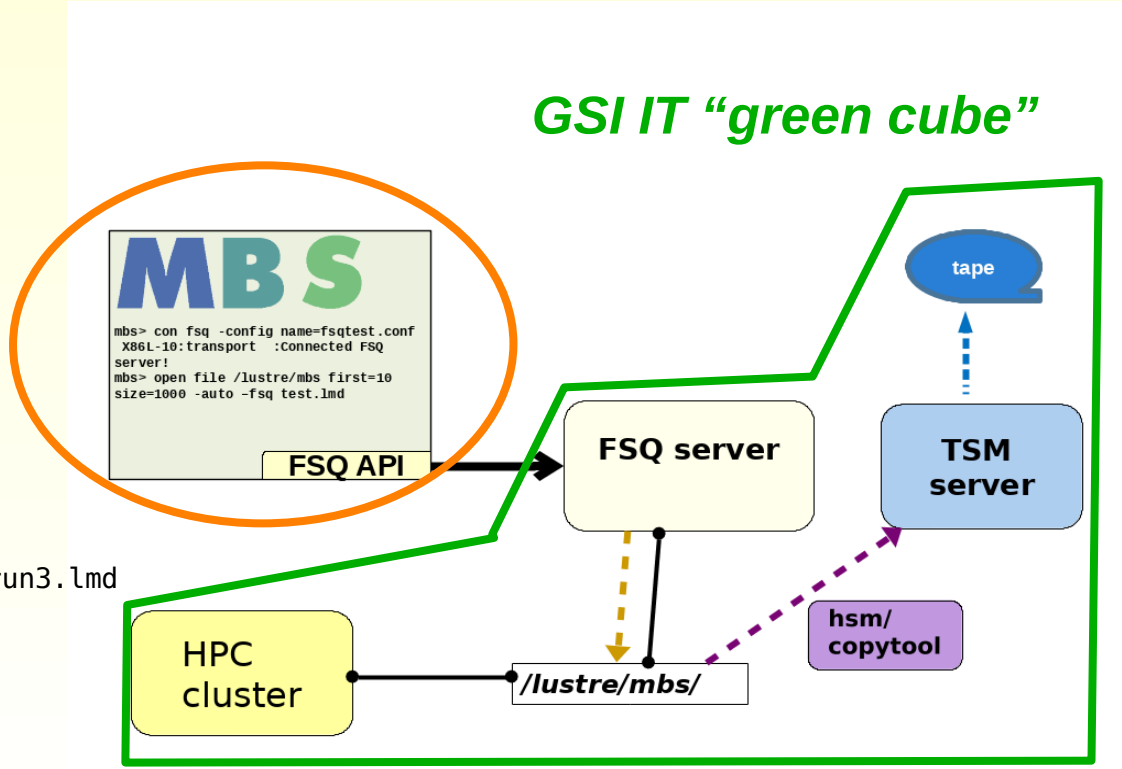

# New mass storage interface FSQ

- “**F**ile **S**torage **Q**ueue” (Thomas Stibor, GSI IT)
- **FSQ server** with access to */lustre* and TSM
- DAQ writes data with **lightweight FSQ protocol**, no IBM libs required
- Files are copied to **/lustre first, then archived to tape**
- Developed and **tested with HADES at beamtime FEB22**
- Will be **common GSI storage interface for experiments**

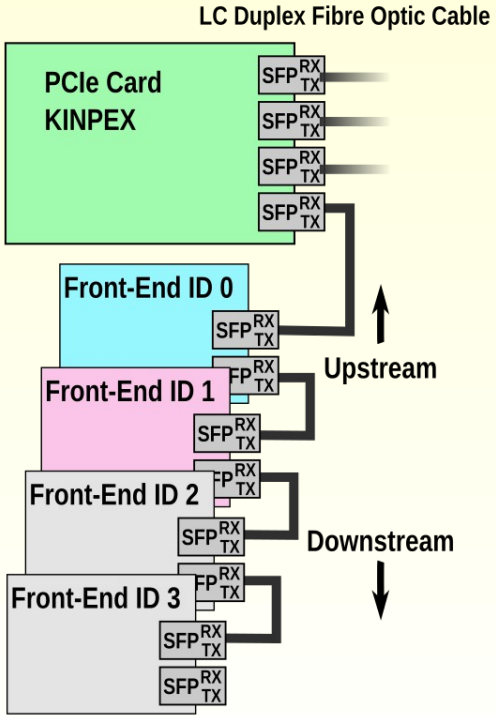
# MBS transport to FSQ server

*MBS event builder*

```
MBS> connect fsq -config myconfig.conf
MBS> open file -fsq -auto /lustre/exp/mar24/run3.lmd
```



# MBS PCIe platform: GOSIP




- Gigabit Optical Serial Interface Protocol
  - Data transfer protocol from FEEs to a PC.
  - 2Gbps ( PCIe 4x 2.5 Gbps )
- Address mode
  - Read/write access to 32-bit registers
  - Address space 24bits per FEE
- Block mode ( token passing)
  - Fast data transfer to PCIe interface
  - Double buffered block data transfer from all chained FEEs

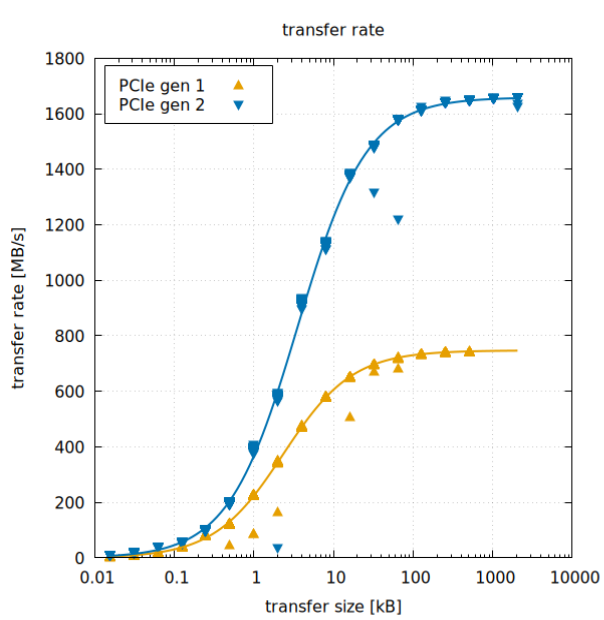
# Ongoing development: GOSIP

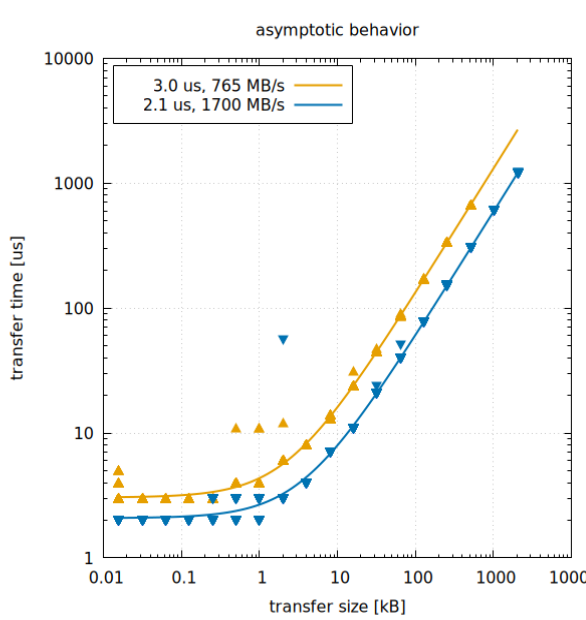
- **Upgrade to GOSIP with 5 Gbps line rate** (Kintex-7 FPGAs):
  - Clock TDCs (**CLKTDC128, KILOM, MPPC_ROB**)
  - 100 MSPS ADC (**FEBEX4**)
- **Upgrade to GOSIP with 2.5 Gbps line rate** (ECP3 FPGAs):
  - High Resolution TDC (**TAMEXs**)
  - 50 MSPS ADC (**FEBEX3**)
- **Allow dynamic change of line rate** for KINPEX PCIe card: 5 Gbps, 3.125 Gbps, 2.5 Gbps and 2 Gbps.

  (S. Minami)

# Ongoing development: PCIe

- KINPEX: PCIe gen 1 → gen 2
  **765 MB/s → 1700 MB/s**
- **64-bit DMA addresses** to relax MBS pipe layout constraints



# New optical connection between TRIXOR and EXPLODER

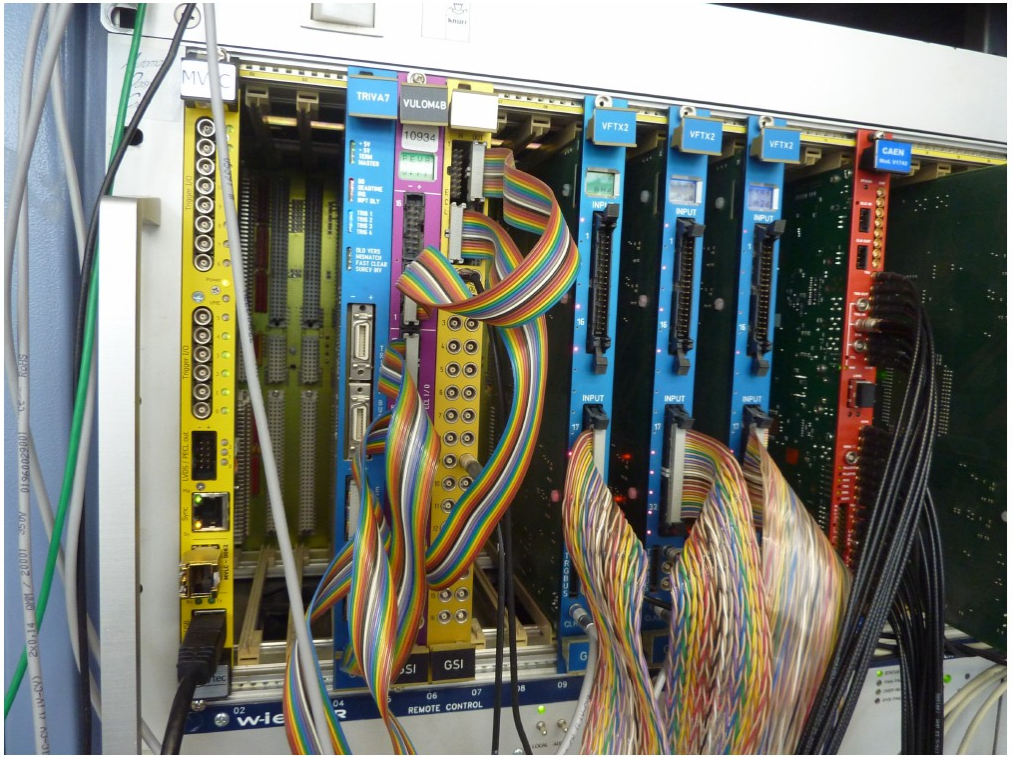
- TRIXORFP_FIBER2 replaces ribbon cable with optical link
- No copper between MBS PC and FE-crate
  → no ground loops

(I. Rusanov, H. Heggen)

# Summary

- MBS release V7.0 provides many developments since 2016
- PCIe X86L- hosts have been upgraded to Debian 11
- New VME platforms: IFC, MVLC
- White Rabbit trigger time latch unit supported
  (VETAR, PEXARIA)
- New GSI storage protocol FSQ integrated to MBS transport
  (for all MBS Linux platforms, even RIO4)
- Development is ongoing

# Thank you!


TRIVA7
VULOM4B
VFTX2
VFTX2
VFTX2
INPUT
INPUT
INPUT
GSI
REMOTE CONTROL