



Status of the new LMD DAQ

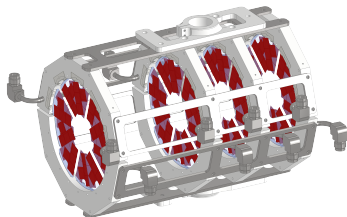
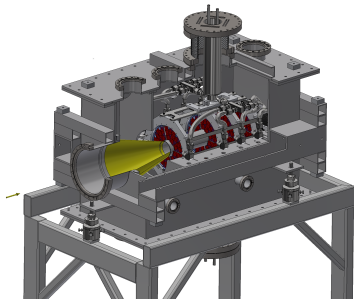
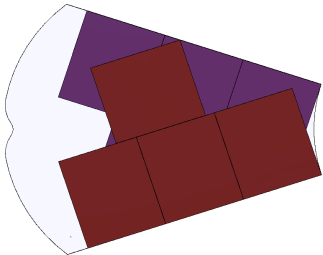
PANDA CM 23/2

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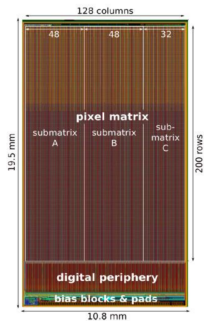
Luminosity Detector

- 320 MuPix chips
- Asynchronous LVDS readout
- Self triggered



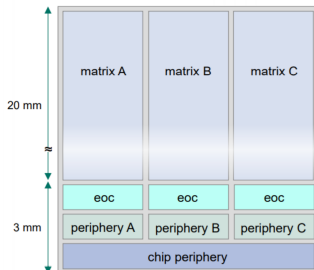
MuPix Sensors

MuPix8



- 128×200 pixels
- Physical size:
 $10.8 \times 19.5 \text{ mm}^2$
- Active area: $10.2 \times 16.2 \text{ mm}^2$

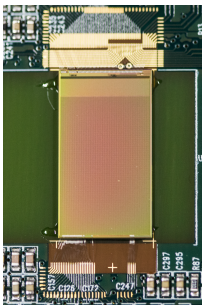
MuPix10/11



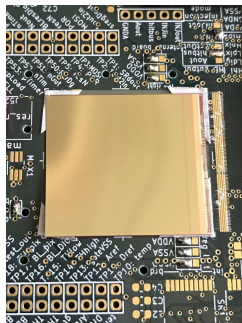
- 256×200 pixels
- Physical size:
 $20.7 \times 23.2 \text{ mm}^2$
- Active area: $20.0 \times 20.5 \text{ mm}^2$

MuPix Sensors

MuPix8



MuPix10/11



Signals from/to MuPix (LVDS):

- Reference Clock input
- 4 data links (each matrix + 1 multiplexed)
- Config interface
- Reset
- Injection

MuPix Timings

- Reference Clock determines timing on MuPix
- Timestamp counter runs with same frequency
(40 MHz ref clock \Rightarrow 25 ns timestamps)
(125 MHz ref clock \Rightarrow 8 ns timestamps)
- Serializer runs at $5 \cdot f_{ref}$ with DDR
(40 MHz ref clock \Rightarrow 400 Mbit/s data rate)
(125 MHz ref clock \Rightarrow 1.25 Gbit/s data rate)

MuPix Datagram

Continuous, asynchronous 8b10b encoded data stream from MuPix

K.28.5	K.28.5	K.28.5	K.28.5
K.28.5	K.28.5	K.28.5	K.28.5
K.28.5	K.28.5	K.28.5	K.28.5
K.28.0	Link ID	K.28.0	Link ID
Counter			TimestampToDet
hit 1			
hit 2			
⋮			
hit n			
K.28.5	K.28.5	K.28.5	K.28.5

} if data available

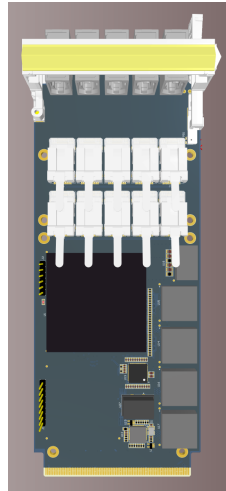
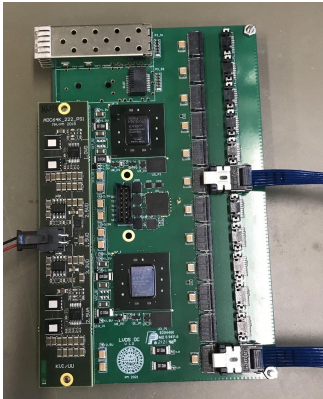
} if no data available

Per readout cycle max 1 hit per column (max $n_{\text{cols}(M)}$ hits per frame)
K.28.5 “comma” word has unique bit sequence

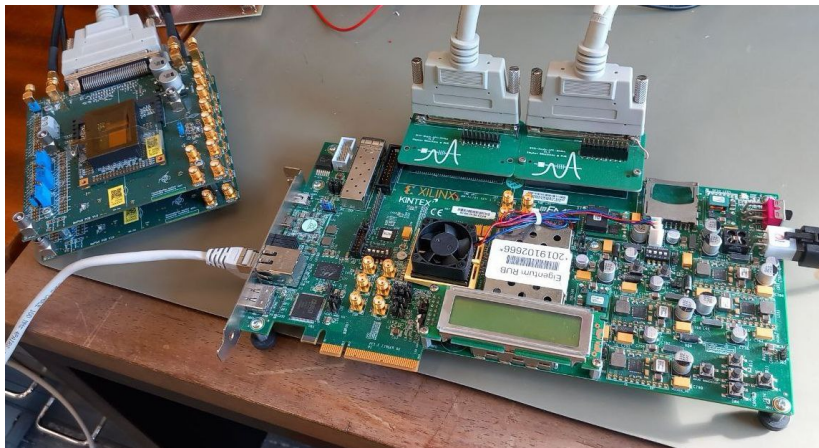
Readout Hardware for final DAQ

Data Concentrator

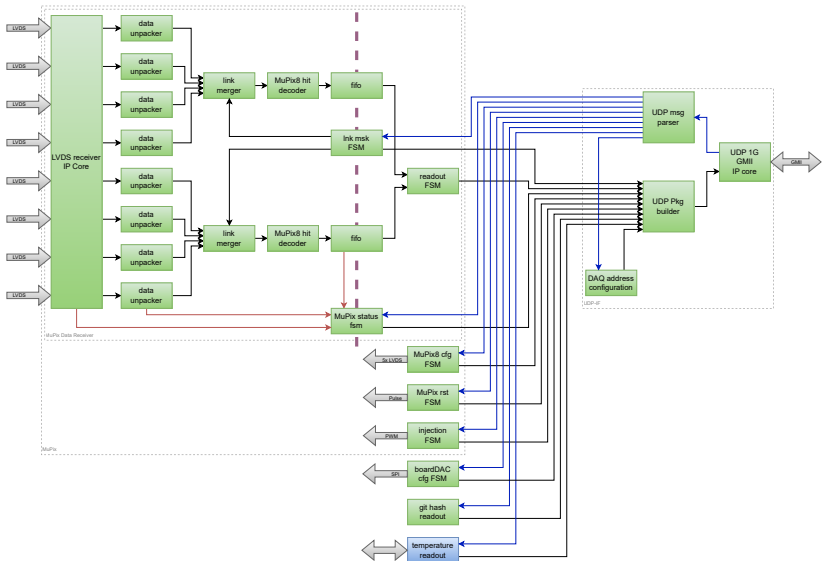
LVDS DC



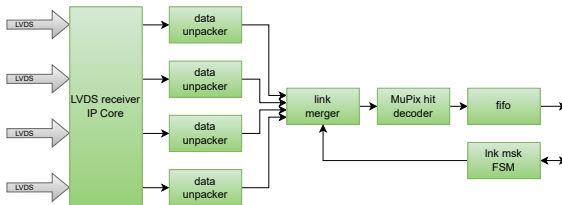
Current Test Setup



Block Diagram of Kintex 7 Firmware



MuPix Data Receiver



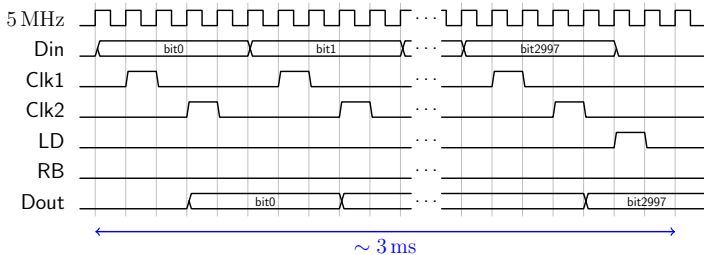
For each MuPix:

- 4 LVDS receiver channels (based on XAPP523)
- Extracting hits from datagram
- Combining streams from (4 channels & link mask) into single stream
- Convert grey counter to binary and RAM pixel address to physical
- Buffer data and cross clock domains

MuPix Configuration

MuPix8:

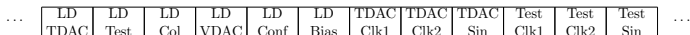
- Configuration realized with 2998 bit deep shift register
- Data needs to be send for each row ($200 \cdot 2998 \text{ bit} \sim 600 \text{ kbit}$)
- Order of bits not “human readable” (e.g. $R[2,0,1,3,4,5]$)
- Different length of individual registers (1, 2, 3, 4, 6 and 10 bit)
- ⇒ Build bitstream on PC rather then on FPGA
- On FPGA: State machine to pipe out bits and control signals (CLK1, CLK2, LD)



MuPix Configuration

MuPix10:

- 32 bit wide SPI interface
- Configuration registers split into blocks
- “Old” control signals encoded in dataword



need to transmit each “bit” 5 times (in total ~ 82 kbit)

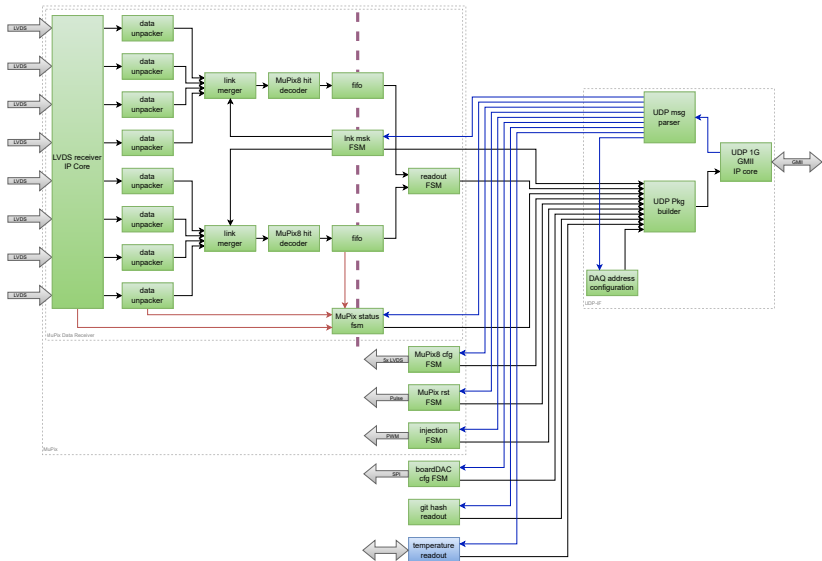
- Different length of individual registers/blocks
- ⇒ Build bitstream for each block on PC
- State machine handles CLK1/CLK2/LD signals

MuPix11:

- Either SPI Interface like MuPix10 or “Mu3e” interface



Block Diagram of Kintex 7 Firmware



Readout FSM and Pkg Builder

- MuPix Readout State Machine implemented as Round-Robin Arbiter
- If Fifo of MuPix n is not empty, request to transmit data, else $n = n + 1$

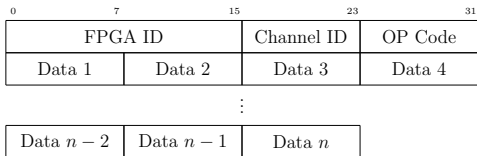
- (UDP) Pkg Builder implemented as Round-Robin Arbiter
- Check if FSM requests to transmit data
- Send corresponding header to UDP Core
- Forward data transmission from FSM to UDP core
- Readout FSM has highest priority

Data transferred between state machines via “framed” AXI-Stream

```
type axis_t is record
  valid : std_logic;           -- data is valid
  data  : std_logic_vector(X downto 0); -- data byte
  last  : std_logic;         -- last byte indicator
end record axis_t;
```

native interface of UDP/IP ($X = 7$) and Aurora8b10b cores
($X = 15||31$)

(UDP) Payload data



Number n of payload data bytes depend on op code

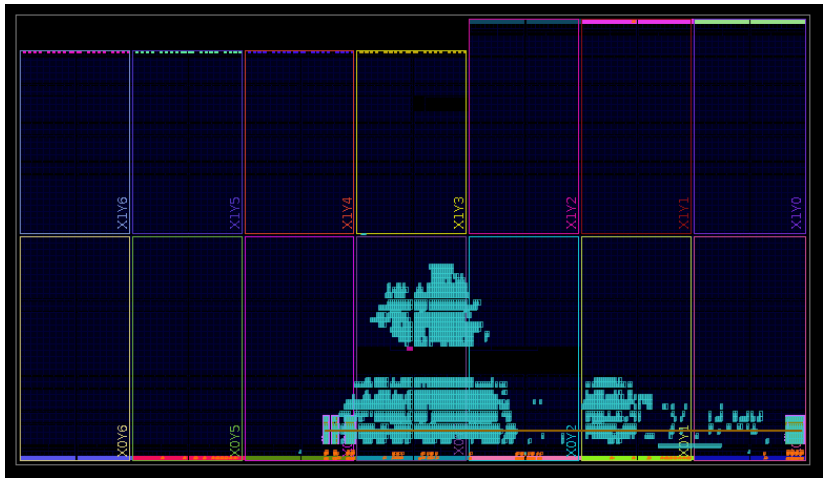
- For MuPix8 configuration $n = 375$
- For link mask $n = 1$
- For readout data: $4 \leq n \leq 4096$

No length information in header

- Already encoded in UDP header
- Framed AXI-Stream interface: Read until last byte flag is asserted

FPGA ID 0xffff used for broadcasts

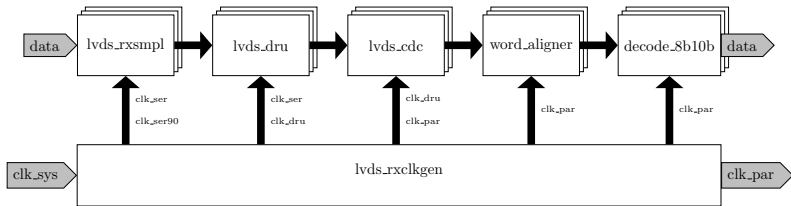
Implemented Design on KC705



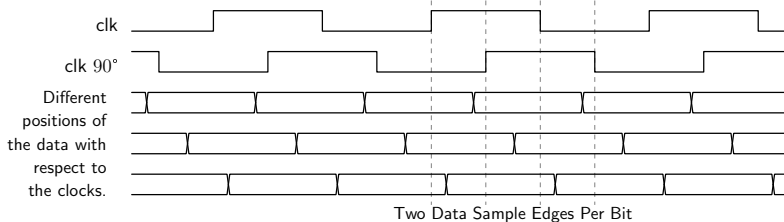
Summary

- Kintex7 Firmware ready
- VHDL-Code uploaded to PANDA gitlab:
<https://panda-repo.gsi.de/PandaDAQ/firmware/lmd-lvds-dc>
<https://panda-repo.gsi.de/PandaDAQ/ip-cores/lvds-receiver>
<https://panda-repo.gsi.de/PandaDAQ/ip-cores/udp-with-dhcp>
- Beamtime:
 - ▶ Test Kintex7 based DAQ
 - ▶ Test first Mupix8 sensor bonded to Alu-FlexCable

LVDS Receiver IP Core

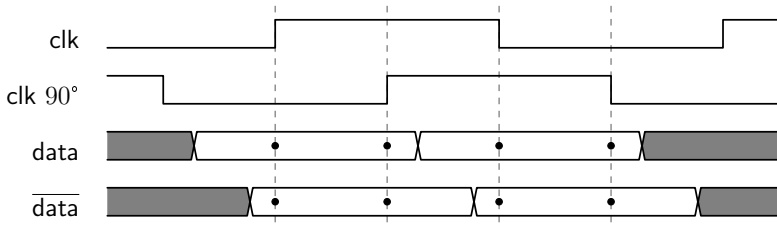
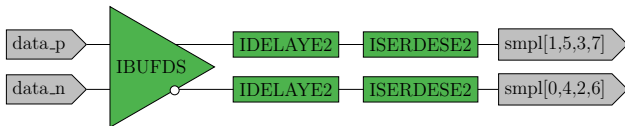


Sampling of asynchronous data bases on XAPP523:



LVDS Receiver IP Core - Data Sampling

Use LVDS input buffer with differential output
Delay negative signal by 45°



UDP IP Core

