Hardware Acceleration
LAB

# PANDA DAQ Summary 2022

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Panda Collaboration Meeting 22/3

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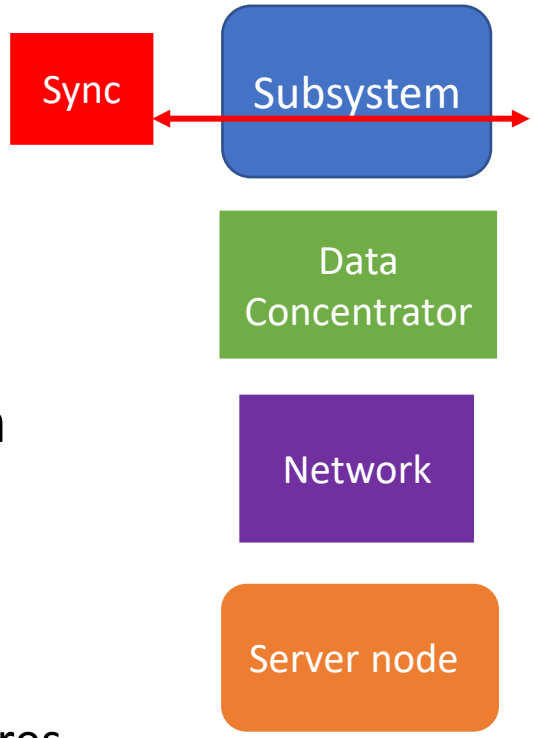
# DAQ-0

- Actual subsystem setup
  - A single segment or more complex setup
- Synchronization
- Actual Data Concentrator hardware platform
- Framework for:
  - Subsystem integration with the DAQ
  - Development of subsystem preprocessing on DC
  - Development of control and monitoring procedures
  - DAQ performance and scalability evaluation
  - Available for beamtests of subsystems

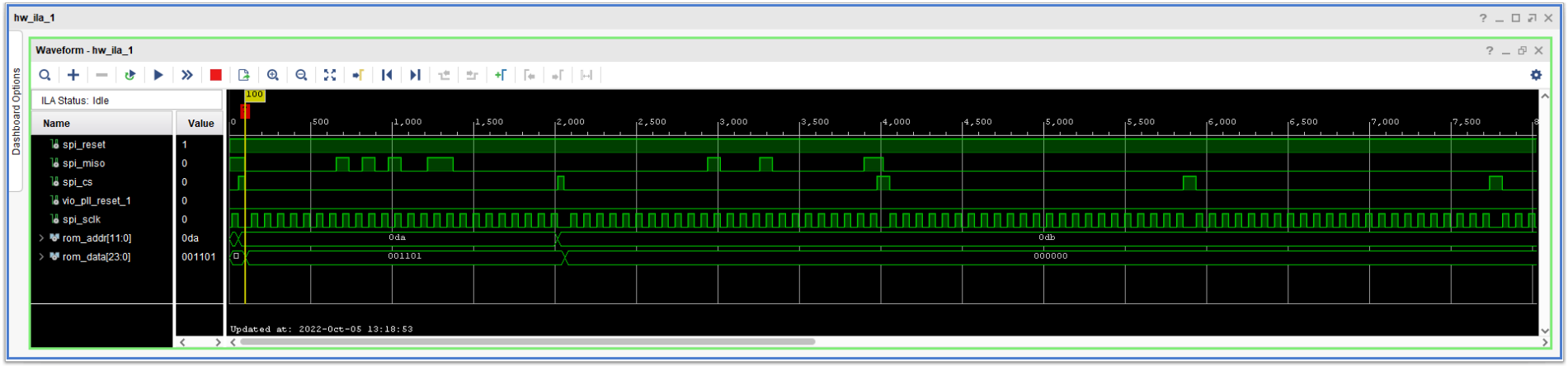


# Panda DC -Status

1. 2 boards were produced. One board is missing 0.9V The problem is faulty PCB. For furter tests of this board power this needs to be provided from an extarnal source. To be tested in future.
2. The second board has passed the power tests and is under tests.
3. The MMC works – used mostly for power control
4. The PLL works – used for providing system clocks
5. 8/11 GTH and 4/8 GTY transceivers work in internal loopback tests. Non-working channels be investigated. The problem is related to internal PLL (not locking).
6. Power consumption of GTH and GTY transceivers agrees with simulations.
7. Split fibers for fiber loopback tests will be delivered in 4 weeks

# PLL controller

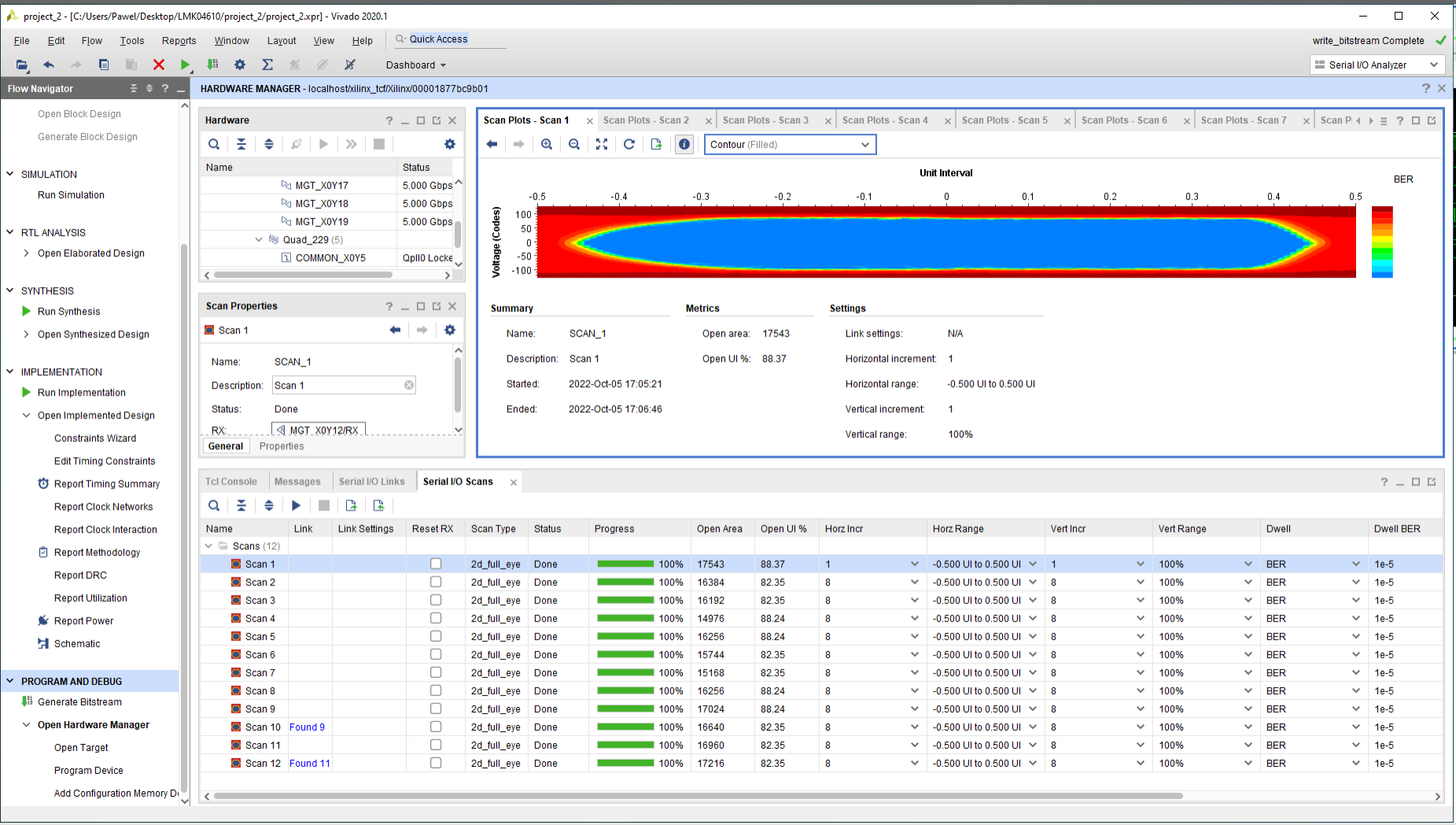
- Clock supplier to Gigabit Transceivers
- SPI controlled device
- HDL SPI controller and configuration file (P. Marciniewski & M. Caselle)
  - Configuration file generated by TI tools and verified on an evaluation board
  - Proper reset sequence
  - PLL registers configuration
  - Device enable by a register at the end of the sequence



# Gigabit Transceivers

- Evaluation of MGT channels performance
  - Automatic IBERT tester component
  - First channels positively tested (P. Marciniewski)
    - 5 Gbps with 100 MHz reference clock
    - Loopback at PMA level
    - Optical components required for external loopback
- Aurora Sync
  - High-level protocol for data transport, AXI transfer, synchronization pulses
  - Implemented on GTP (Artix), GTX (Kintex, ZynqU+), GTH (KintexU+)
  - To be adapter to GTY

# Transceiver loopback tests



# DAQ-0 setup

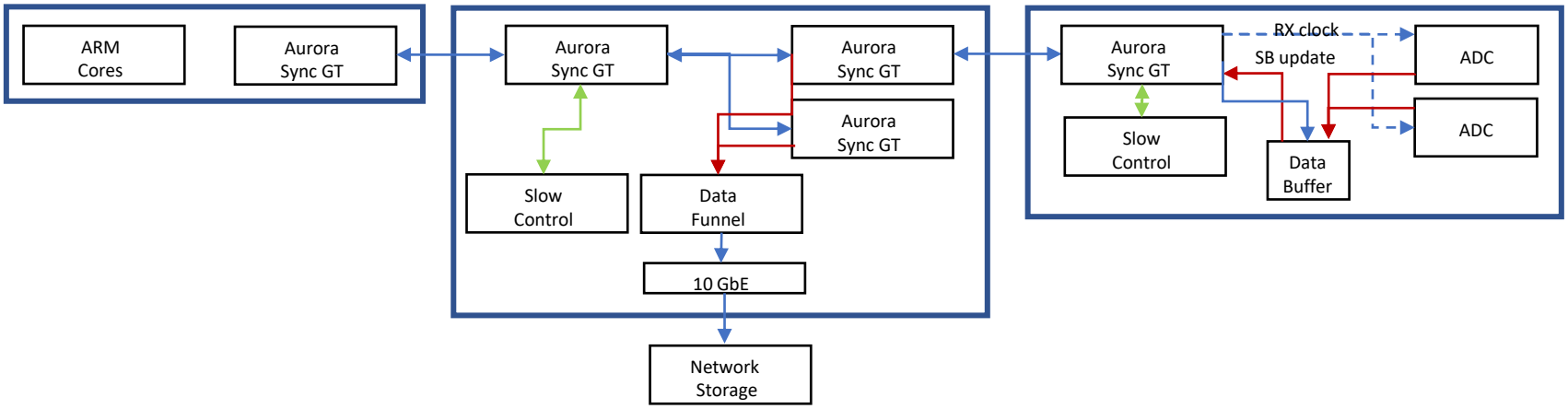
**Controller Board**
- Common clock source
- Synchronous transc.
- Linux + master AXI

L. Linzen works on dev. board

**Data Concentrator**
- Common clock recovery
- Common clock forwarding
- Endp. data aggregation
- Ethernet output
- AXI forwarding and local

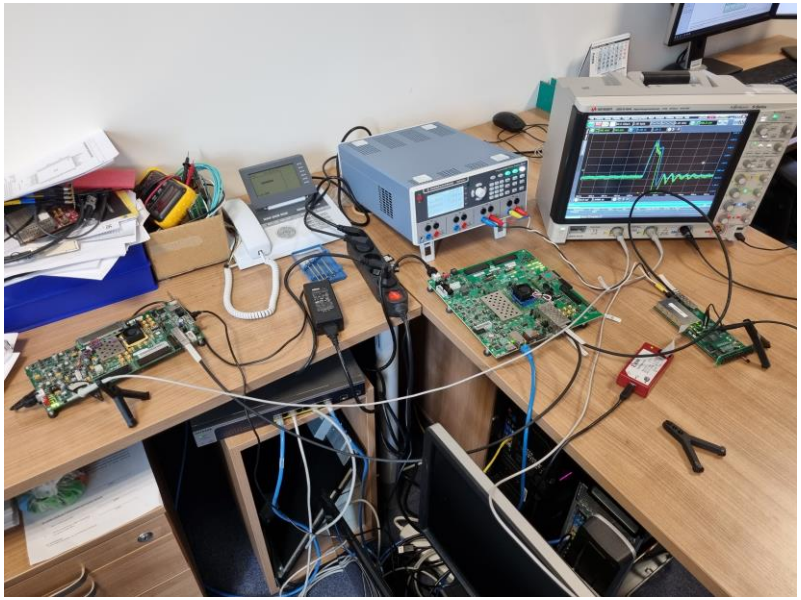
**Endpoint**
- Common clock recovery
- Data buffering
- Slow control

GTX endpoint tested on dev. board



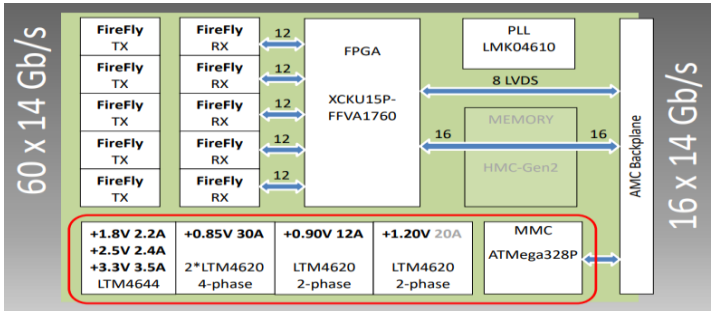
# Summary

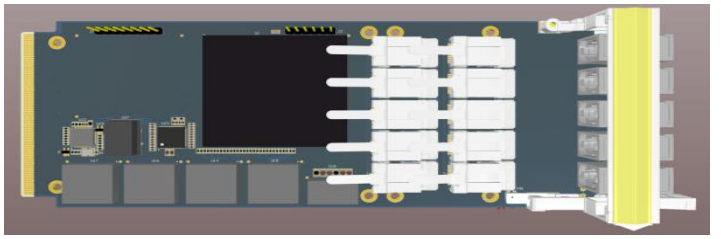
- Basic DC functionality operational
- Proceed to evaluate communication infrastructure
  - Testing setup ready in Cracow
  - 1 DC unit to share
- EMC SADC as Endpoint
  - Tests of Aurora on GTX
  - Integration with ADC readout



# Data Concentrator

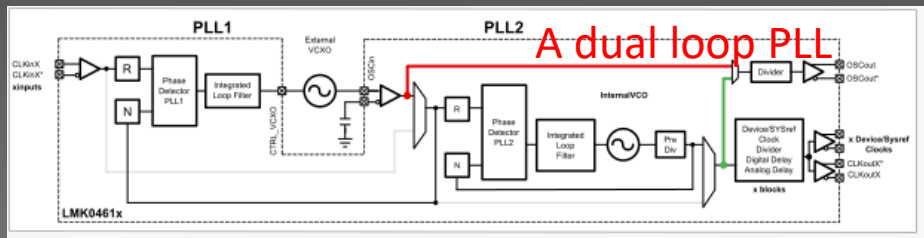
- 2 units produced and equipped
  - 1 u. operational, 1 u. power supply under investigation
- FPGA programmable
- Module Management Controller operational
- Initial firmware (P. Marciniewski & M. Caselle)
  - PLL HDL controller – clock source for MGTs
  - Evaluation of MGT channels
- FPGAs purchased for more units
- Firefly transceivers sets for 2 units
  - Purchase required for additional 2 units
  - Additional cabling for loopbacks and bundle splits ordered



P. Marciniewski

# PANDA DC

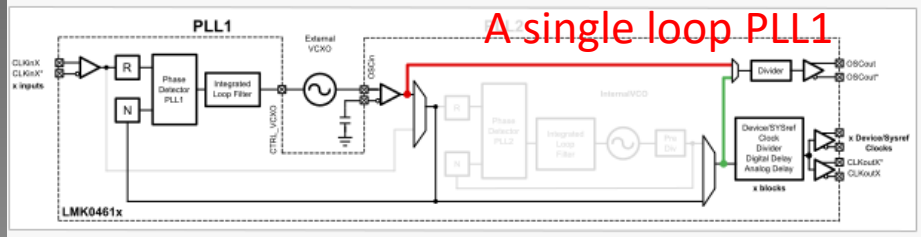



Dual Loop

Normal
Dual Loop
OscOut = OscIn

Dual Loop

Normal
Dual Loop
OscOut = PLL2 Output

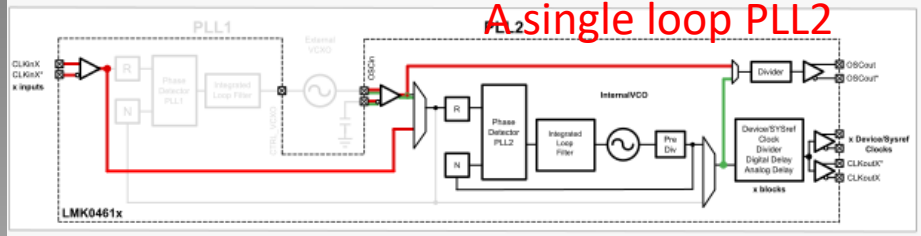



Single Loop PLL1

PLL1
Single Loop
OscOut = OscIn

Single Loop PLL1

PLL1
Single Loop
OscOut = PLL1 Output

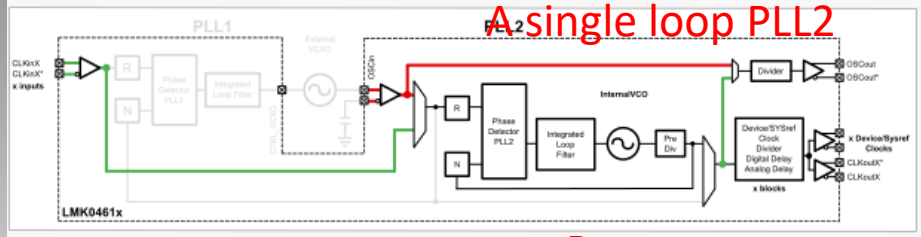



Single Loop PLL2

PLL2
Single Loop
Ref=CLKINx
OscOut = OscIn

Single Loop PLL2

PLL2
Single Loop
Ref=OscIn
OscOut = PLL Output

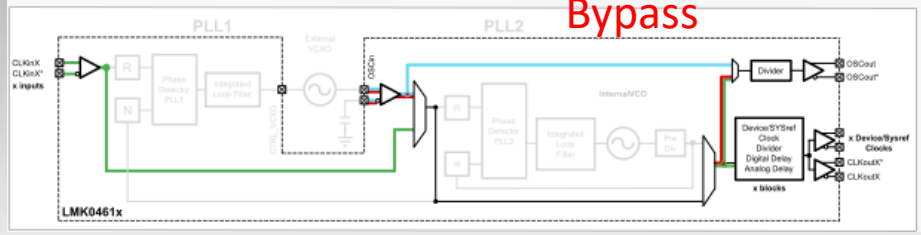



Single Loop PLL2

PLL2
Single Loop
Ref=OscIn
OscOut = OscIn

Single Loop PLL2

PLL2
Single Loop
Ref=CLKINx
OscOut = PLL Output



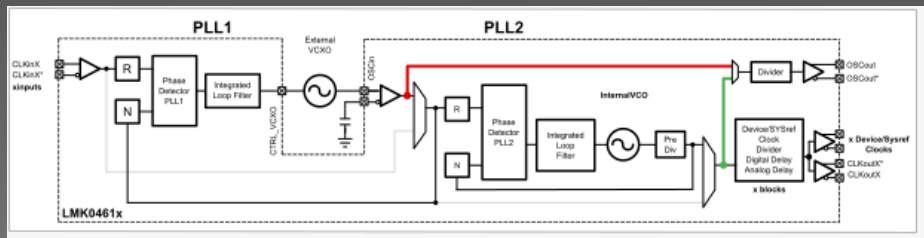

Bypass 2A

Mode 2A
Bypass
OSCIn- > CLKoutX
OscOut = PLL bypass

Bypass 1

Mode 1
Bypass
CLKINx- > CLKoutX
OscOut = PLL bypass

# Status of the DAQ electronics for the EMC
# PANDA DC

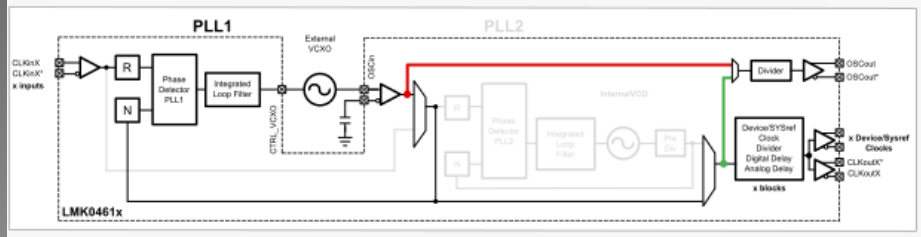



Dual Loop

Normal
Dual Loop
OscOut = OscIn

Dual Loop

Normal
Dual Loop
OscOut = PLL2 Output

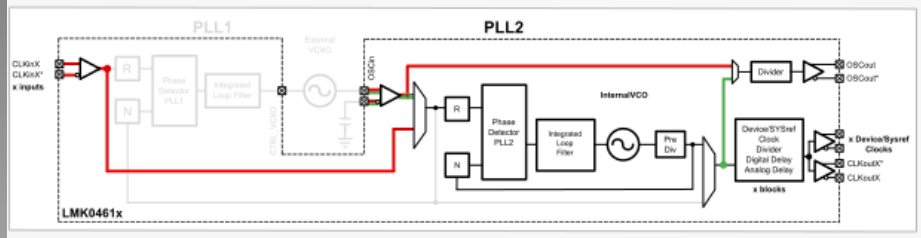



Single Loop PLL1

PLL1
Single Loop
OscOut = OscIn

Single Loop PLL1

PLL1
Single Loop
OscOut = PLL1 Output

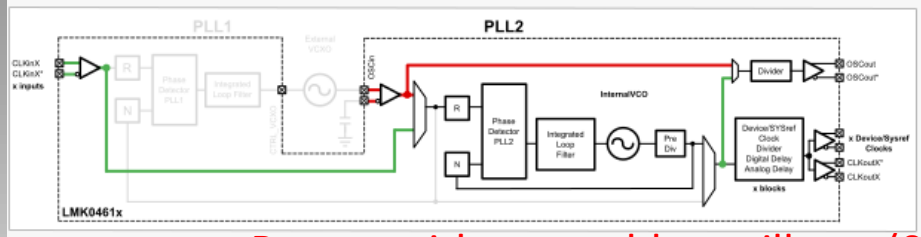



Single Loop PLL2

PLL2
Single Loop
Ref=CLKINx
OscOut = OscIn

Single Loop PLL2

PLL2
Single Loop
Ref=OscIn
OscOut = PLL Output



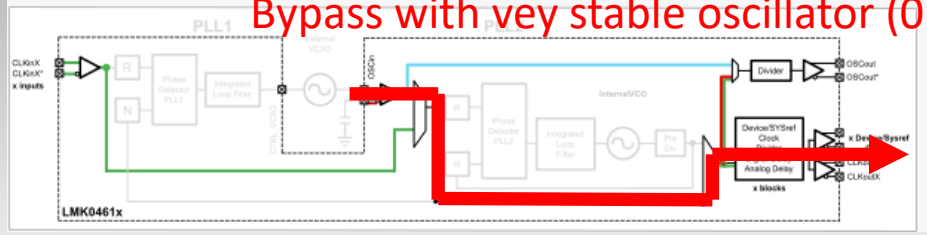

Single Loop PLL2

PLL2
Single Loop
Ref=OscIn
OscOut = OscIn

Single Loop PLL2

PLL2
Single Loop
Ref=CLKINx
OscOut = PLL Output

Bypass with vey stable oscillator (0.2 ppm)



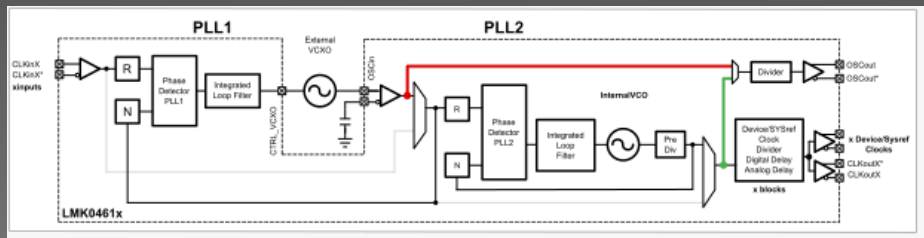

Bypass 2A

Mode 2A
Bypass
OSCIn- > CLKoutX
OscOut = PLL bypass

Bypass 1

Mode 1
Bypass
CLKINx- > CLKoutX
OscOut = PLL bypass

# Status of the DAQ electronics for the EMC
# PANDA DC

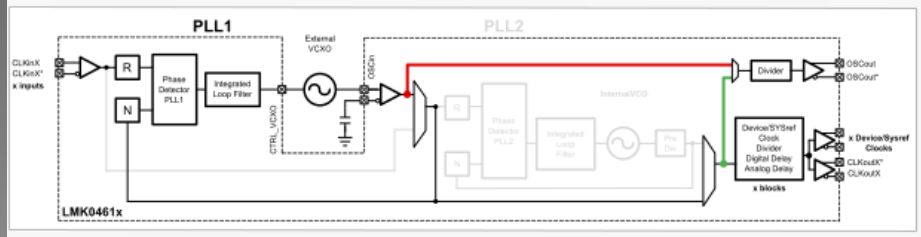



Dual Loop

Normal
Dual Loop
OscOut = OscIn

Dual Loop

Normal
Dual Loop
OscOut = PLL2 Output

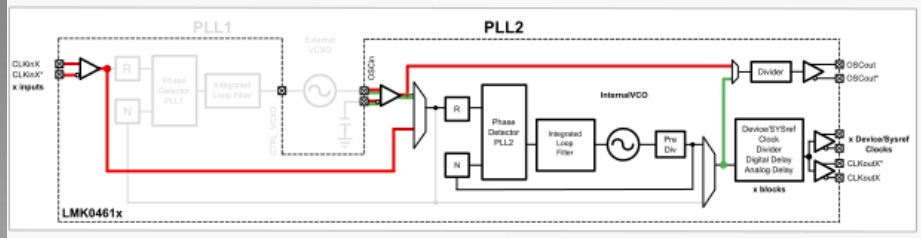



Single Loop PLL1

PLL1
Single Loop
OscOut = OscIn

Single Loop PLL1

PLL1
Single Loop
OscOut = PLL1 Output

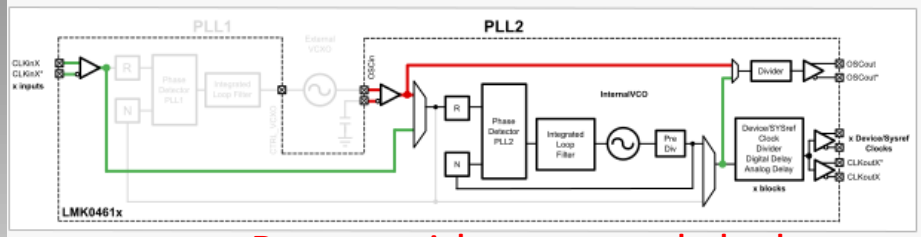



Single Loop PLL2

PLL2
Single Loop
Ref=CLKINx
OscOut = OscIn

Single Loop PLL2

PLL2
Single Loop
Ref=OscIn
OscOut = PLL Output



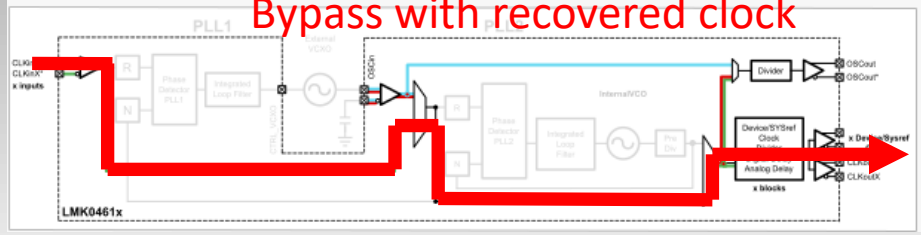

Single Loop PLL2

PLL2
Single Loop
Ref=OscIn
OscOut = OscIn

Single Loop PLL2

PLL2
Single Loop
Ref=CLKINx
OscOut = PLL Output

Bypass with recovered clock



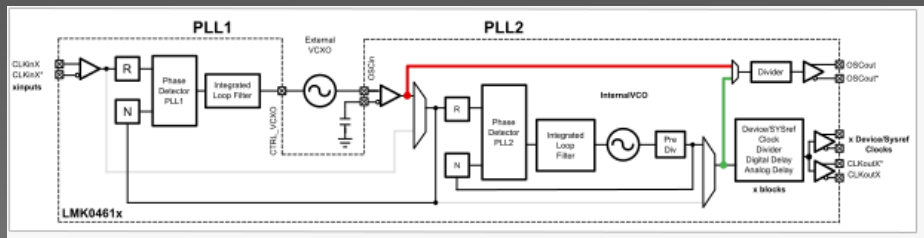

Bypass 2A

Mode 2A
Bypass
OSCIn- > CLKoutX
OscOut = PLL bypass

Bypass 1

Mode 1
Bypass
CLKINx- > CLKoutX
OscOut = PLL bypass

# Status of the DAQ electronics for the EMC
# PANDA DC

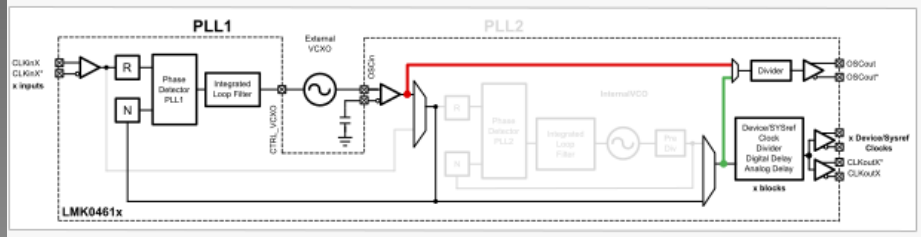



Dual Loop

Normal
Dual Loop
OscOut = OscIn

Dual Loop

Normal
Dual Loop
OscOut = PLL2 Output

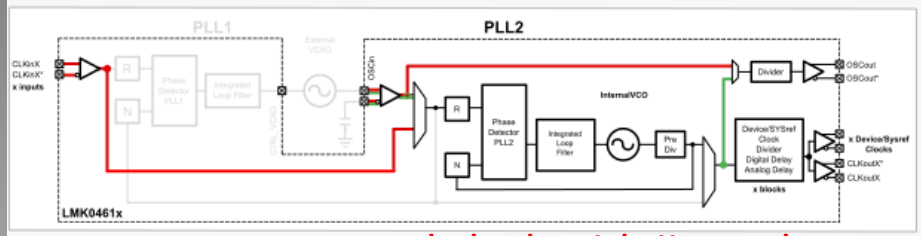



Single Loop PLL1

PLL1
Single Loop
OscOut = OscIn

Single Loop PLL1

PLL1
Single Loop
OscOut = PLL1 Output



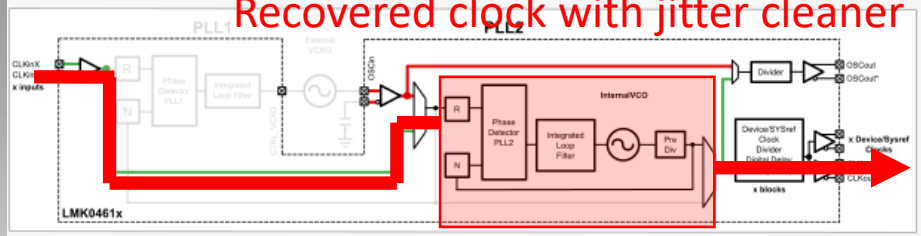

Single Loop PLL2

PLL2
Single Loop
Ref=CLKINx
OscOut = OscIn

Single Loop PLL2

PLL2
Single Loop
Ref=OscIn
OscOut = PLL Output

Recovered clock with jitter cleaner

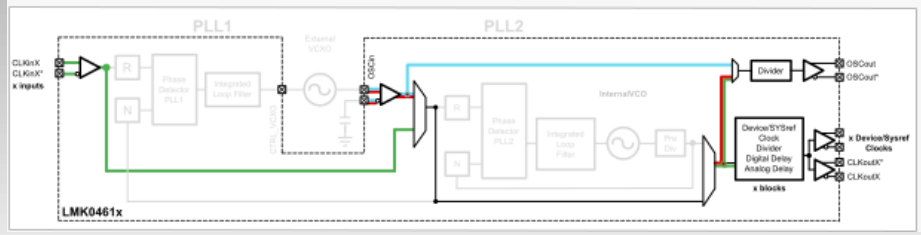



Single Loop PLL2

PLL2
Single Loop
Ref=OscIn
OscOut = OscIn

Single Loop PLL2

PLL2
Single Loop
Ref=CLKINx
OscOut = PLL Output




Bypass 2A

Mode 2A
Bypass
OSCIn- > CLKoutX
OscOut = PLL bypass

Bypass 1

Mode 1
Bypass
CLKINx- > CLKoutX
OscOut = PLL bypass