



Hardware Acceleration
LAB



PANDA DAQ Summary 2022

Grzegorz Korcyl

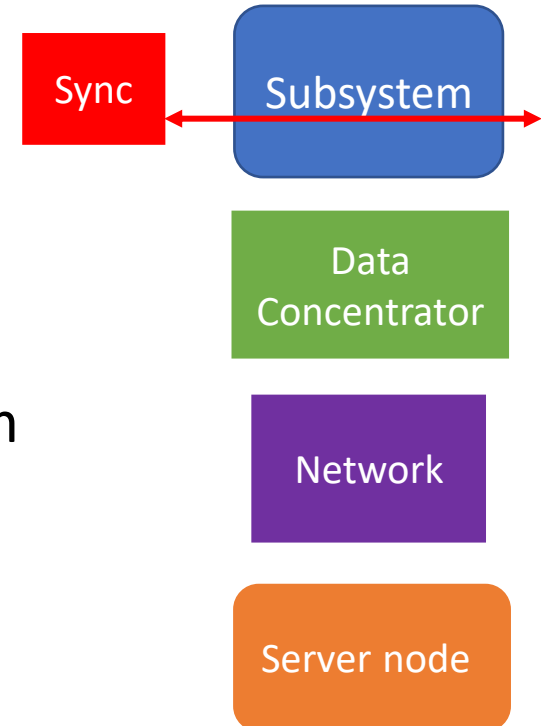
Panda Collaboration Meeting 22/3

10.10.2022



DAQ-0

- Actual subsystem setup
 - A single segment or more complex setup
- Synchronization
- Actual Data Concentrator hardware platform
- Framework for:
 - Subsystem integration with the DAQ
 - Development of subsystem preprocessing on DC
 - Development of control and monitoring procedures
 - DAQ performance and scalability evaluation
 - Available for beamtests of subsystems



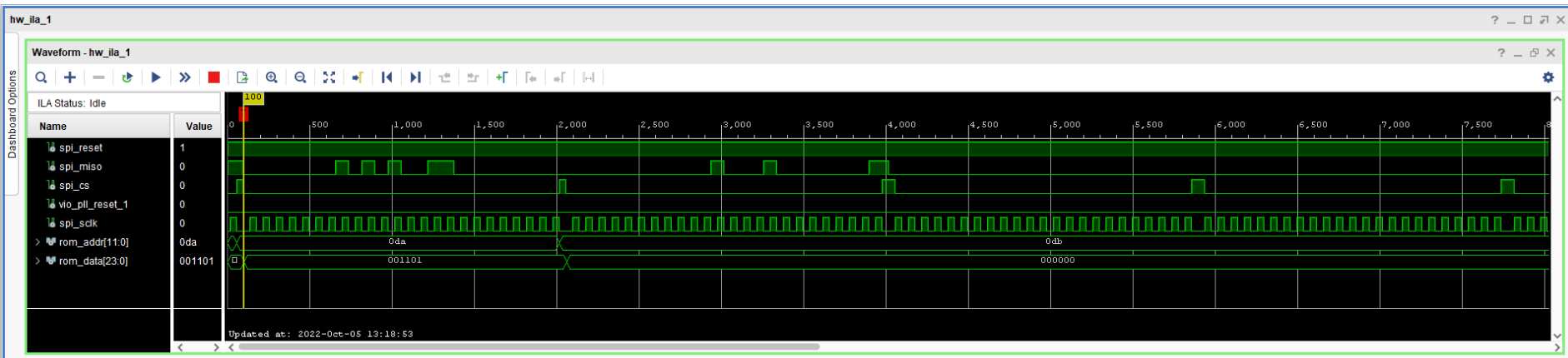


Panda DC -Status

1. 2 boards were produced. One board is missing 0.9V The problem is faulty PCB. For further tests of this board power this needs to be provided from an external source. To be tested in future.
2. The second board has passed the power tests and is under tests.
3. The MMC works – used mostly for power control
4. The PLL works – used for providing system clocks
5. 8/11 GTH and 4/8 GTY transceivers work in internal loopback tests. Non-working channels be investigated. The problem is related to internal PLL (not locking).
6. Power consumption of GTH and GTY transceivers agrees with simulations.
7. Split fibers for fiber loopback tests will be delivered in 4 weeks

PLL controller

- Clock supplier to Gigabit Transceivers
- SPI controlled device
- HDL SPI controller and configuration file (P. Marciniewski & M. Caselle)
 - Configuration file generated by TI tools and verified on an evaluation board
 - Proper reset sequence
 - PLL registers configuration
 - Device enable by a register at the end of the sequence



Gigabit Transceivers

- Evaluation of MGT channels performance
 - Automatic IBERT tester component
 - First channels positively tested (P. Marciniewski)
 - 5 Gbps with 100 MHz reference clock
 - Loopback at PMA level
 - Optical components required for external loopback
- Aurora Sync
 - High-level protocol for data transport, AXI transfer, synchronization pulses
 - Implemented on GTP (Artix), GTX (Kintex, ZynqU+), GTH (KintexU+)
 - To be adapter to GTY

Transceiver loopback tests

project_2 - [C:/Users/Pawel/Desktop/LMK04610/project_2/project_2.xpr] - Vivado 2020.1

File Edit Flow Tools Reports Window Layout View Help Quick Access

write_bitstream Complete

Serial I/O Analyzer

Flow Navigator

HARDWARE MANAGER - localhost:xlinox_tcf/xlinox/00001877bc9b01

Hardware

Name	Status
MGT_X0Y17	5.000 Gbps
MGT_X0Y18	5.000 Gbps
MGT_X0Y19	5.000 Gbps
Quad_229 (5)	
COMMON_X0Y5	QpII0 Lock

Scan Properties

Scan 1

Name: SCAN_1

Description: Scan 1

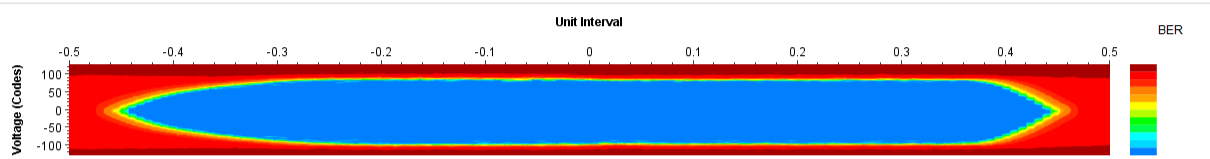
Status: Done

RX: MGT_X0Y12/RX

General Properties

Scan Plots - Scan 1

Contour (Filled)



Unit Interval

Summary

Summary	Metrics	Settings
Name: SCAN_1	Open area: 17543	Link settings: N/A
Description: Scan 1	Open UI %: 88.37	Horizontal increment: 1
Started: 2022-Oct-05 17:05:21		Horizontal range: -0.500 UI to 0.500 UI
Ended: 2022-Oct-05 17:06:46		Vertical increment: 1
		Vertical range: 100%

Tcl Console Messages Serial I/O Links Serial I/O Scans

Name	Link	Link Settings	Reset RX	Scan Type	Status	Progress	Open Area	Open UI %	Horz Incr	Horz Range	Vert Incr	Vert Range	Dwell	Dwell BER
Scans (12)														
Scan 1			<input type="checkbox"/>	2d_full_eye	Done	100%	17543	88.37	1	-0.500 UI to 0.500 UI	1	100%	BER	1e-5
Scan 2			<input type="checkbox"/>	2d_full_eye	Done	100%	16384	82.35	8	-0.500 UI to 0.500 UI	8	100%	BER	1e-5
Scan 3			<input type="checkbox"/>	2d_full_eye	Done	100%	16192	82.35	8	-0.500 UI to 0.500 UI	8	100%	BER	1e-5
Scan 4			<input type="checkbox"/>	2d_full_eye	Done	100%	14976	88.24	8	-0.500 UI to 0.500 UI	8	100%	BER	1e-5
Scan 5			<input type="checkbox"/>	2d_full_eye	Done	100%	16256	88.24	8	-0.500 UI to 0.500 UI	8	100%	BER	1e-5
Scan 6			<input type="checkbox"/>	2d_full_eye	Done	100%	15744	82.35	8	-0.500 UI to 0.500 UI	8	100%	BER	1e-5
Scan 7			<input type="checkbox"/>	2d_full_eye	Done	100%	15168	82.35	8	-0.500 UI to 0.500 UI	8	100%	BER	1e-5
Scan 8			<input type="checkbox"/>	2d_full_eye	Done	100%	16256	88.24	8	-0.500 UI to 0.500 UI	8	100%	BER	1e-5
Scan 9			<input type="checkbox"/>	2d_full_eye	Done	100%	17024	88.24	8	-0.500 UI to 0.500 UI	8	100%	BER	1e-5
Scan 10	Found 9		<input type="checkbox"/>	2d_full_eye	Done	100%	16640	82.35	8	-0.500 UI to 0.500 UI	8	100%	BER	1e-5
Scan 11			<input type="checkbox"/>	2d_full_eye	Done	100%	16960	82.35	8	-0.500 UI to 0.500 UI	8	100%	BER	1e-5
Scan 12	Found 11		<input type="checkbox"/>	2d_full_eye	Done	100%	17216	82.35	8	-0.500 UI to 0.500 UI	8	100%	BER	1e-5

DAQ-0 setup

Controller Board

- Common clock source
- Synchronous transc.
- Linux + master AXI

L. Linzen works on dev. board

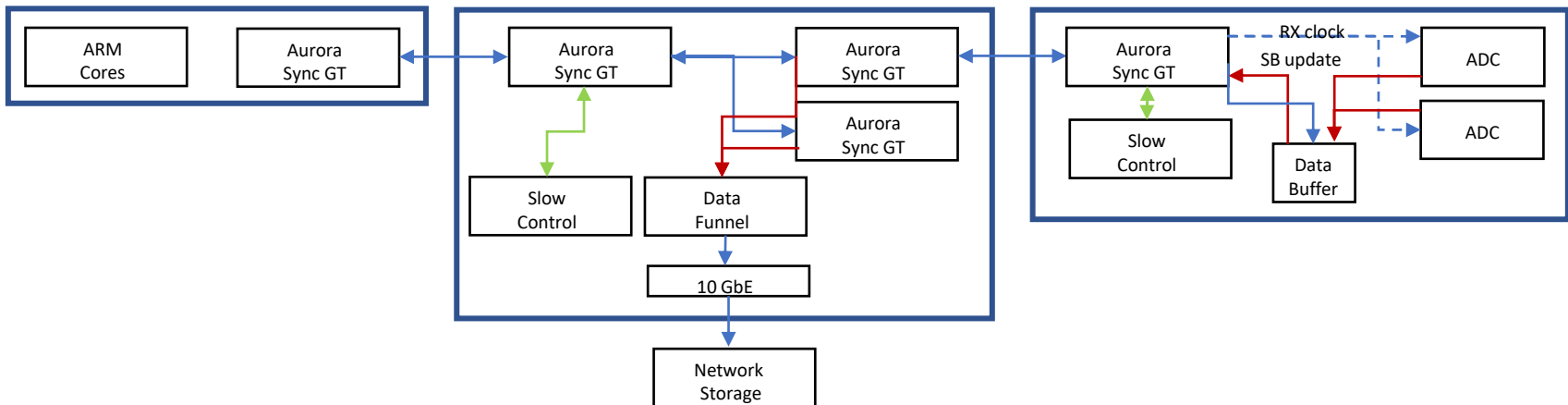
Data Concentrator

- Common clock recovery
- Common clock forwarding
- Endp. data aggregation
- Ethernet output
- AXI forwarding and local

Endpoint

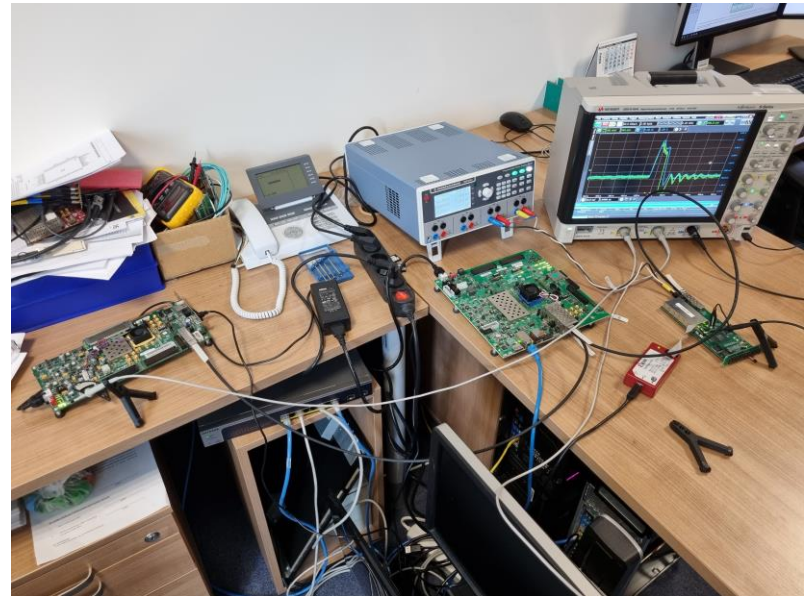
- Common clock recovery
- Data buffering
- Slow control

GTX endpoint tested on dev. board



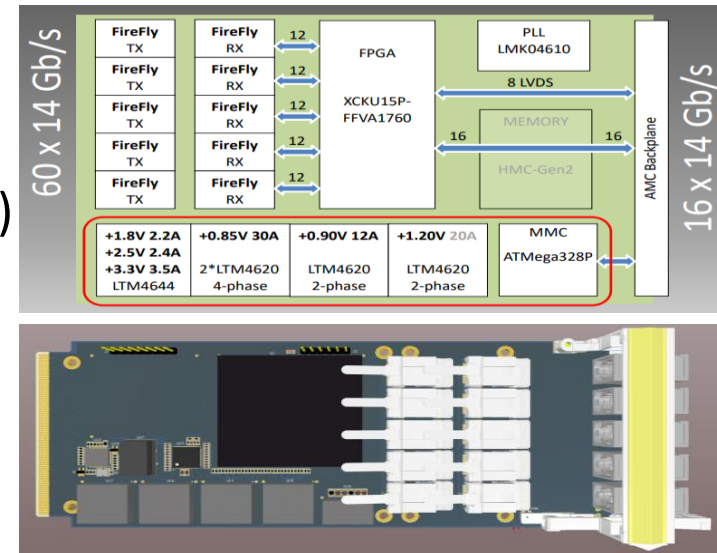
Summary

- Basic DC functionality operational
- Proceed to evaluate communication infrastructure
 - Testing setup ready in Cracow
 - 1 DC unit to share
- EMC SADC as Endpoint
 - Tests of Aurora on GTX
 - Integration with ADC readout



Data Concentrator

- 2 units produced and equipped
 - 1 u. operational, 1 u. power supply under investigation
- FPGA programmable
- Module Management Controller operational
- Initial firmware (P. Marciniewski & M. Caselle)
 - PLL HDL controller – clock source for MGTs
 - Evaluation of MGT channels
- FPGAs purchased for more units
- Firefly transceivers sets for 2 units
 - Purchase required for additional 2 units
 - Additional cabling for loopbacks and bundle splits ordered



P. Marciniewski

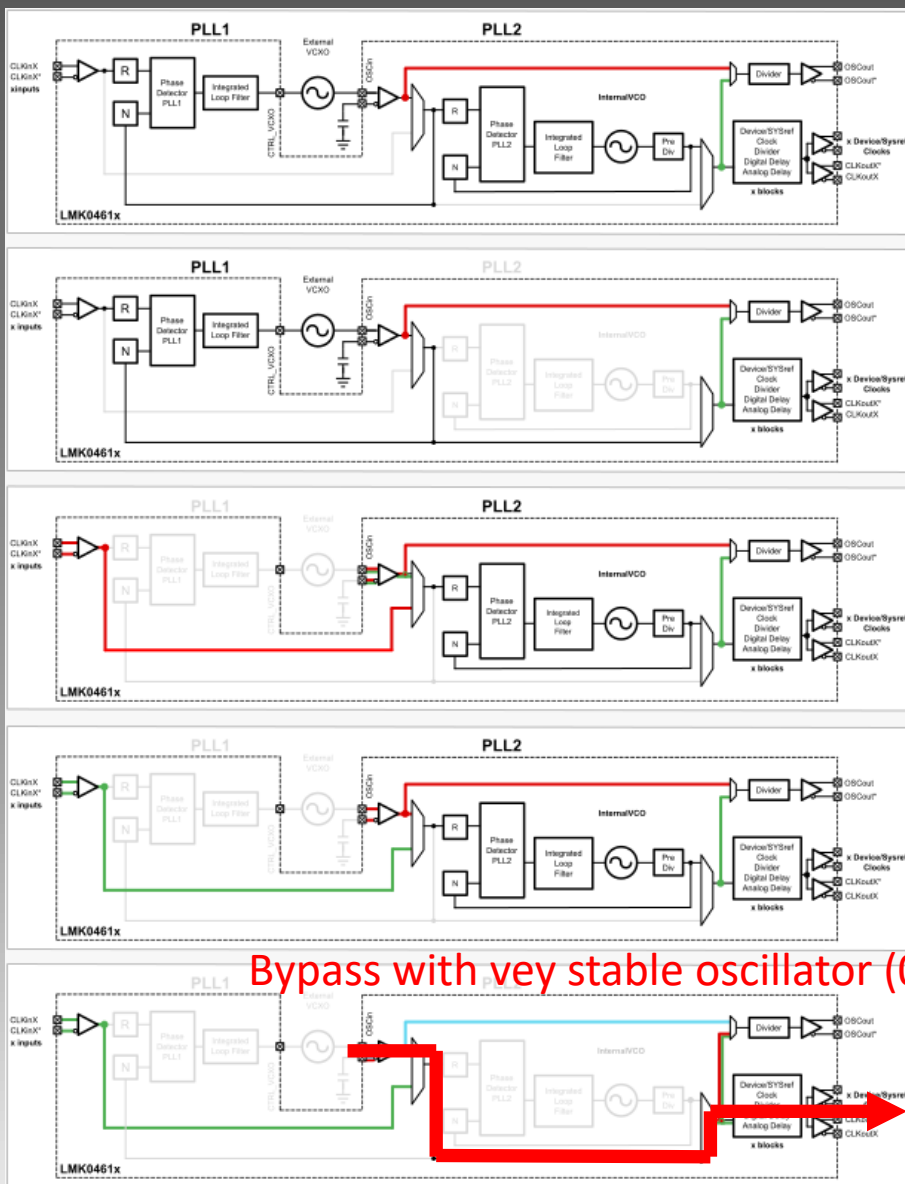


PANDA DC

<p style="color: red; text-align: center;">A dual loop PLL</p>	<p style="background-color: #e67e22; color: white; padding: 5px; text-align: center;">Dual Loop</p> <p>Normal Dual Loop OscOut = OscIn</p>	<p style="background-color: #27ae60; color: white; padding: 5px; text-align: center;">Dual Loop</p> <p>Normal Dual Loop OscOut = PLL2 Output</p>
<p style="color: red; text-align: center;">A single loop PLL1</p>	<p style="background-color: #e67e22; color: white; padding: 5px; text-align: center;">Single Loop PLL1</p> <p>PLL1 Single Loop OscOut = OscIn</p>	<p style="background-color: #27ae60; color: white; padding: 5px; text-align: center;">Single Loop PLL1</p> <p>PLL1 Single Loop OscOut = PLL1 Output</p>
<p style="color: red; text-align: center;">A single loop PLL2</p>	<p style="background-color: #e67e22; color: white; padding: 5px; text-align: center;">Single Loop PLL2</p> <p>PLL2 Single Loop Ref=CLKINx OscOut = OscIn</p>	<p style="background-color: #27ae60; color: white; padding: 5px; text-align: center;">Single Loop PLL2</p> <p>PLL2 Single Loop Ref=OscIn OscOut = PLL Output</p>
<p style="color: green; text-align: center;">A single loop PLL2</p>	<p style="background-color: #e67e22; color: white; padding: 5px; text-align: center;">Single Loop PLL2</p> <p>PLL2 Single Loop Ref=OscIn OscOut = OscIn</p>	<p style="background-color: #27ae60; color: white; padding: 5px; text-align: center;">Single Loop PLL2</p> <p>PLL2 Single Loop Ref=CLKINx OscOut = PLL Output</p>
<p style="color: green; text-align: center;">Bypass</p>	<p style="background-color: #e67e22; color: white; padding: 5px; text-align: center;">Bypass 2A</p> <p>Mode 2A Bypass OscIn -> CLKOutX OscOut = PLL bypass</p>	<p style="background-color: #27ae60; color: white; padding: 5px; text-align: center;">Bypass 1</p> <p>Mode 1 Bypass CLKINx -> CLKOutX OscOut = PLL bypass</p>



PANDA DC



Dual Loop

Dual Loop

Normal Dual Loop
OscOut = OscIn

Normal Dual Loop
OscOut = PLL2 Output

Single Loop PLL1

Single Loop PLL1

PLL1 Single Loop
OscOut = OscIn

PLL1 Single Loop
OscOut = PLL1 Output

Single Loop PLL2

Single Loop PLL2

PLL2 Single Loop
Ref=CLKINx
OscOut = OscIn

PLL2 Single Loop
Ref=OscIn
OscOut = PLL Output

Single Loop PLL2

Single Loop PLL2

PLL2 Single Loop
Ref=OscIn
OscOut = OscIn

PLL2 Single Loop
Ref=CLKINx
OscOut = PLL Output

Bypass with very stable oscillator (0.2 ppm)

Bypass 2A

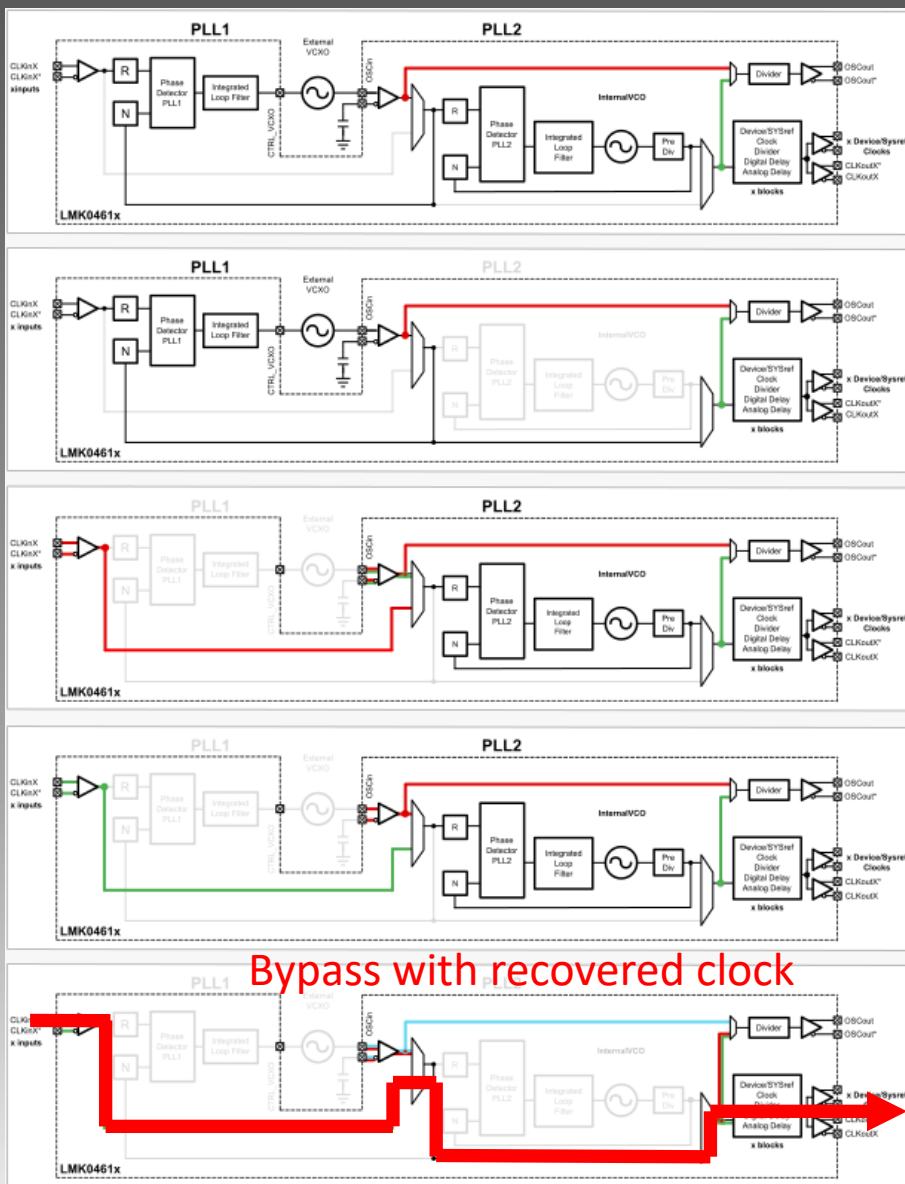
Bypass 1

Mode 2A Bypass
OscIn -> CLKOutX
OscOut = PLL bypass

Mode 1 Bypass
CLKINx -> CLKOutX
OscOut = PLL bypass



Status of the DAQ electronics for the EMC PANDA DC



Dual Loop

Normal Dual Loop
OscOut = OscIn

Dual Loop

Normal Dual Loop
OscOut = PLL2 Output

Single Loop PLL1

PLL1 Single Loop
OscOut = OscIn

Single Loop PLL1

PLL1 Single Loop
OscOut = PLL1 Output

Single Loop PLL2

PLL2 Single Loop
Ref=CLKINx
OscOut = OscIn

Single Loop PLL2

PLL2 Single Loop
Ref=OSCIn
OscOut = PLL Output

Single Loop PLL2

PLL2 Single Loop
Ref=OSCIn
OscOut = OscIn

Single Loop PLL2

PLL2 Single Loop
Ref=CLKINx
OscOut = PLL Output

Bypass with recovered clock

Bypass 2A

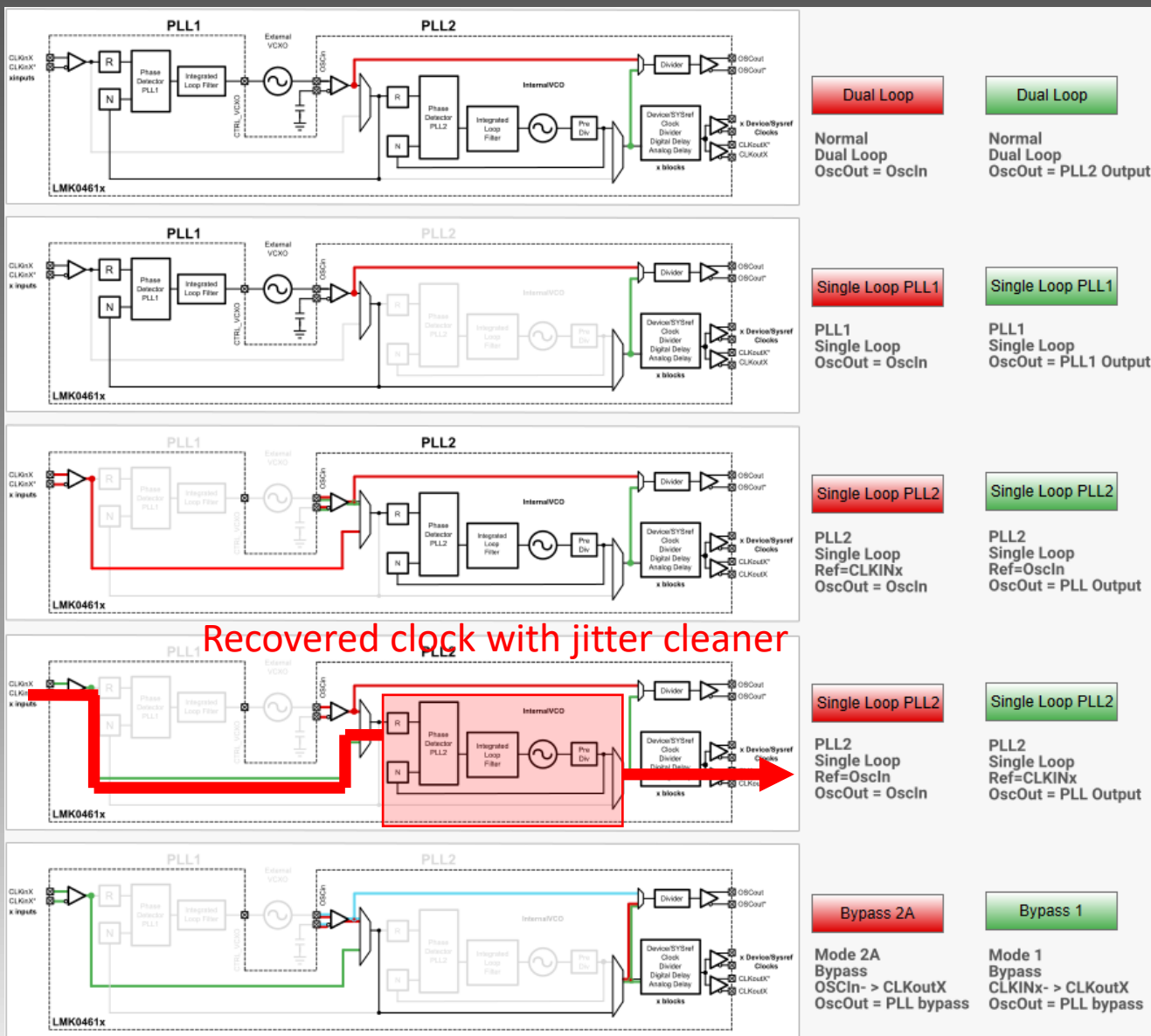
Mode 2A Bypass
OSCIn -> CLKOutX
OSCOut = PLL bypass

Bypass 1

Mode 1 Bypass
CLKINx -> CLKOutX
OSCOut = PLL bypass



Status of the DAQ electronics for the EMC PANDA DC



Recovered clock with jitter cleaner