Design and performance of dedicated ASICs for SiPM readout

F. Corsi, I. Indiveri, F. Licciulli, C. Marzocca, G. Matarrese

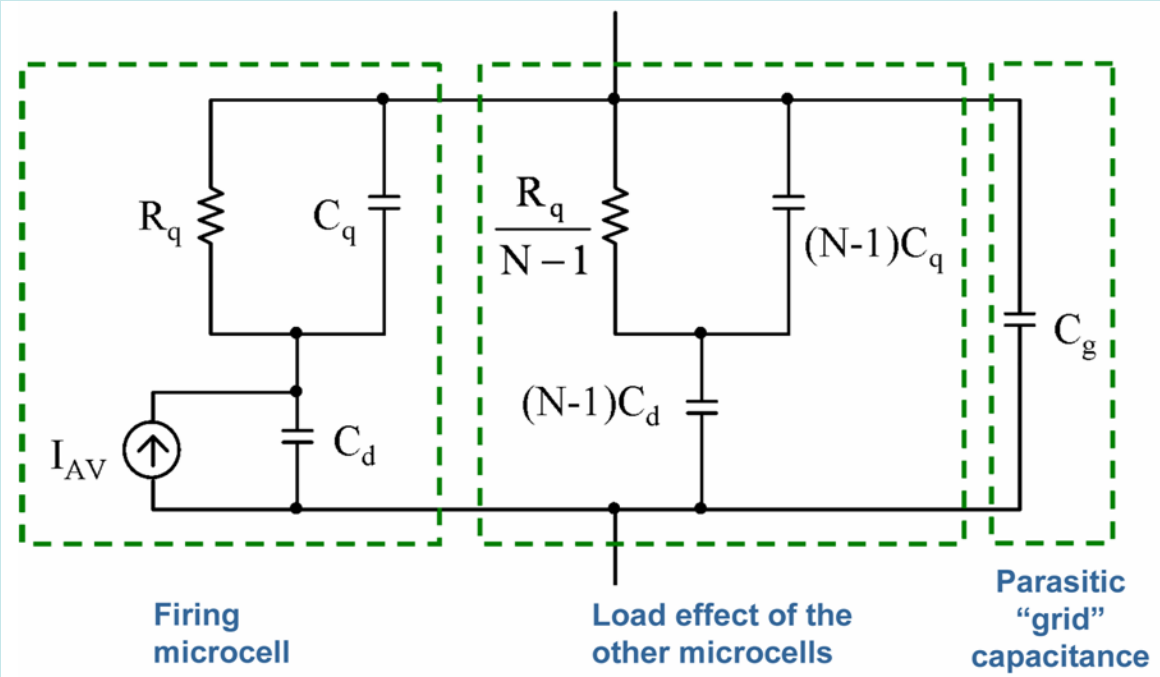
DEE - Politecnico di Bari and INFN - Sezione di Bari, Italy

I3HP-FP7 Silicon Multiplier Workshop, GSI, October 6-7, 2011

Outline

- Silicon Photo-Multipliers: model and characterization
- Front-end architecture: different approaches
- Structure and design of the analog channel
- Architecture and design of multichannel ASICs (BASIC8 and BASIC32)
- Characterization results
- Architecture of the last version of the ASIC (BASIC32_ADC)
- Ongoing and future work

SiPM model



R_q: quenching resistor (hundreds of kΩ)

C_d: photodiode capacitance (few tens of fF)

C_q: parasitic capacitance (smaller than C_d)

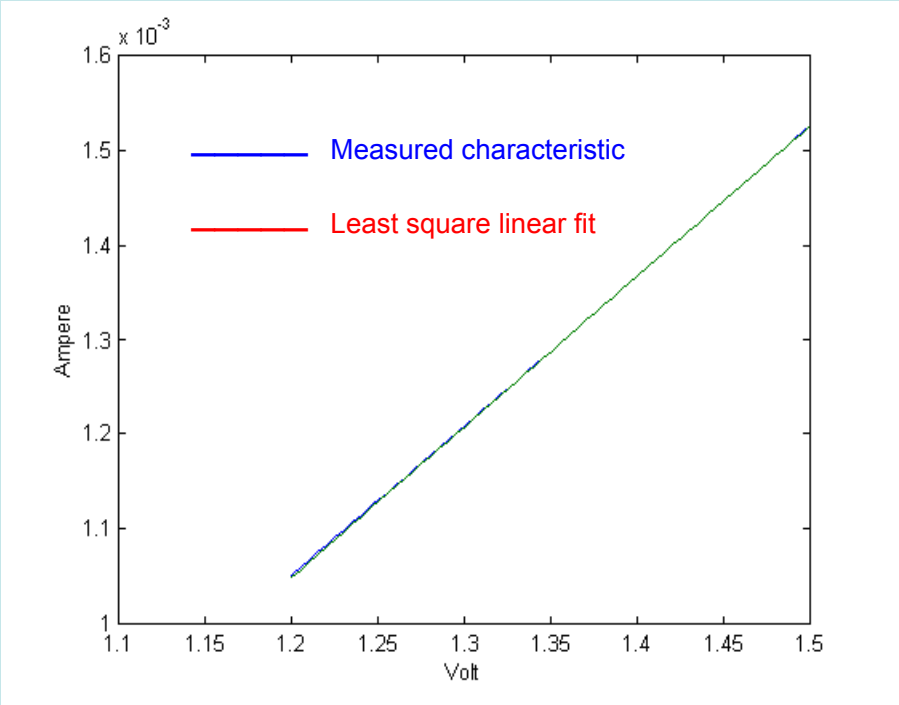
I_{AV}: short current pulse containing the charge Q delivered by a single microcell during the avalanche

- $Q=\Delta V(C_d+C_q)$, with $\Delta V=V_{BIAS}-V_{BR}$
- C_g : parasitic capacitance due to the routing of the bias voltage to the N microcells, realized with a metal grid.

Example: metal-substrate unit area capacitance 0.03 fF/mm^2
metal grid = 35% of the total detector area = 1mm^2 ⇒ Cg ≅ 10pF, without considering the fringe parasitics

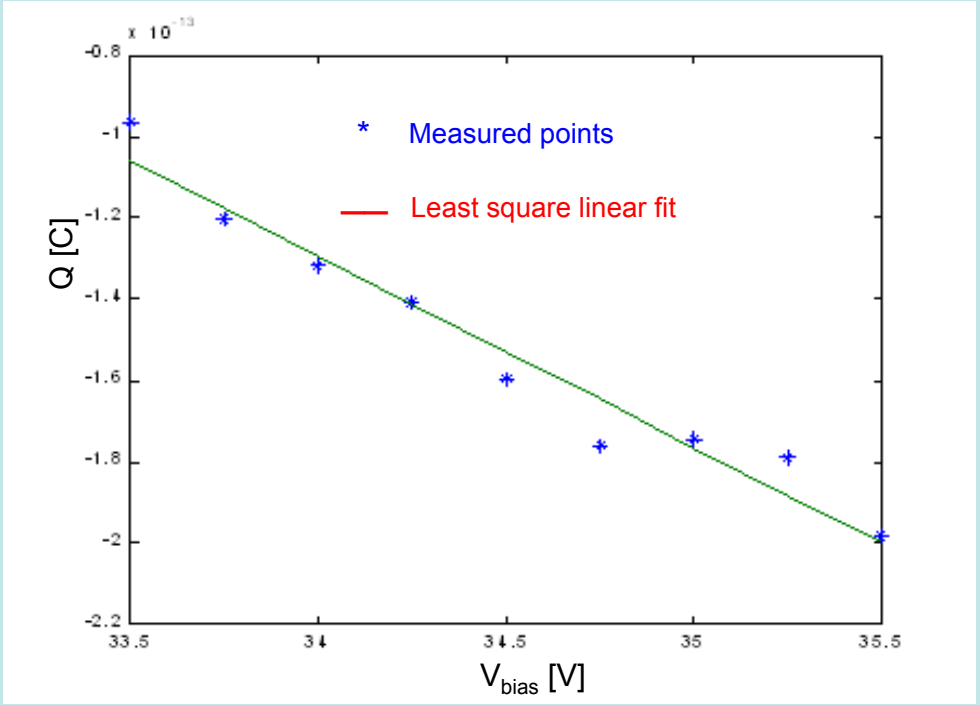
Parameter extraction I

R_q : forward characteristic of the SiPM (slope almost constant and equal to R_q/N)



Forward characteristic of a SiPM manufactured by FBK-Irst.

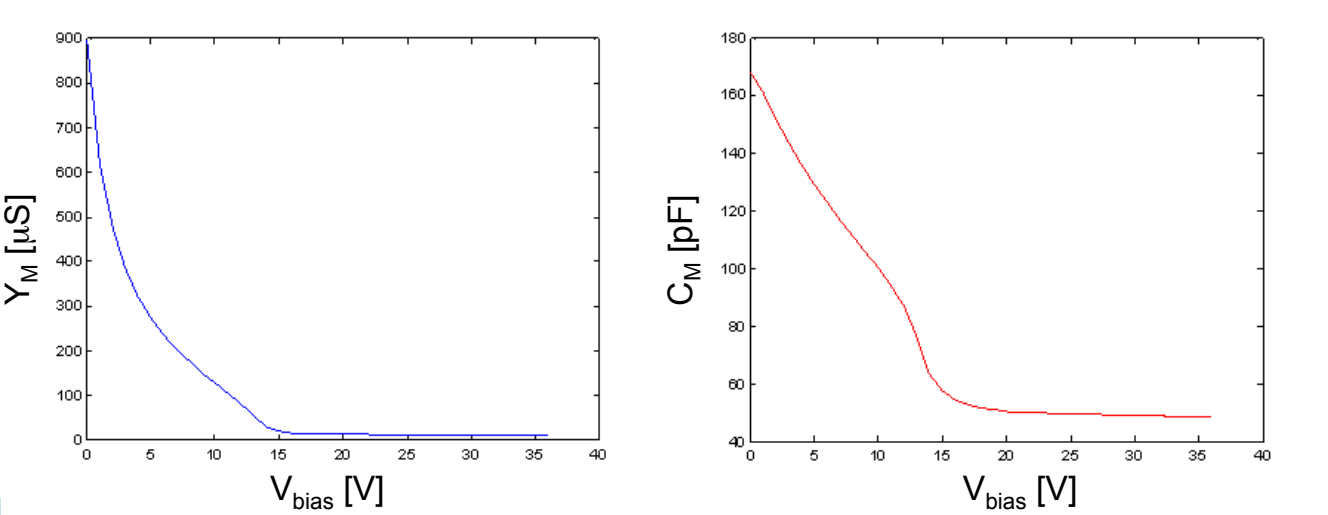
(Cd+Cq) and V_{BR}: charge associated to a single dark pulse as a function of the bias voltage $Q=(C_d+C_q)(V_{BIAS}-V_{BR})$



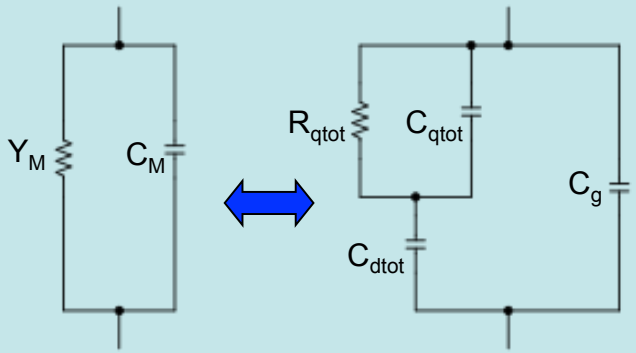
Charge contained in a single dark count pulse vs. bias voltage

Parameter extraction II

- CV plotter measurements of the SiPM near the breakdown voltage: Y_M and C_M
- According to the SiPM model, Y_M and C_M are expressed in terms of $C_{dtot}=NC_d$, $C_{qtot}=NC_q$, $R_{qtot}=R_q/N$ and the frequency ω of the signal used by the CV plotter.



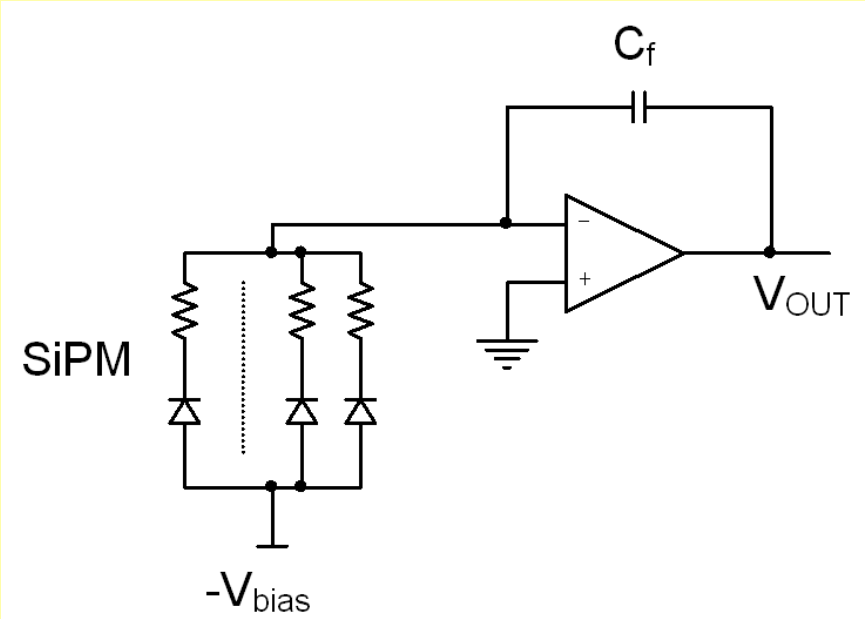
CV plotter measurement results for a SiPM manufactured from FBK-Irst.



$$Y_M = \frac{\omega^2 R_{qtot} C_{dtot}^2}{1+\omega^2 R_{qtot}{}^2 C_t^2} \qquad (C_t = C_{dtot} + C_{qtot}) \Rightarrow C_d, C_q$$

$$C_M = \frac{C_{dtot} + C_g + \omega^2 R_{qtot}^2 C_t (C_g C_t + C_{qtot} C_{dtot})}{1+\omega^2 R_{qtot}^2 C_t^2} \Rightarrow C_g$$

Front-end electronics: different approaches I



Charge Sensitive Amplifier

The charge delivered by the detector is collected on C_f

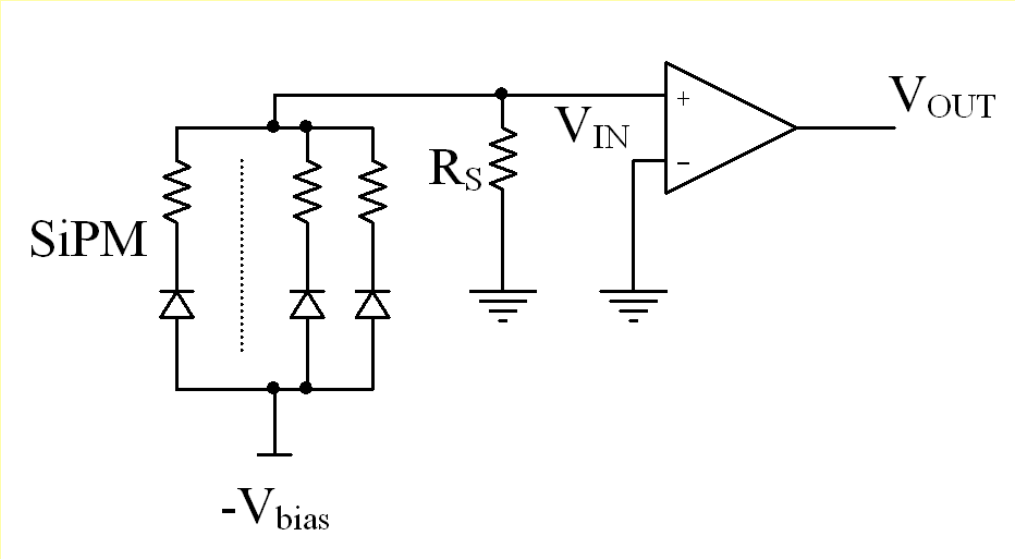
Example:

Maximum ΔV_{OUT} :	3V
SiPM gain:	10^6
No of hit microcells:	300
Total charge Q_{TOT} :	48pC

Large integration capacitance needed: C_f =16pF

- Dynamic range problems
- Large silicon area required
- Large capacitive loads: power consumption issues or bandwidth limitations

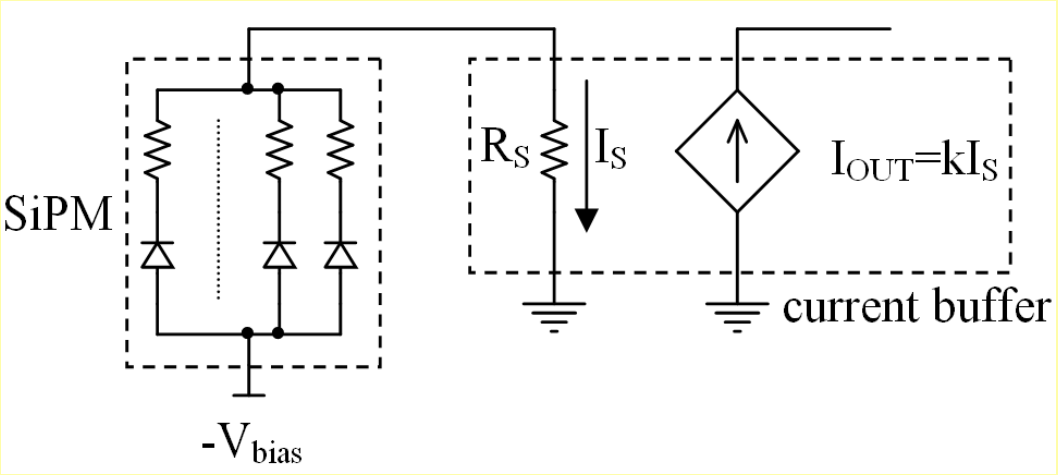
Front-end electronics: different approaches II



Voltage Amplifier

- A current-to-voltage conversion of the SiPM signal is realized by means of R_S
- Often used for characterization purposes
- V_{OUT} must be integrated to extract the charge information: further V-I conversion needed
- No virtual ground at the amplifier input: R_s must be small
- Small R_S: large gain, wide-bandwidth voltage amplifier required (power consumption issues)

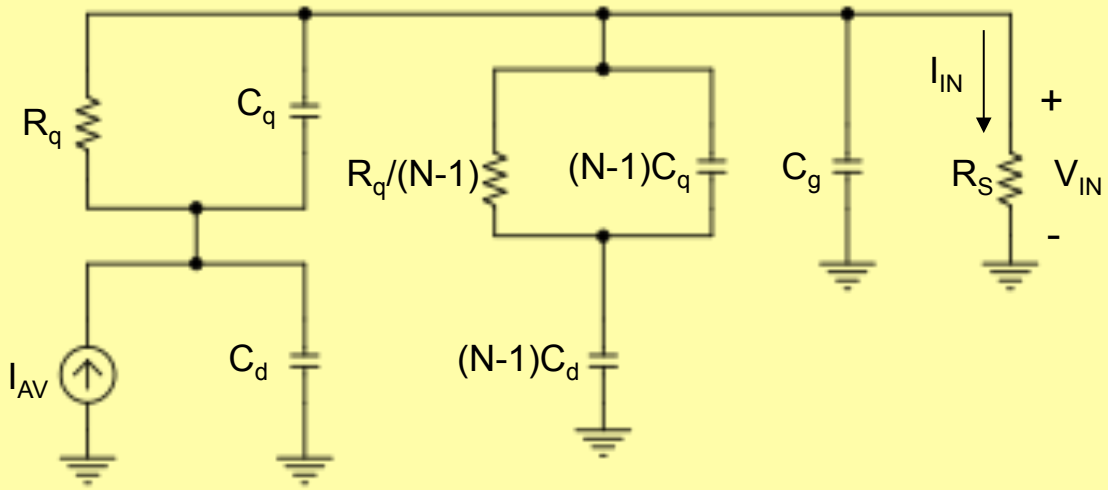
Front-end electronics: different approaches III



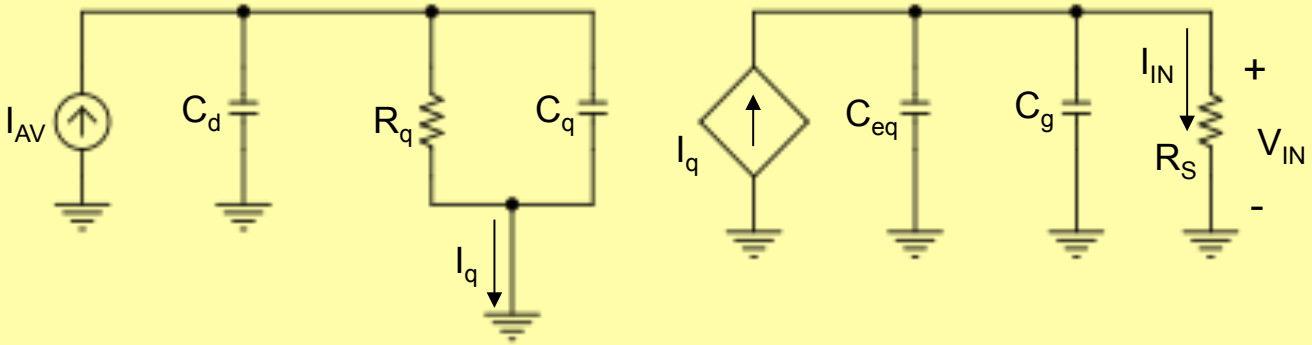
Current Amplifier

- R_S is the very small input impedance of the current amplifier
- The output current can be easily replicated (by means of current mirrors) and further processed (e.g. integrated)
- The circuit is inherently fast (low impedance nodes)
- Less problems of dynamic range, also for decreasing supply voltage

SiPM coupled to the front-end



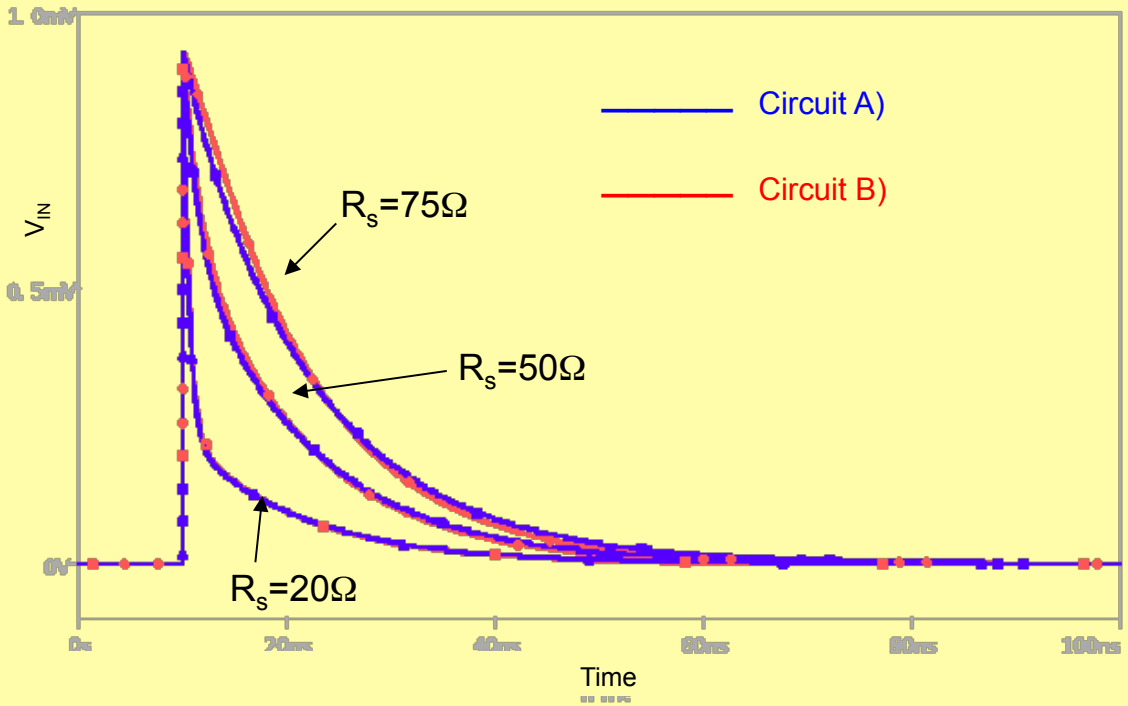
A) SiPM coupled to an amplifier with input impedance R_s



$$\frac{1}{C_{eq}} = \frac{1}{(N-1)C_d} + \frac{1}{(N-1)C_q}$$

B) Simplified circuit (R_S << R_q/N)

SiPM + front-end behaviour



Response of the circuits A) and B) to a single dark pulse (160fC) for three different values of Rs and typical parameter values

$$V_{IN}(t) \cong \frac{QR_S}{\tau_r - \tau_{IN}}\left(\frac{\tau_q - \tau_{IN}}{\tau_{IN}}\exp(-\frac{t}{\tau_{IN}}) + \frac{\tau_r - \tau_q}{\tau_r}\exp(-\frac{t}{\tau_r})\right)$$

$$(\tau_q = R_q C_q)$$

Simplified circuit: two time constants

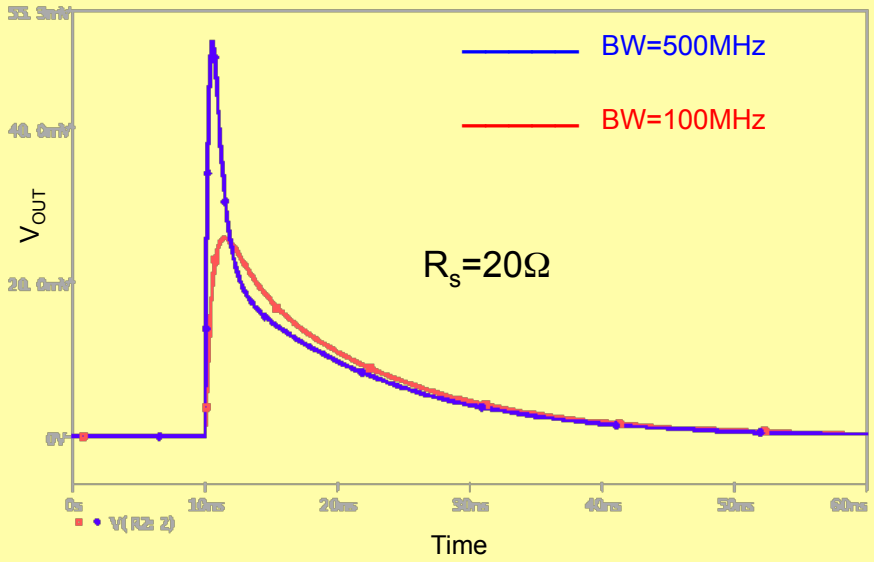
- $\tau_{IN} = R_s C_{tot}$
- $\tau_r = R_q(C_d + C_q)$

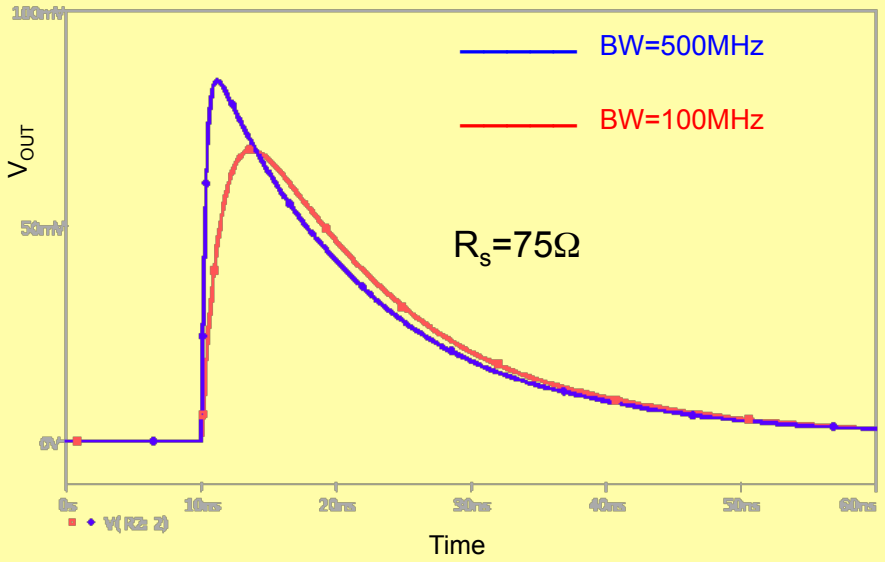
The peak of V_{IN} is almost independent of R_s

$$V_{INMAX} \cong \frac{Q_{IN}}{C_{tot}} \qquad Q_{IN} = Q\frac{C_q}{C_d + C_q}$$

A constant fraction Q_{IN} of the charge Q delivered during the avalanche is almost instantly collected on $C_{tot}=C_g+C_{eq}$

Bandwidth of the amplifier



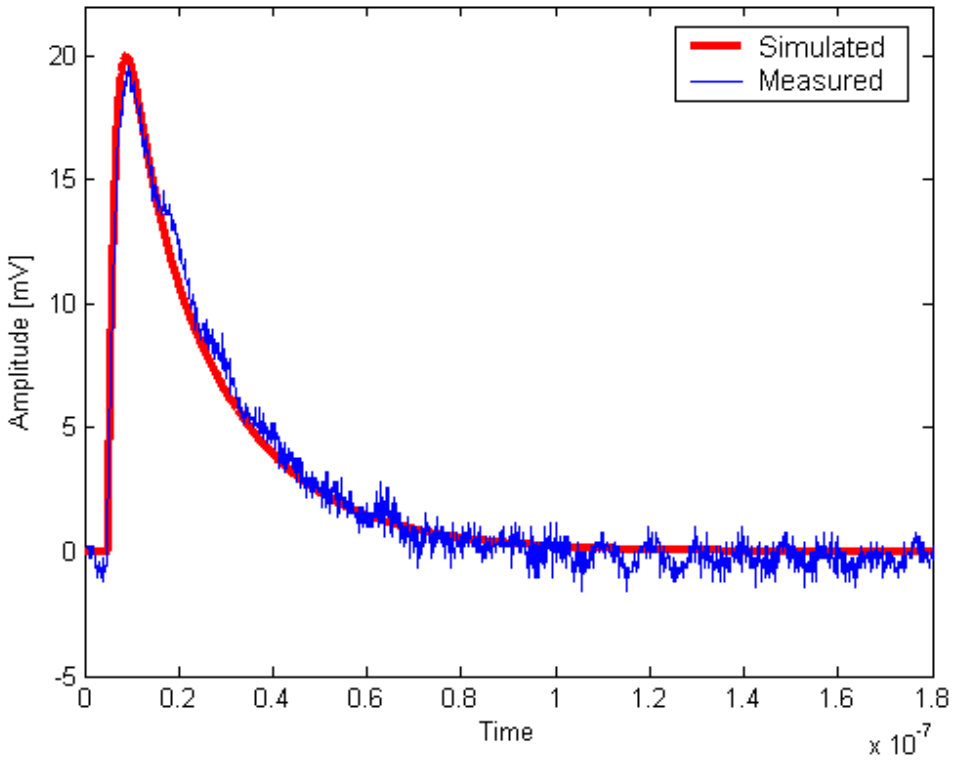


Amplifier output voltage for a single dark pulse: same gain and different bandwidth

- The bandwidth of the amplifier directly affects the **rise time** of the waveform, independently of the value of R_S
- The **peak** of the waveform is strongly dependent on the amplifier bandwidth, especially for low values of R_S
- The **time needed to collect the charge** is just slightly influenced by the amplifier bandwidth
- The same conclusions are valid also for the waveform of the output current obtained with a current amplifier

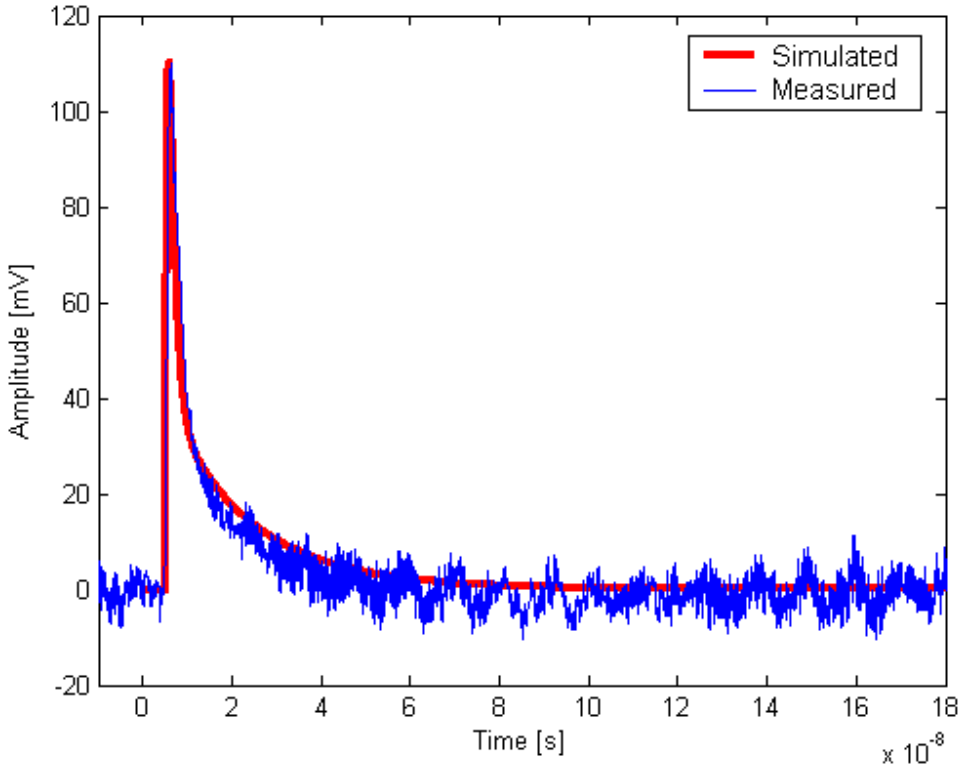
Model validation

Two different discrete amplifiers have been used to read-out the same SiPM



a) Transimpedance amplifier

BW=80MHz Rs=110Ω Gain=2.7kΩ

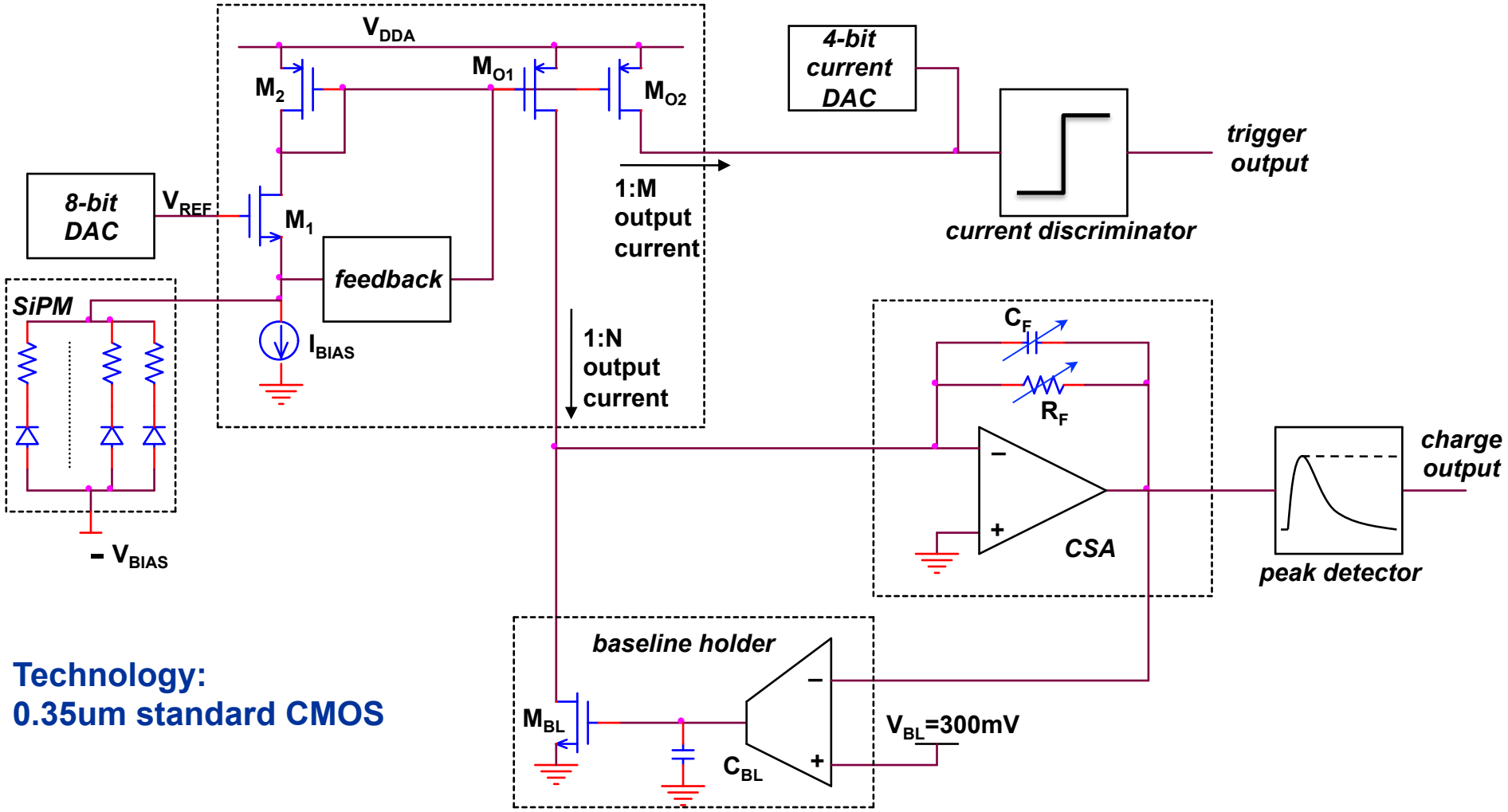


b) Voltage amplifier

BW=360MHz Rs=50Ω Gain=140

- **The model extracted according to the procedure described above has been used in the SPICE simulations**
- **The fitting between simulations and measurements is quite good**

Structure of the analog channel



Technology:
0.35um standard CMOS

Main features and parameters of the analog channel

Current buffer

- Small signal bandwidth: 250MHz (with a 30pF detector)
- Low input resistance: 17Ω
- Scaling factors: N=10, M= 20
- V_{REF} variable in the range 1V÷2V
- Total current consumption: 800uA

Fast Current Discriminator

- Leading edge
- Trise ≈ 300ps
- Threshold programmable : 4-bit current DAC from 0 to 40μA

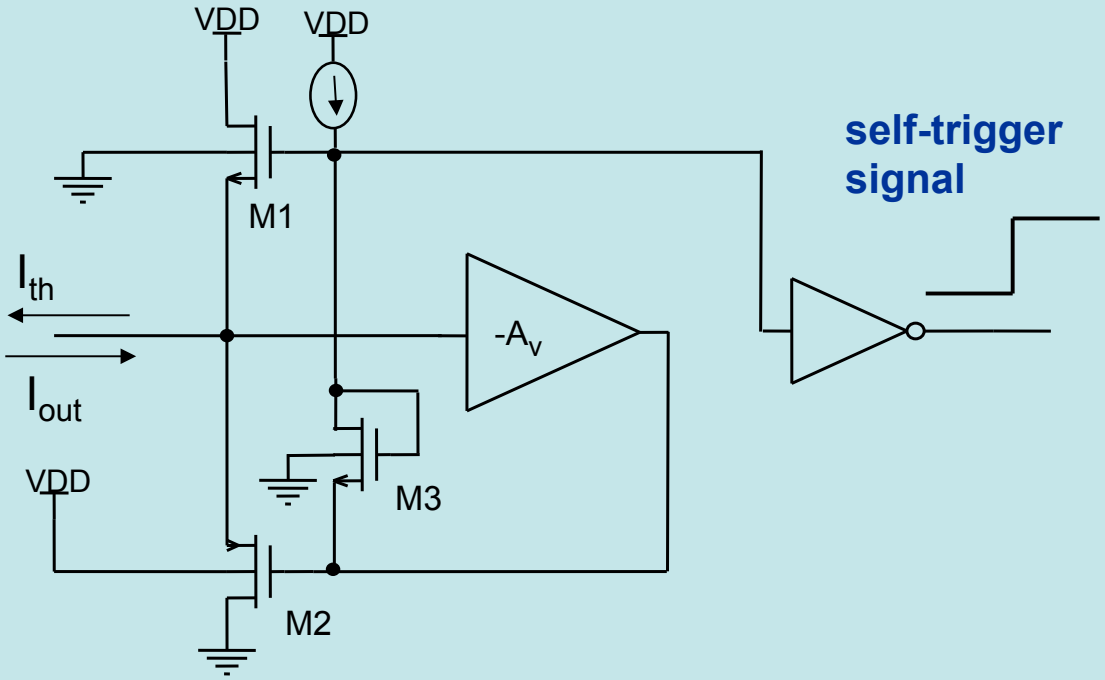
CSA

- Continuous passive reset
- Variable gain: C_F=1pF, 2pF, 3pF
- Damping time constant: 200ns
- Output voltage range: 0.3V ÷ 2.7V

Baseline holder

- Very slow feedback loop
- "Ad hoc" techniques to reproduce large time constants
- Small baseline shifts at high event rates (-1mV @ 100kHz, full dynamic)

The current discriminator



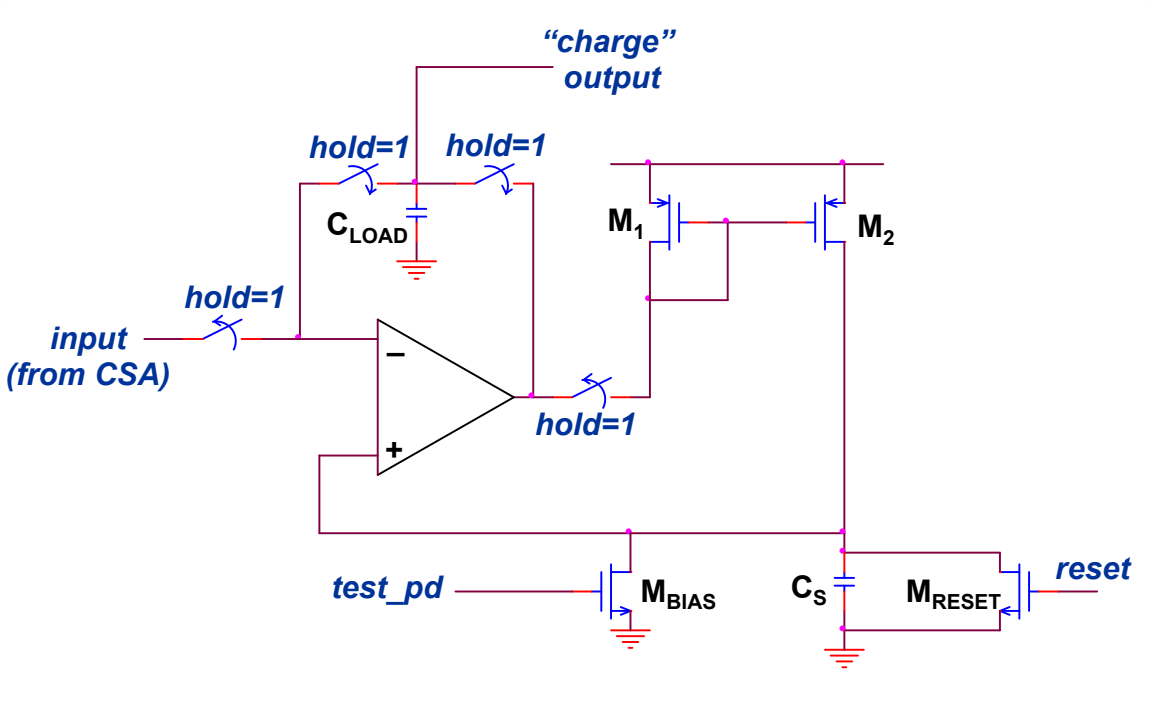
Principle of operation

If I_{out} is less than I_{th}, then M1 is on and M2 is off. When I_{out} becomes greater than I_{ref}, the MOSFETs switch and the amplifier output goes low, thus the inverter output goes high

- **Threshold level set by the value of I_{th} (4-bit current DAC from 0 to 40μA)**
- **Rise time of the output signal ≅ 300ps**

Peak detector modes of operation

- Logic control signals involved: “hold”, “test_pd” and “reset”



test_pd=1, hold=0

The voltage on C_S follows the CSA output , thanks to the current of M_{BIAS}

test_pd=0, hold=0

The voltage on C_S tracks the peak of the CSA output (M_{BIAS} is OFF)

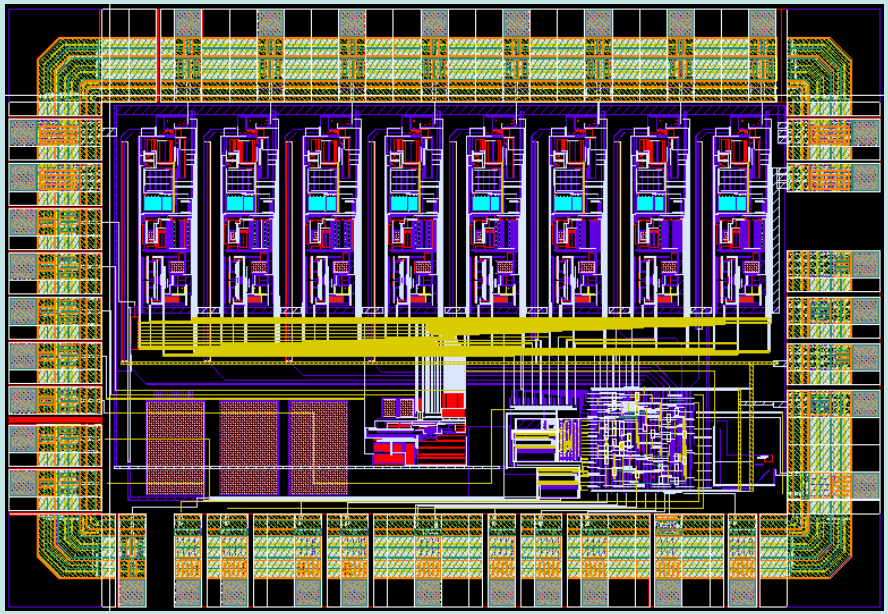
test_pd=0, hold=1

The voltage stored on C_S is buffered ad transferred to the output of the circuit.

Multichannel ASICs available

BASIC8

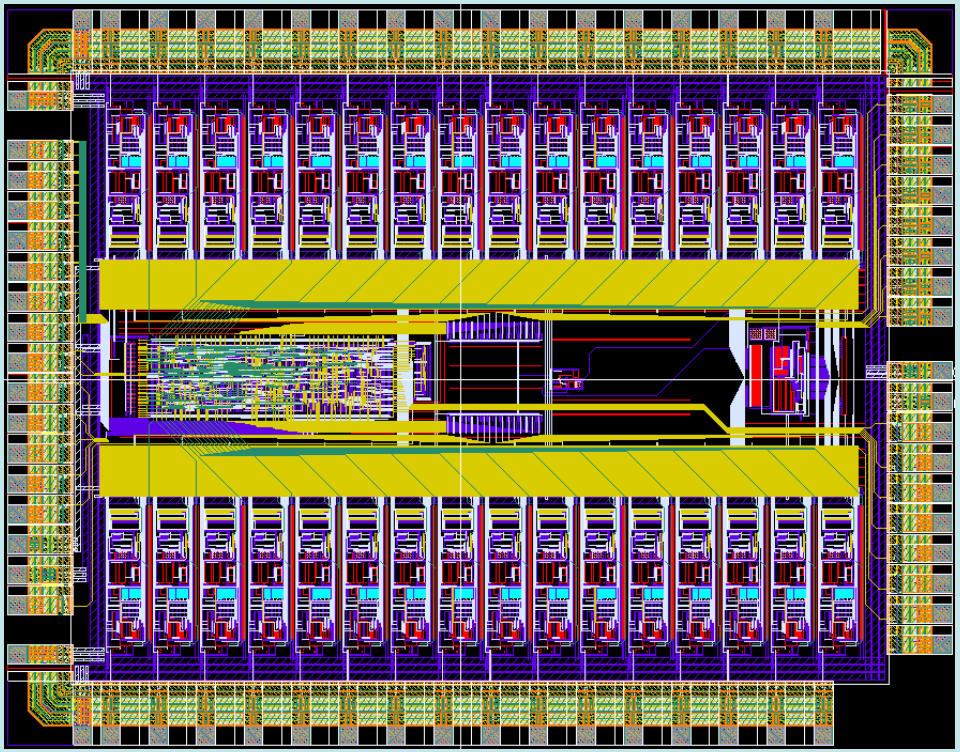
- ❑ 8 channels
- ❑ “Sparse” and “serial” read-out modes
- ❑ 8 bit SAR integrated ADC



Layout of BASIC8 (3.2 x 2.2 mm²)

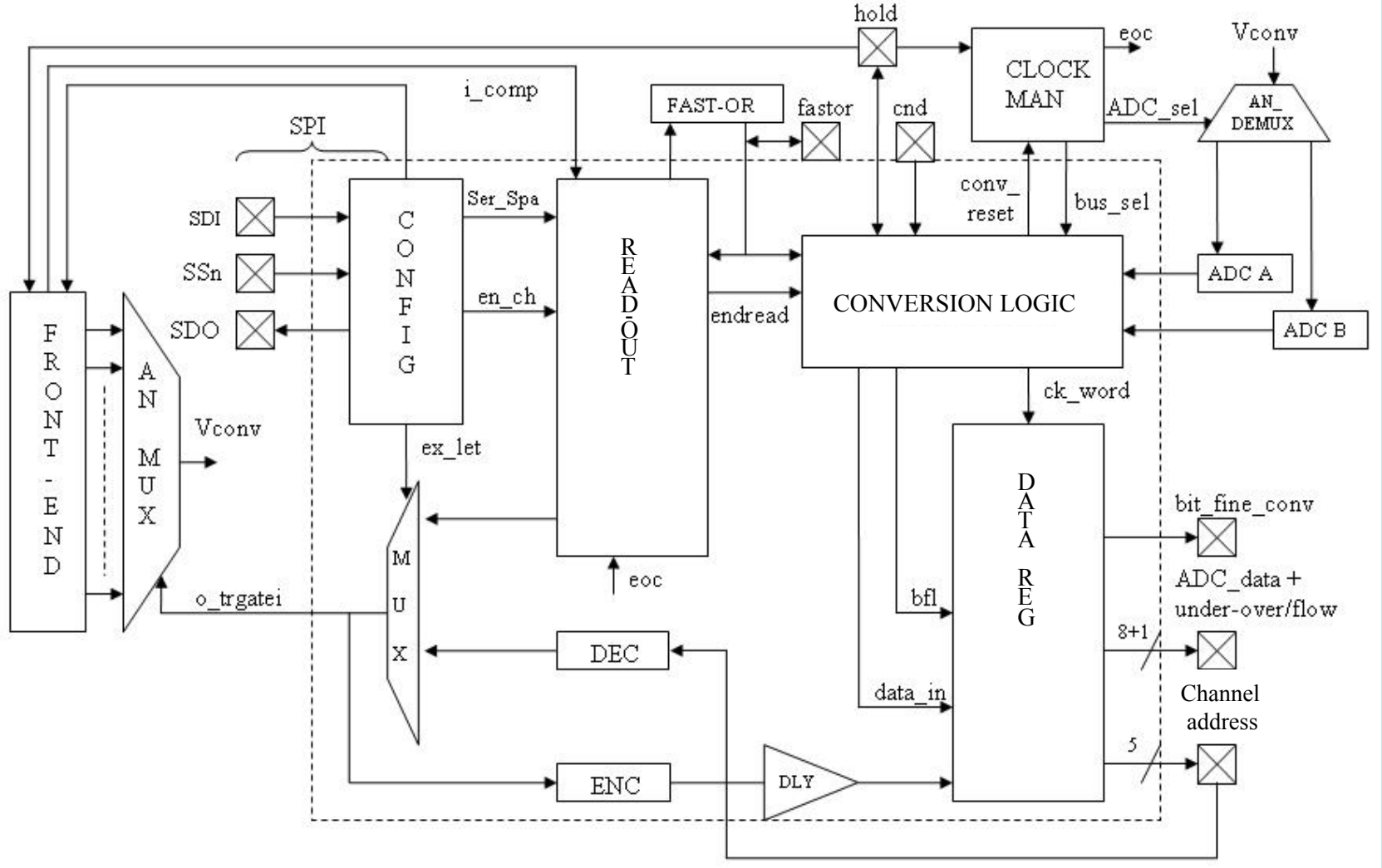
BASIC32

- ❑ 32 channels
- ❑ Enhanced programmability and RO modes
- ❑ No integrated ADC



Layout of BASIC32 (5 x 3.9 mm²)

BASIC32: block diagram



BASIC32: main features

Acquisition modes

Internal read-out

Internal trigger ("fast-OR") } Sparse
External trigger } Serial

External read-out

External control of the PD's
External channel addressing

⇩

Multiplexing and reset of the channels managed by the read-out logic

Configuration logic

- ❑ **SPI interface**
- ❑ **56-bit configuration word**
- ❑ **Verification features**

Read-out logic

- ❑ **Multiplexer management**
- ❑ **Fast-or management**
- ❑ **Masking and reset of the channels**

Conversion logic

- ❑ **ADC management**
- ❑ **Data flow management**
- ❑ **End of acquisition control**

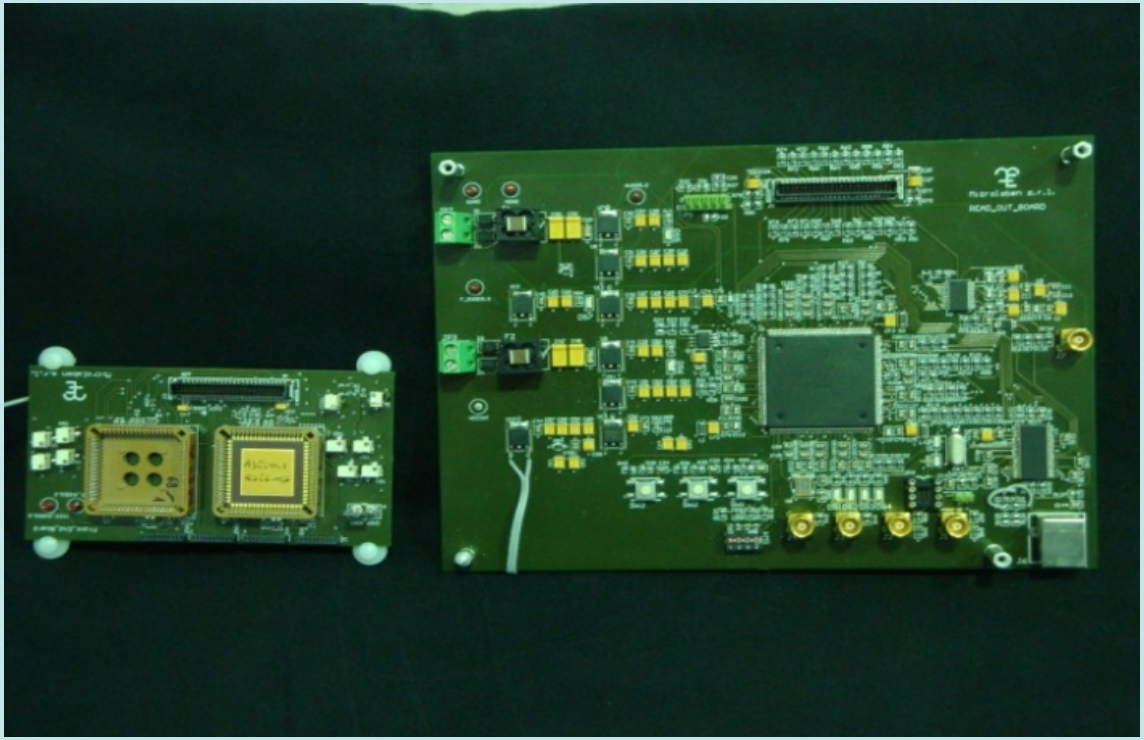
Coincidence management

- ❑ **External "coincidence" signal:**

In internal read-out mode, the acquisition is conditioned by this signal

BASIC32: characterization

Test boards



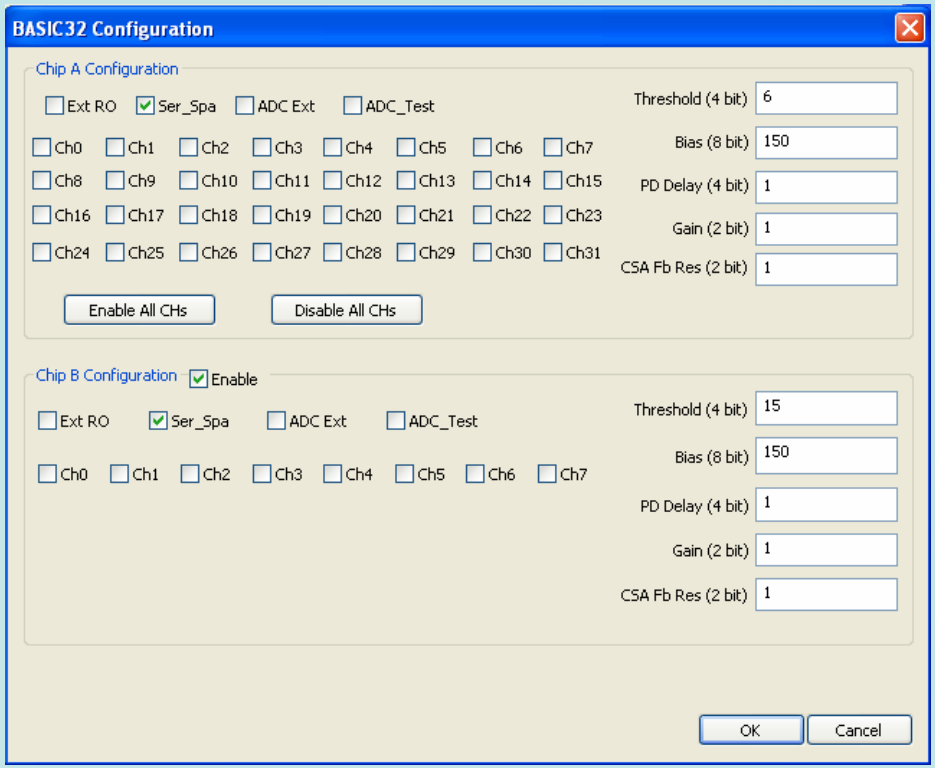
Front-end board

- Housing for two ASICs
- Bias for the detectors
- Analog buffers
- Voltage and current refs.

Read-out board

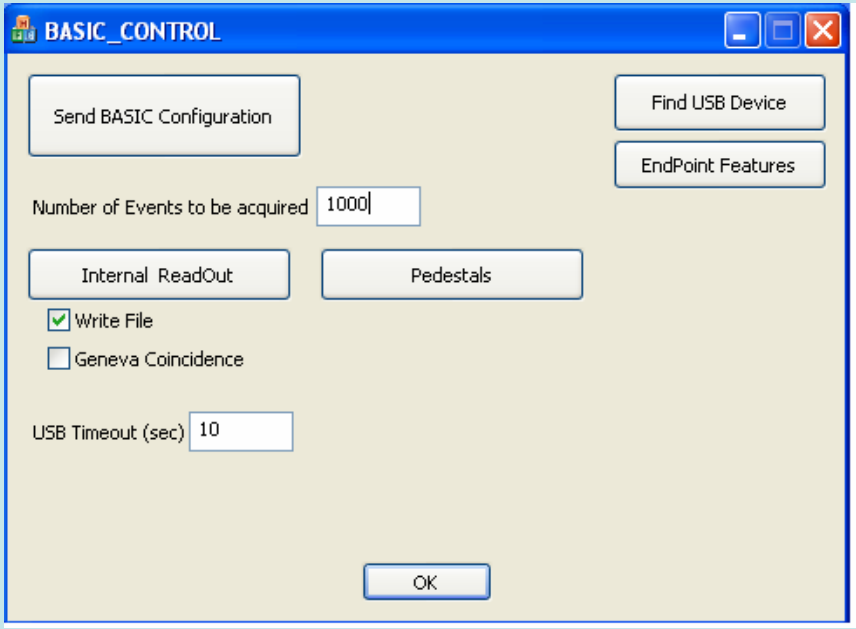
- 12 bit, 40MS/s external ADC
- FPGA Altera Cyclone II EPC20Q240
- USB interface

Management and acquisition software

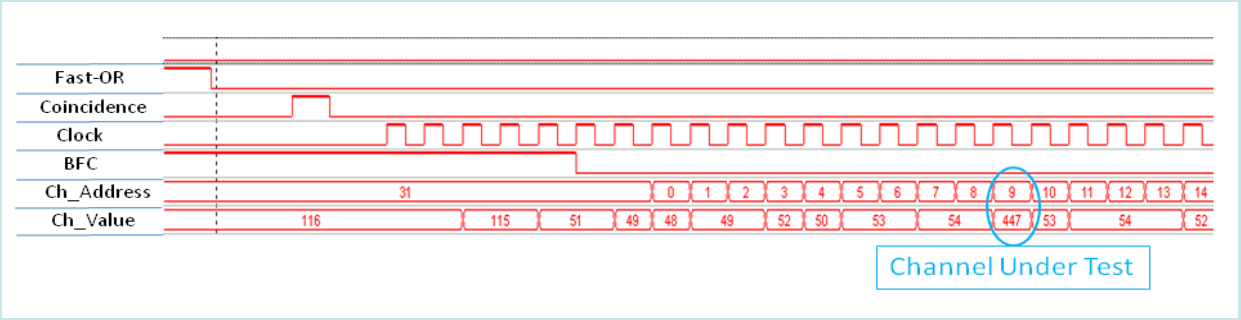


Configuration mask

Visual C++ application

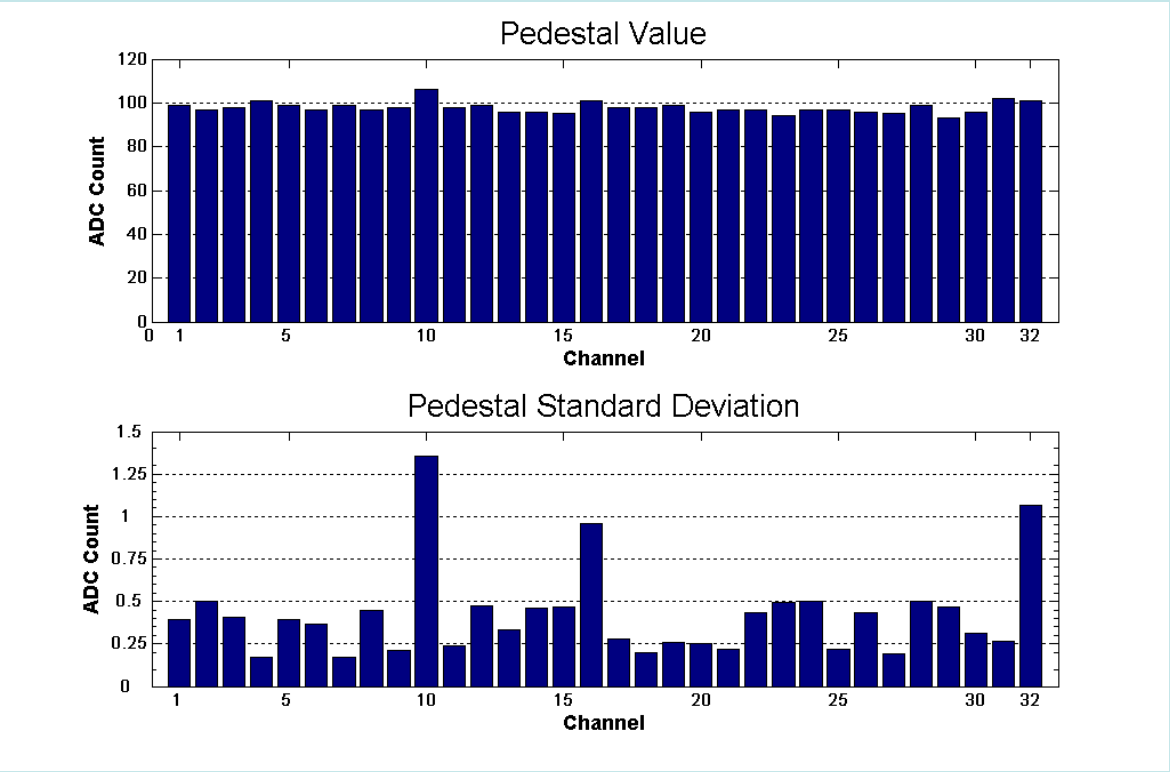


Acquisition control window



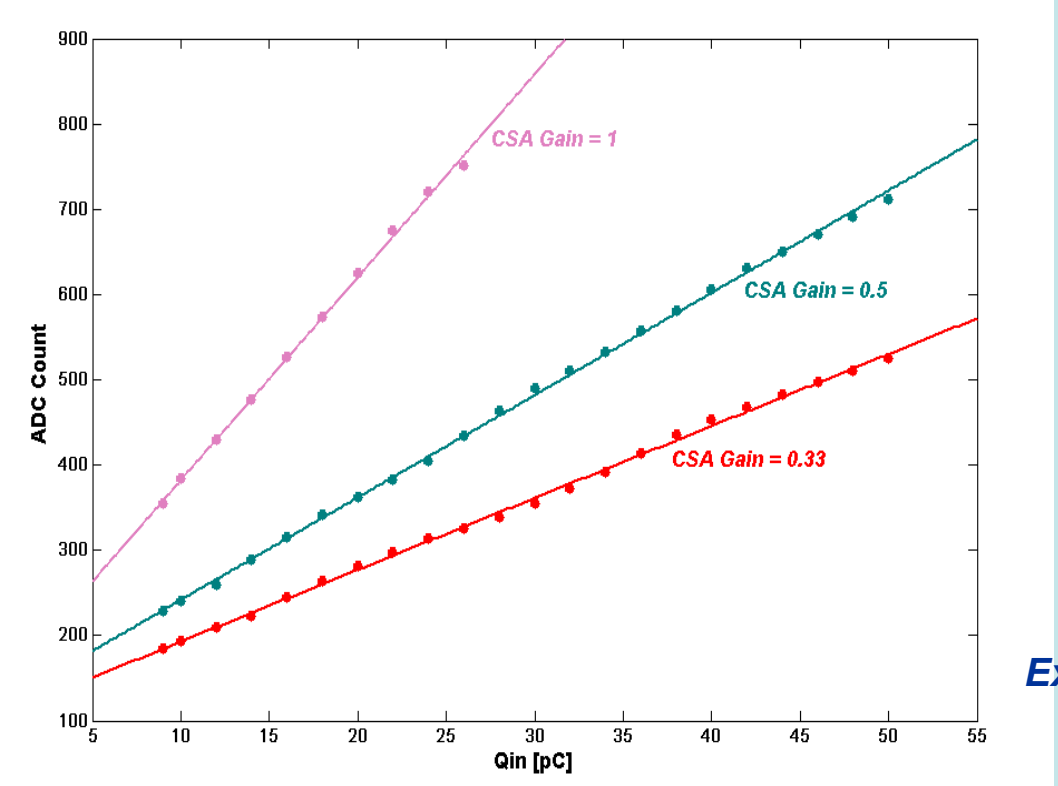
Altera SignalTap tool used to monitor the firmware

Experimental results: pedestals



- *Acquisition mode: internal read-out , external trigger, serial*
- *The "test_pd" signal of the PD's is controlled externally, to avoid the discharge of the Cs capacitance during the "hold=1" phase*
- *An ADC count corresponds to about 3.9 mV*
- *Pedestals quite uniform*
- *Some channels exhibit more noise than the average, i.e. about 1.7mV rms, corresponding to 50fC rms*

Experimental results: injection capacitance, gain



Charge to voltage gain of the analog channel

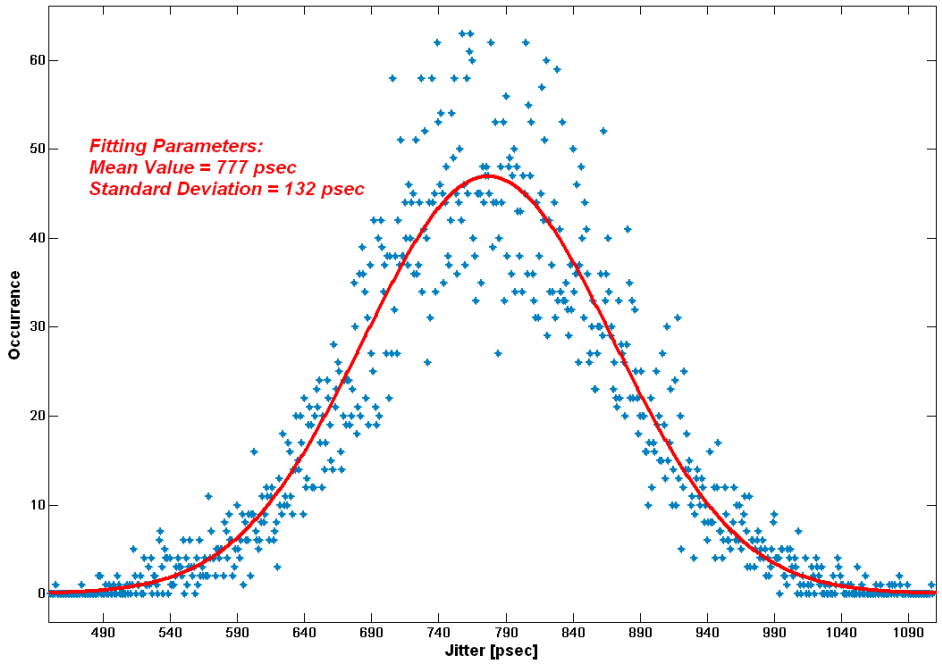
$$\frac{\Delta V_{OUT}}{Q_{in}} = \frac{1}{NC_F}$$

C_F	1pF	2pF	3pF
Expected gain	100	50	33
Measured gain	94	47	33

Expected and measured values of the gain $\Delta V_{OUT}/Q_{in}$ [mV/pC]

- ***Overall charge to voltage gain very close to the expected one (max. deviation ≅ 6%)***
- ***Max dynamic range ≅ 70pC @ C_F=3pF (1% linearity error)***

Experimental results: injection capacitance, timing



Timing accuracy of the fast-OR response vs the input pulse

- ***Measured standard deviation***

  $\sigma_{meas} \cong 132$ ps

- ***Intrinsic error of the measurement setup***

  $\sigma_{setup} \cong 60$ ps

- ***Resulting intrinsic timing accuracy of the fast-OR signal***

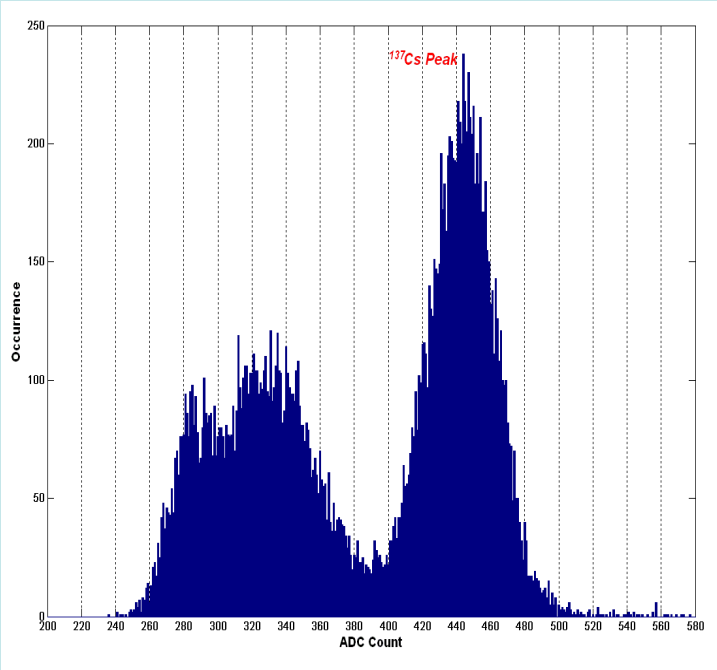
  $\sigma_{int} \cong 118$ ps

Experimental results: coupling to SiPM+scintillator (I)

- *MPPCs Hamamatsu a) 3600 micro-cells, 3x3mm^2 , (gain = 7.5x10^5 @ V_{BIAS}=71.3V) and b) 782 micro-cells, 3.22x1.19mm^2, (gain = 1.3x10^5 @ V_{BIAS}=71.2V)*
- *MPPCs coupled to a small LYSO scintillator 3x3x10mm^3*
- *The MPPC+LYSO detector has been coupled to a channel of the ASIC and exposed to different radiation sources:*

^{176}Lu (203keV and 307keV), ^{22}Na (511keV), ^{137}Cs (662keV), ^{57}Co (122keV)

Hamamatsu MPPC coupled to the LYSO crystal

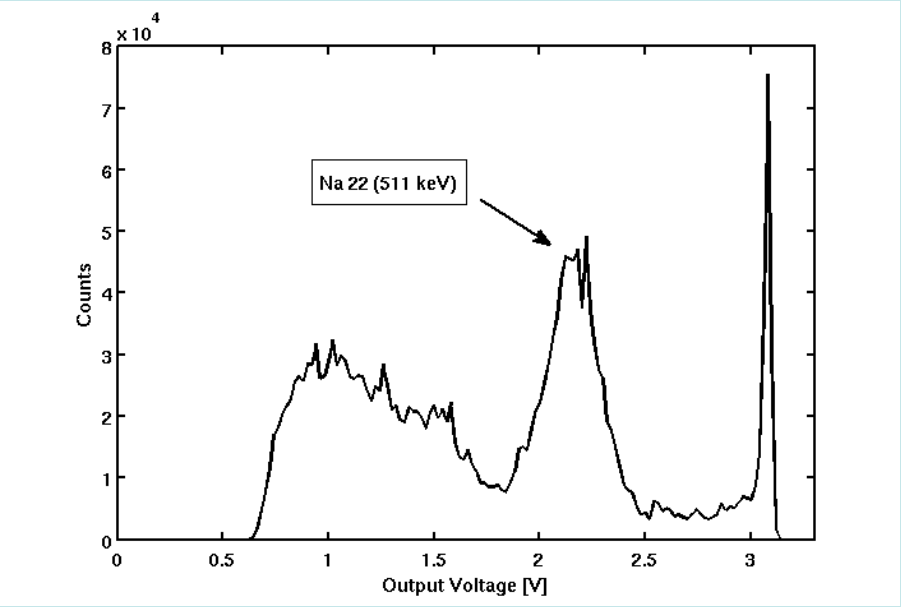


Example of ^{137}Cs spectrum (≅ 12% FWHM)

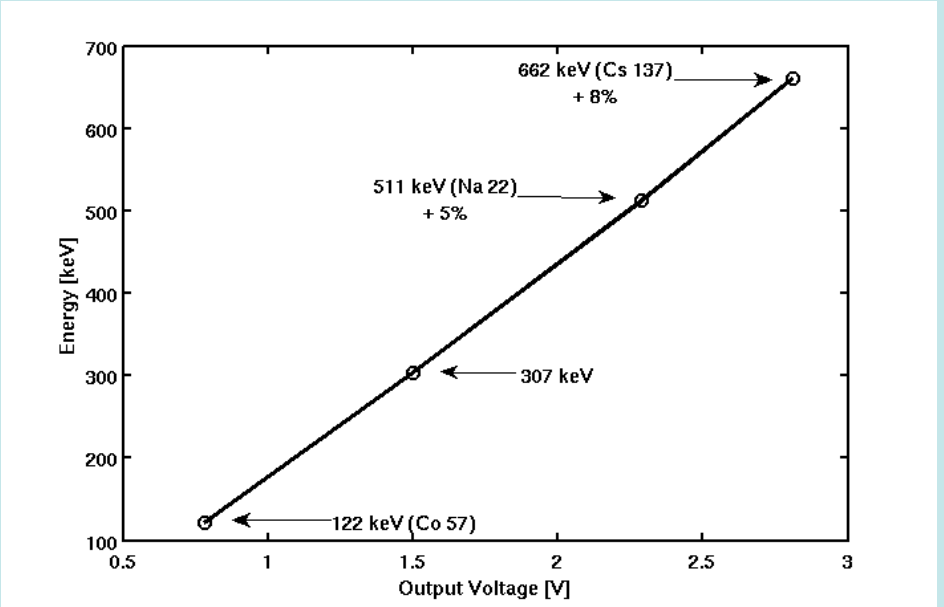
- *3x3mm^2 MPPC*
- *V_{BIAS} = 70.2V*
- *Gain = 33mV/pC*

Experimental results: coupling to SiPM+scintillator (II)

- ***782 micro-cells Hamamatsu MPPC, V_{BIAS} = 70V, gain = 0.33mV/pC***



Spectrum of ^{22}Na (about 22% FWHM)

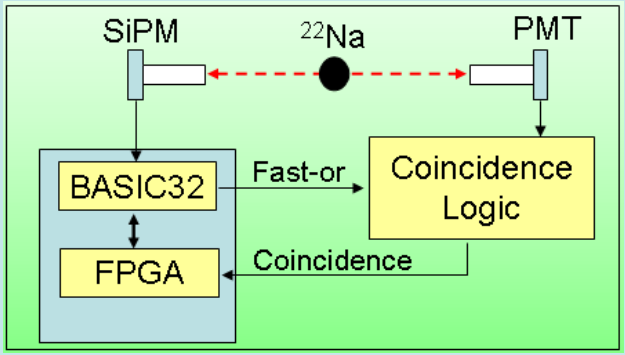


Energy vs average output voltage for the different sources

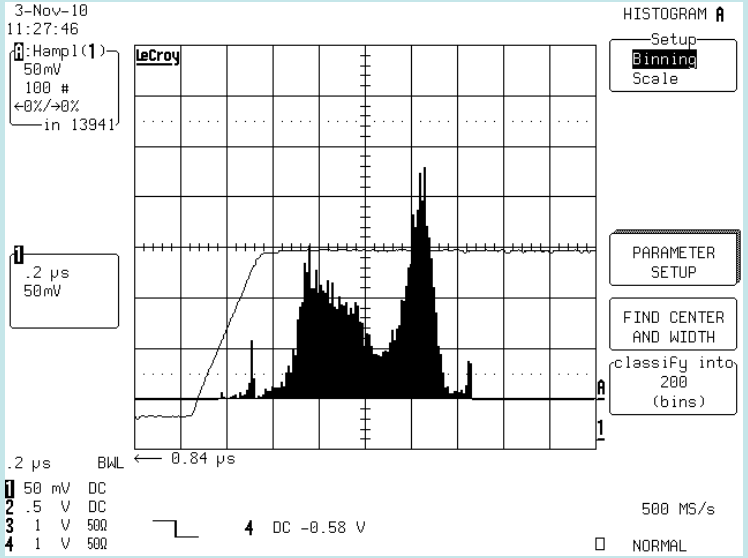
- ***Corrections applied to compensate for MPPC saturation (large no. of fired micro-cells)***

Measurements of SiPM in coincidence with a PMT (I)

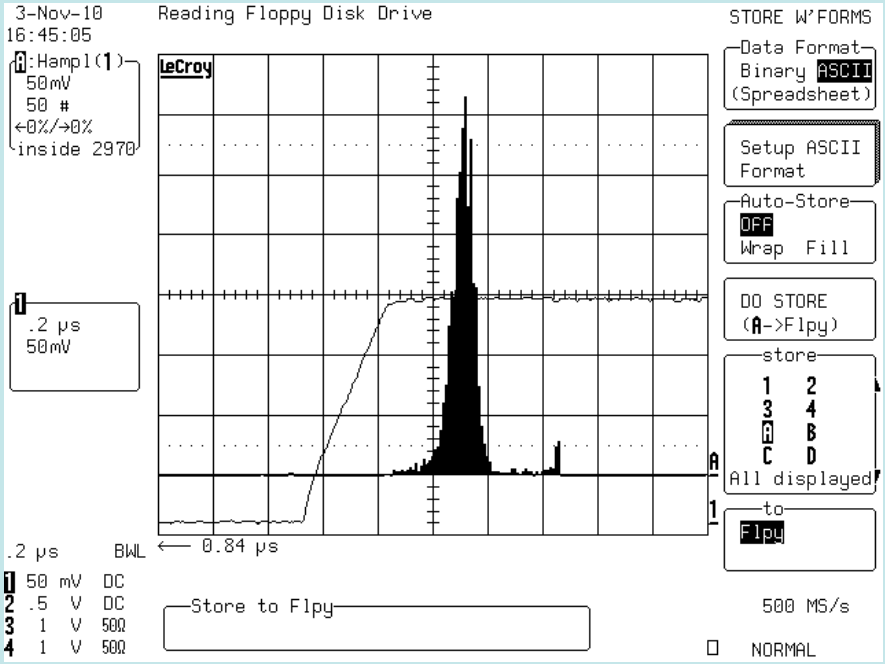
Measurement setup at CERN (courtesy of E. Chesi, A. Rudge and J. Seguinot)



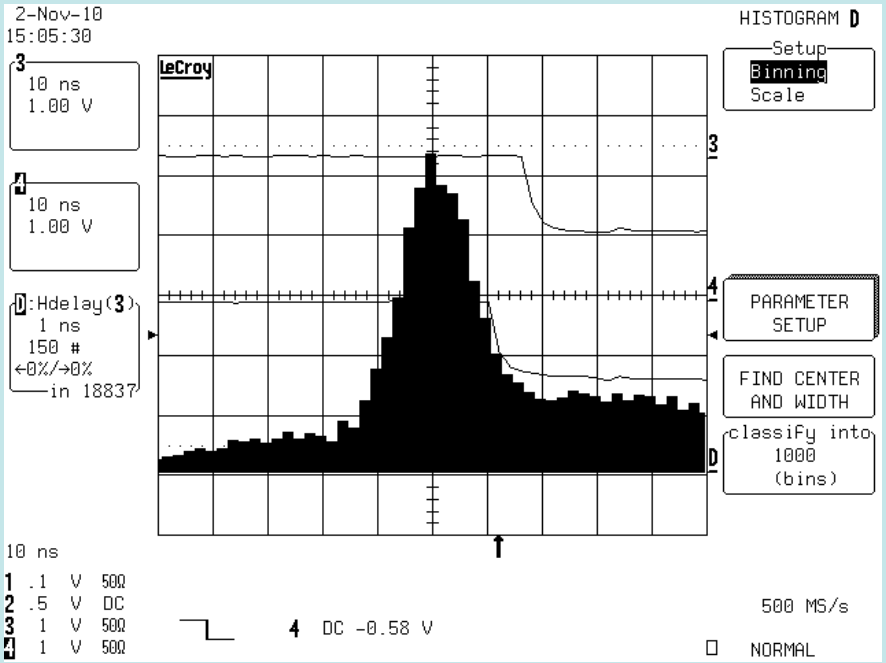
- ***Measurements taken in coincidence with a PMT***
- ***Very low event rate (≅ 1.9 Hz)***
- ***Signals acquired with an oscilloscope***
- ***Spectrum of ^{22}Na spectrum very similar to the one shown in the previous slide (low threshold)***



Measurements of SiPM in coincidence with a PMT (II)



Energy spectrum of ^{22}Na



Timing accuracy of the fast-OR signal vs the trigger provided by the PMT

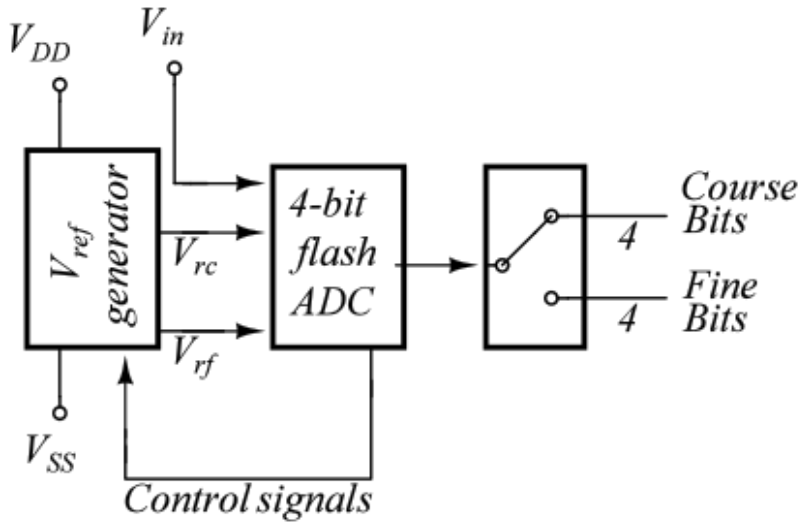
- ***Threshold increased to get rid of the Comptons:***

  energy resolution ≅ 11% FWHM

- ***Low threshold level:***

  timing accuracy ≅ 1.2 ns FWHM

Design of a “two step” (subranging), 8-bit ADC



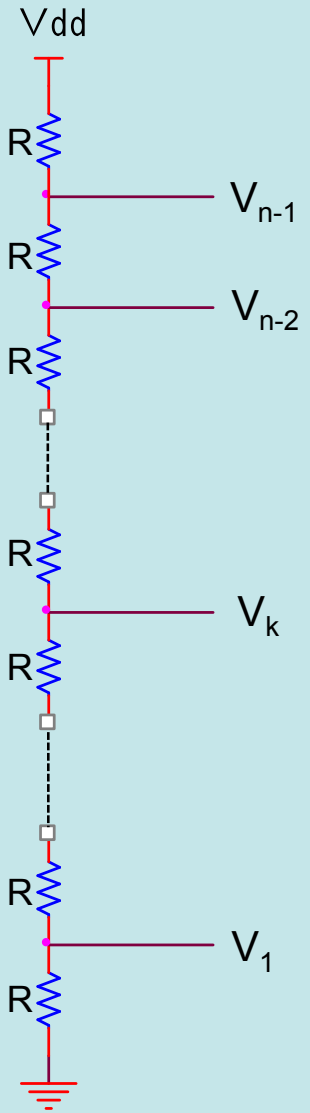
Schematic architecture of the AD converter

Same comparators used in both conversion phases, i.e. “coarse” (MSB’s) and “fine” (LSB’s), by conveniently selecting in each phase the thresholds, generated by a resistor ladder

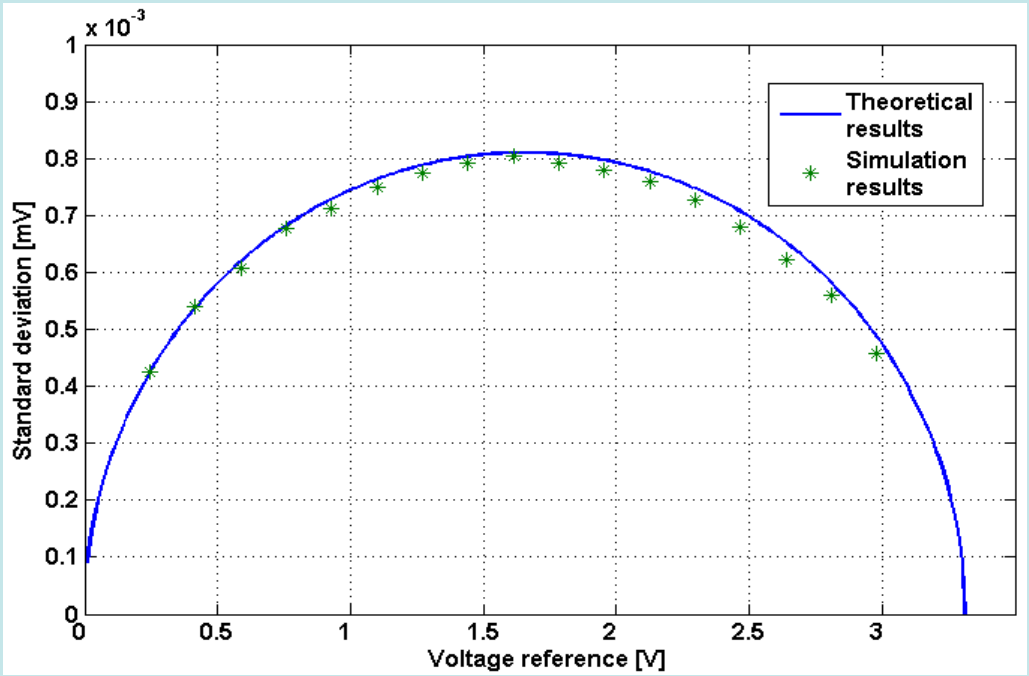
- ***Correction logic for both “bubble” error and wrong “fine” threshold selection***
- ***Boost circuits for the clock phases applied to the CMOS switches***
- ***Layout of the resistor ladder designed on the basis of a statistical analysis of the effects of mismatch***
- ***Final ADC structure: two ADC of the described kind, operated in “interleaved” mode***
- ***Total power consumption: 22.4mW***
- ***Maximum conversion speed (post-layout simulations): 20MS/s***

“Two step”, 8-bit ADC: design of the resistor ladder

- ***Statistical model of the reference voltages vs resistor mismatch***

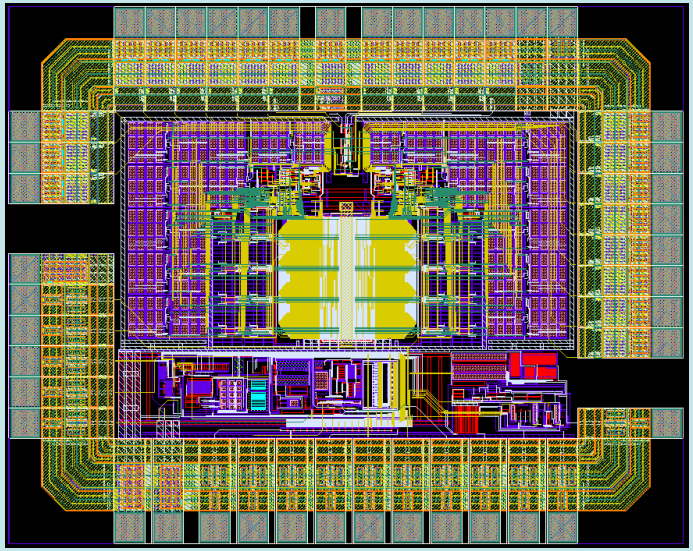


- ***Resistor mismatch:*** $\sigma_{\Delta R/R} = \dfrac{A_R}{\sqrt{W \cdot L}}$
- ***Variance of V_K :*** $\sigma^2_{V_K} = \alpha k(n-k)$ $\left(\alpha = \dfrac{V_{dd}^2 \sigma^2_{\Delta R/R}}{n^2(\sqrt{n} - 3\sigma_{\Delta R/R})^2}\right)$
- ***Max. error (k=n/2):*** $\sigma_{V_{kMAX}} = \dfrac{V_{dd}\sigma_{\Delta R/R}}{2(\sqrt{n} - 3\sigma_{\Delta R/R})}$

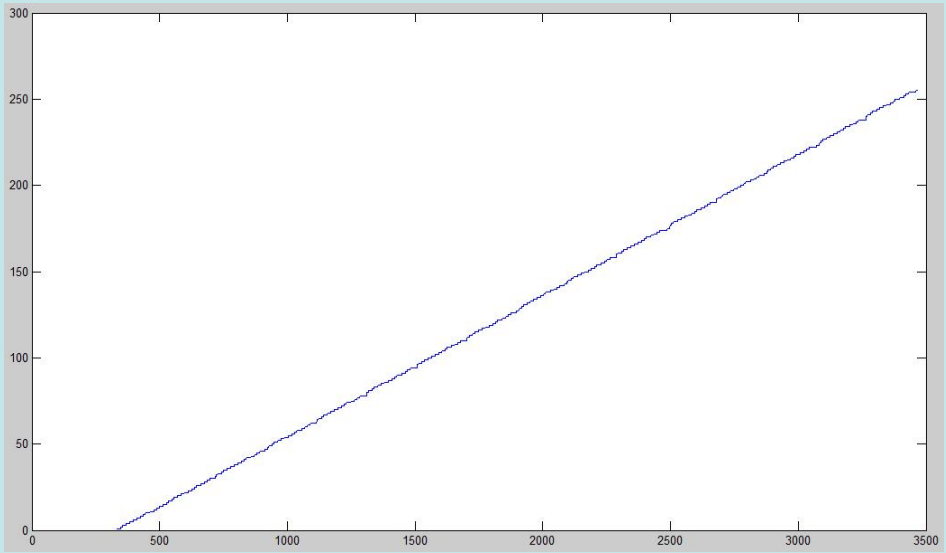


Good agreement between theoretical results and MC simulations

“Two step”, 8-bit ADC: test chip and results



Layout of the test chip (2.18 x 1.74 mm^2)



ADC input –output characteristic

	DNL	INL
ADC_1	1.18LSB	1.44LSB
ADC_2	1.27LSB	1.65LSB

- ***Problems in the intervention of the correction logic (missing codes)***
- ***The resistor ladder exhibits good accuracy***
- ***Offset of the comparators slightly greater than expected***
- ***Good 7-bit ADC***

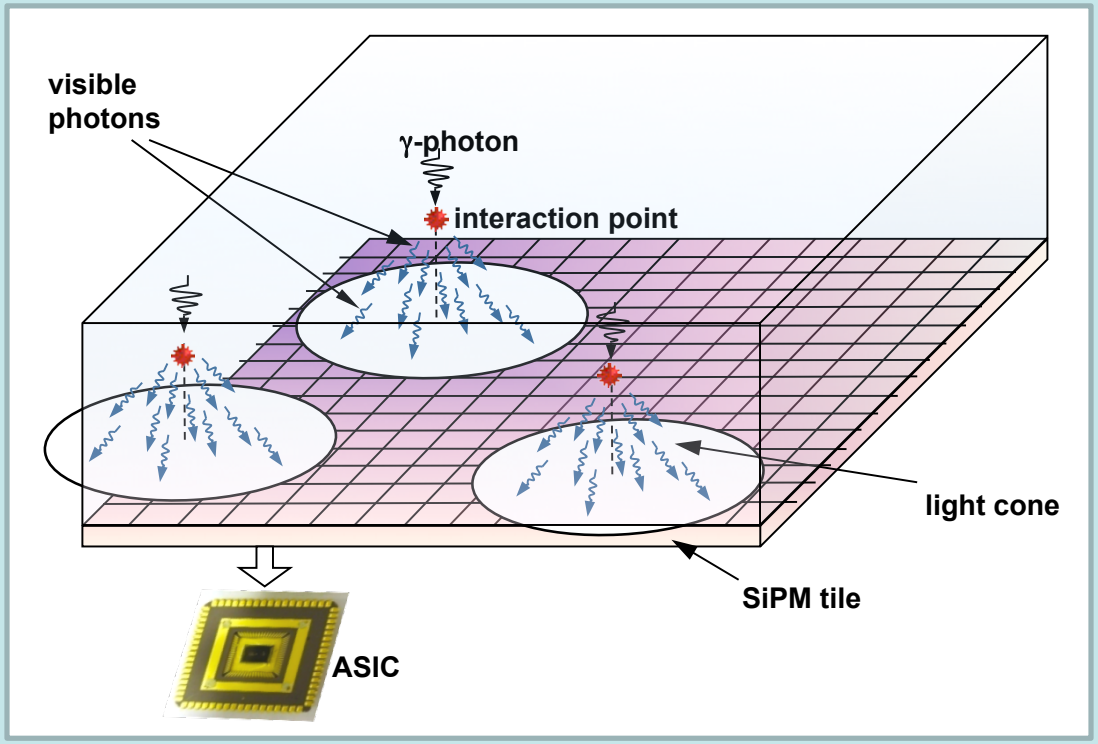
Changes in the architecture of the ASIC

Application: continuous scintillator slab

DOI information is related to the no. of SiPM in the cluster interested by the scintillation light

SiPMs at the border of the cluster receive a small total number of photons, distributed in time according to the time constant of the scintillator

The current signal can be under the threshold set on the current level, thus they would be ignored in a sparse read-out acquisition



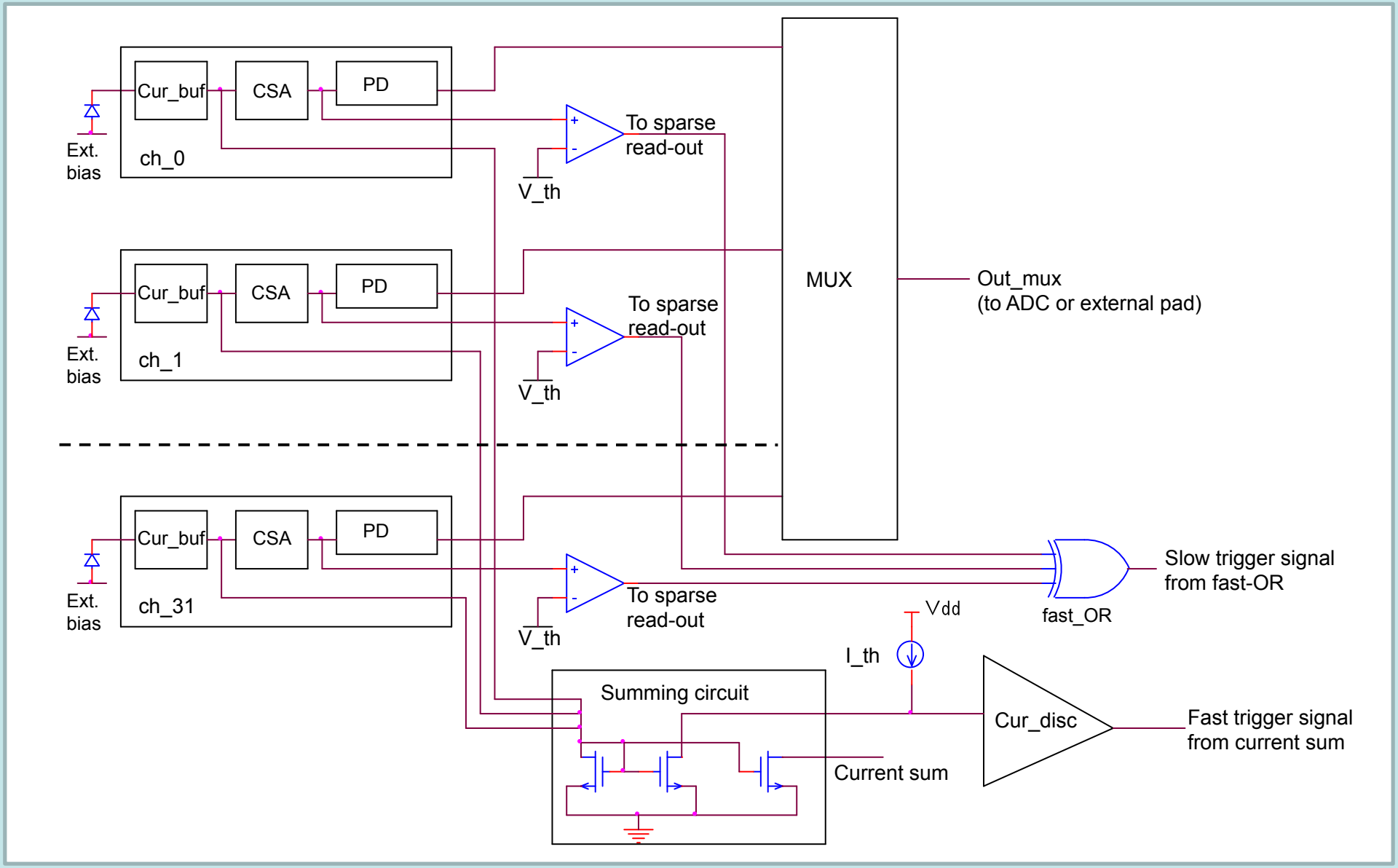
Proposed solution

1) *Sum of the current pulses from all the channels (exploiting the "fast" signal path of the FE)*

2) *Current discriminator which fires when the **sum** of the currents overcomes the threshold*

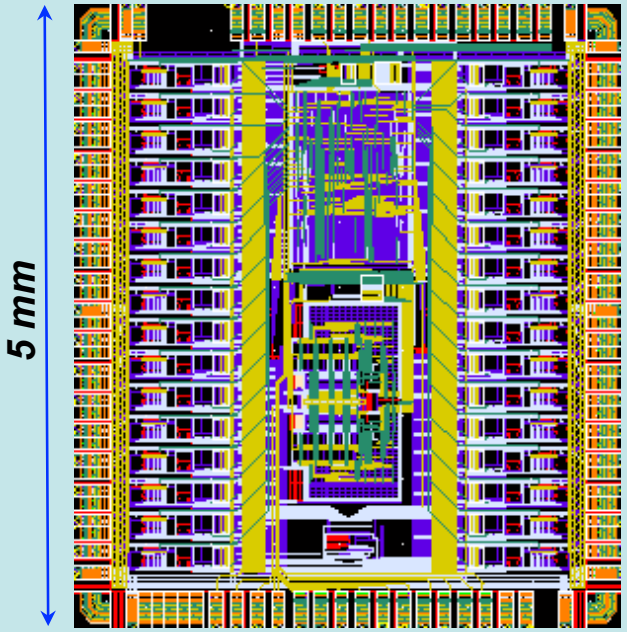
3) *Voltage discriminator at the "**charge**" output of each channel ("slow" signal path), instead of the current discriminator in the "fast" signal path, to make effective the sparse read-out operation*

New proposed architecture



Last version of the ASIC: BASIC32_ADC

- *Internal 8-bit subranging ADC*
- *Extended dynamic range (more than 100pC)*
- *Improved configuration flexibility (524 bits) (channels configurable independently)*
- *Analog current sum output available*
- *The internal read-out procedure can be started by the "slow" (fast-OR of the voltage comparators) or "fast" (current discriminator) trigger*
- *Enhanced and improved management of the RO with external trigger*



Layout of the prototype

Work in progress

- Application of BASIC in a PET prototype: small animal PET (Pisa), AX-PET (CERN)
- Characterization of the last version of the ASIC
- Implementation of a new scheme for the compensation of the SiPM gain vs temperature
- Design of a new version of the front-end in SiGe technology
- Statistical modelling of the current pulse waveform produced by the system scintillator + SiPM + FE electronics