ASIC Development @ GSI

Holger Flemming

Experiment Electronic / ASIC-Design

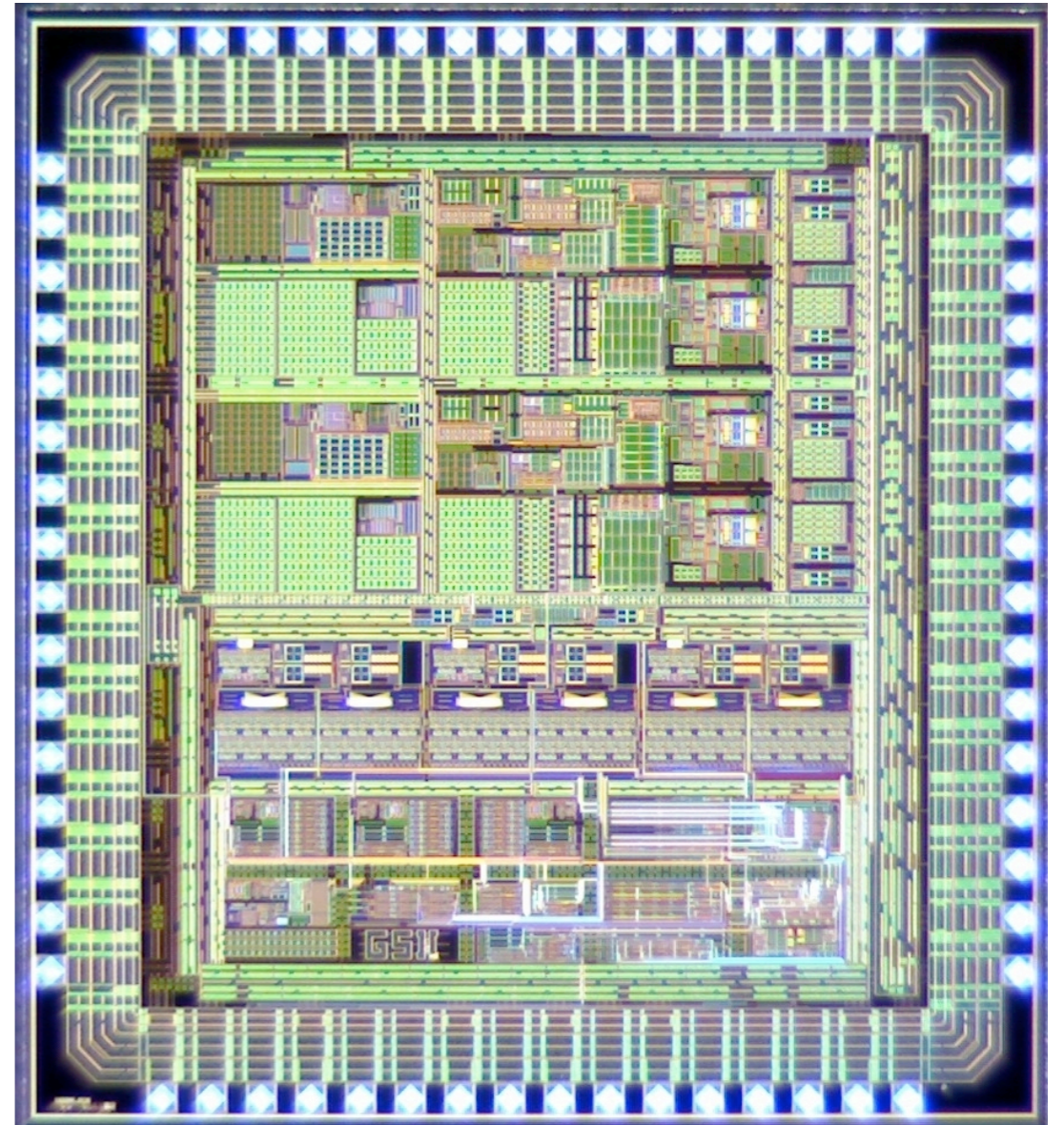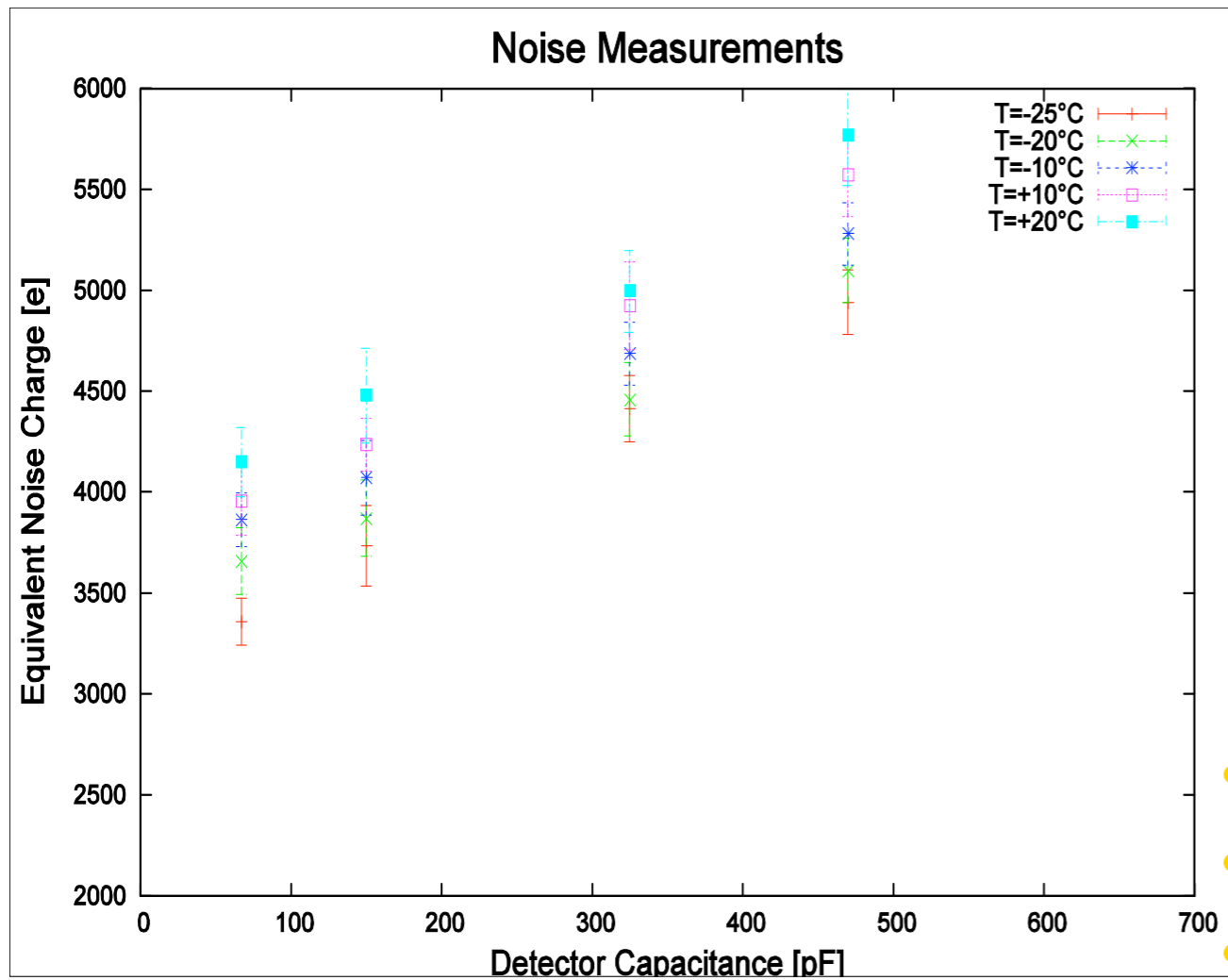# The GSI ASIC Design Group

- Since 2002 part of experiment electronics department
- 5 Team members
  - 4 designer
  - 1 technician
- CAD tools (via Europractice)
  - Cadence Design Framework II (Full Custom Analog and Digital Design)
  - Mentor Graphics Calibre (verification), ModelSim (digital simulation)
  - Synopsys Design Compiler (digital synthesis)
  - Cadence SOC Encounter (Place and Route of digital designs)
- Bond-Lab
  - Die-Bonder
  - Wire-Bonder
  - Manuel Prober
- Electronics Lab

Preamplifier and Shaper ASIC: APFEL

- **A**SIC for **P**ANDA **F**ront end **El**ectronics

- Readout of the electromagnetic calorimeter of the PANDA - detector
  - 11000 lead tungstate crystals read out by two large area avalanche photo diodes each

- Requirements:
  - Preamplifier and shaper
  - Input matched to the avalanche photo diodes, detector capacitance 300 pF
  - Low noise
  - Large dynamic > 10000
  - Pulse rate: > 300 kHz
  - Peaking time: 250 ns
  - Power consumption: < 50 mW/ch
  - Environmental temperature: -25 °C

The APFEL - ASIC

- 350-nm-CMOS-technology by AMS
- 2 poly- and 4 metal layer
- Supply voltage: 3,3 V
- 2 channels on: 3,3 × 3,4 mm^2

Noise Measurements plot: Equivalent Noise Charge [e] vs Detector Capacitance [pF], legend T=-25°C, T=-20°C, T=-10°C, T=+10°C, T=+20°C

- Noise @ 280 pF / -25 °C: 4248 e = 0,68 fC
- Upper limit of dynamic range: 6,89 pC
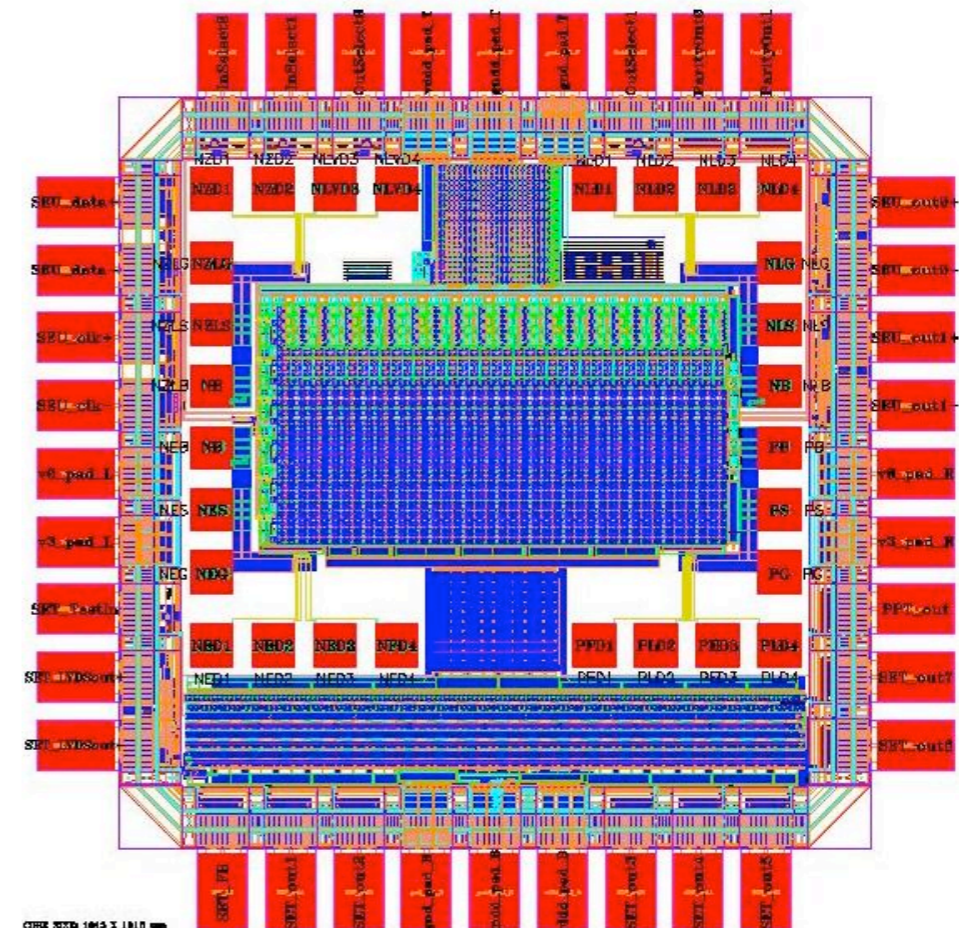- Dynamic range: 10140

Study on Radiation Effects

- Characterisation of the UMC 180 nm CMOS technology regarding:

    - Cross sections of single event effects
        - Single Event Transients
        - Single Event Upsets

    - Total Ionising Dose Effects of single transistors
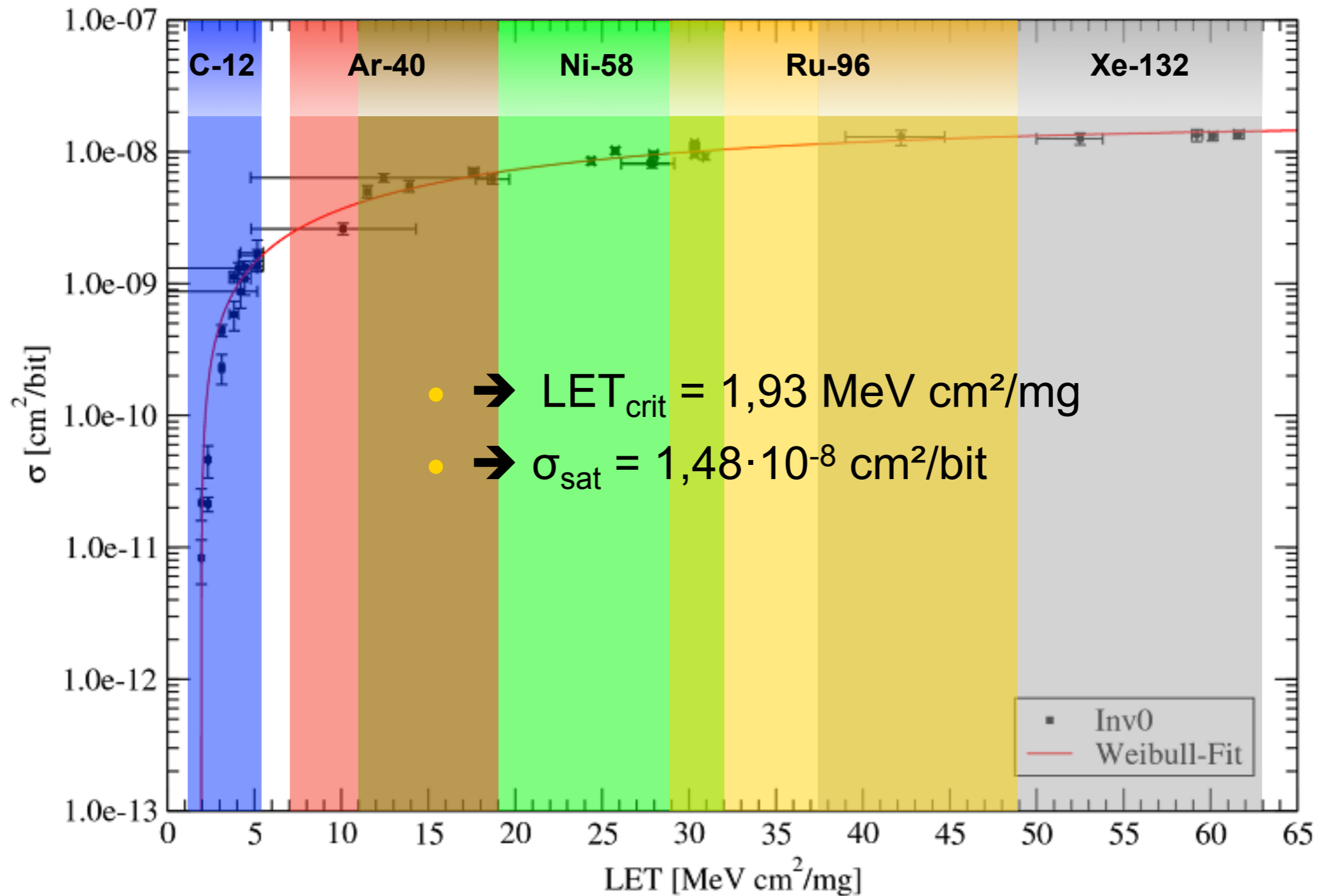   - Threshold shift
        - Increasing of leakage

Test chip GRISU

Bestrahlungsplatz X6

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Cross Section

➔ LET_{crit} = 1,93 MeV cm²/mg

➔ σ_{sat} = 1,48·10⁻⁸ cm²/bit

Holger Flemming, GSI, EE

Silicon Multiplier WS 10/2011
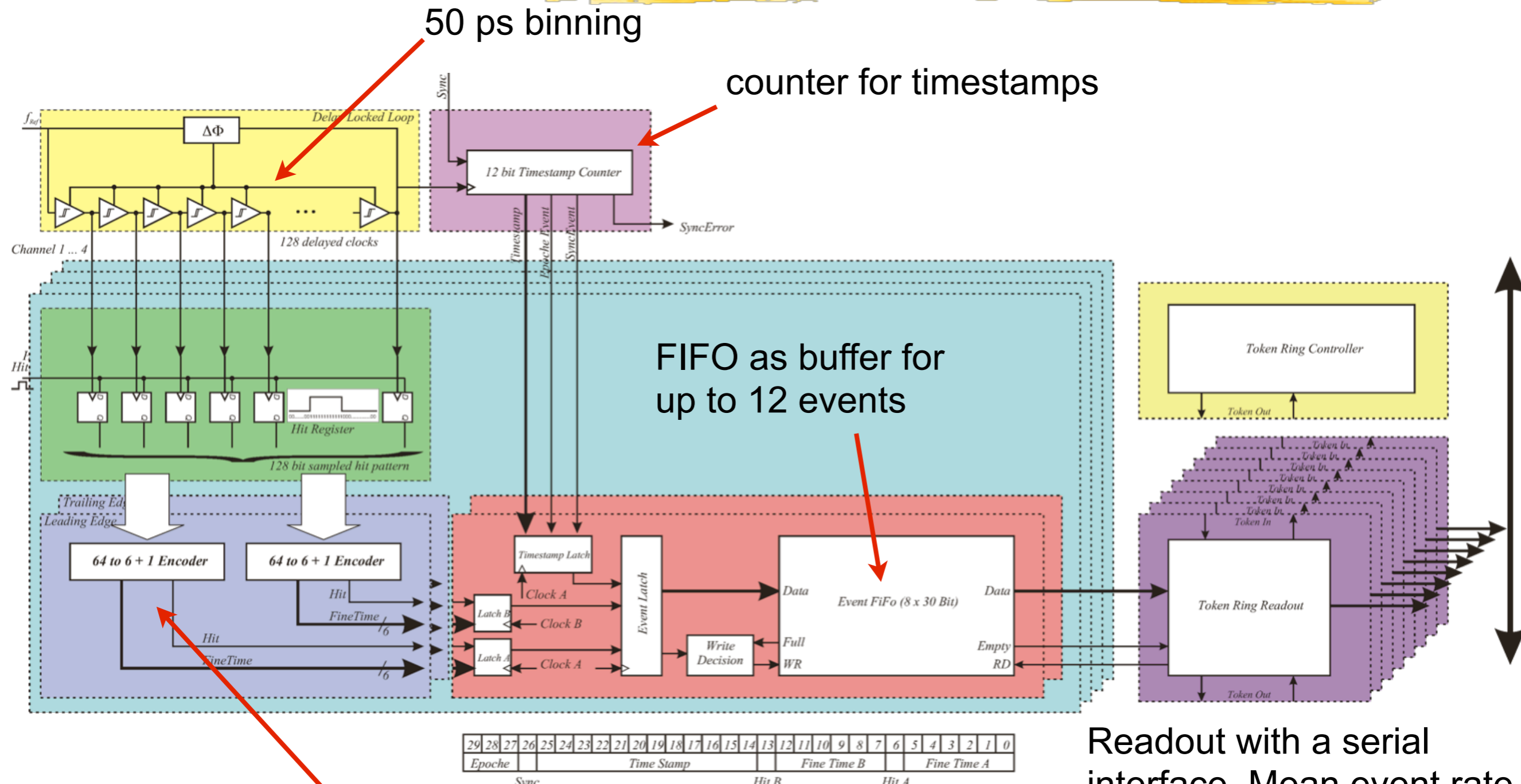
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The GSI Event driven TDC GET4

- Developed for the CBM Time of Flight Detector
- Requirements from CBM:
  - Time resolution
    - System < 80 ps
    - TDC   < 25 ps
  - Event rate > 50 kHz / Ch
  - Power consumption 60 mW / Ch
    - FEE : 30 mW / Ch
    - TDC : 30 mW / Ch
  - Double pulse resolution < 5 ns
  - Number of channels ~65000
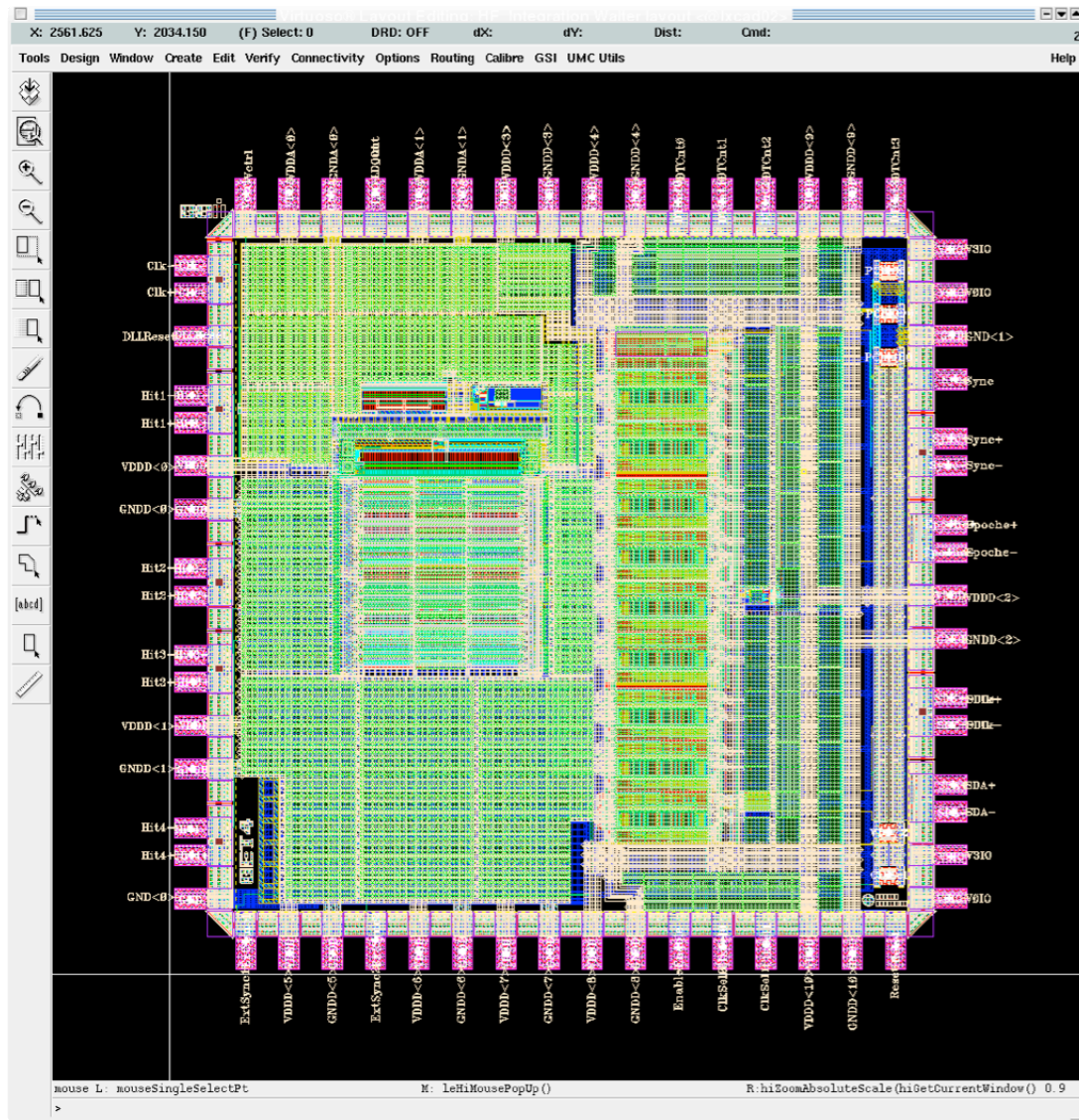 - „Time over Threshold" measurements
  - Data acquisition event driven

GET4 Overview
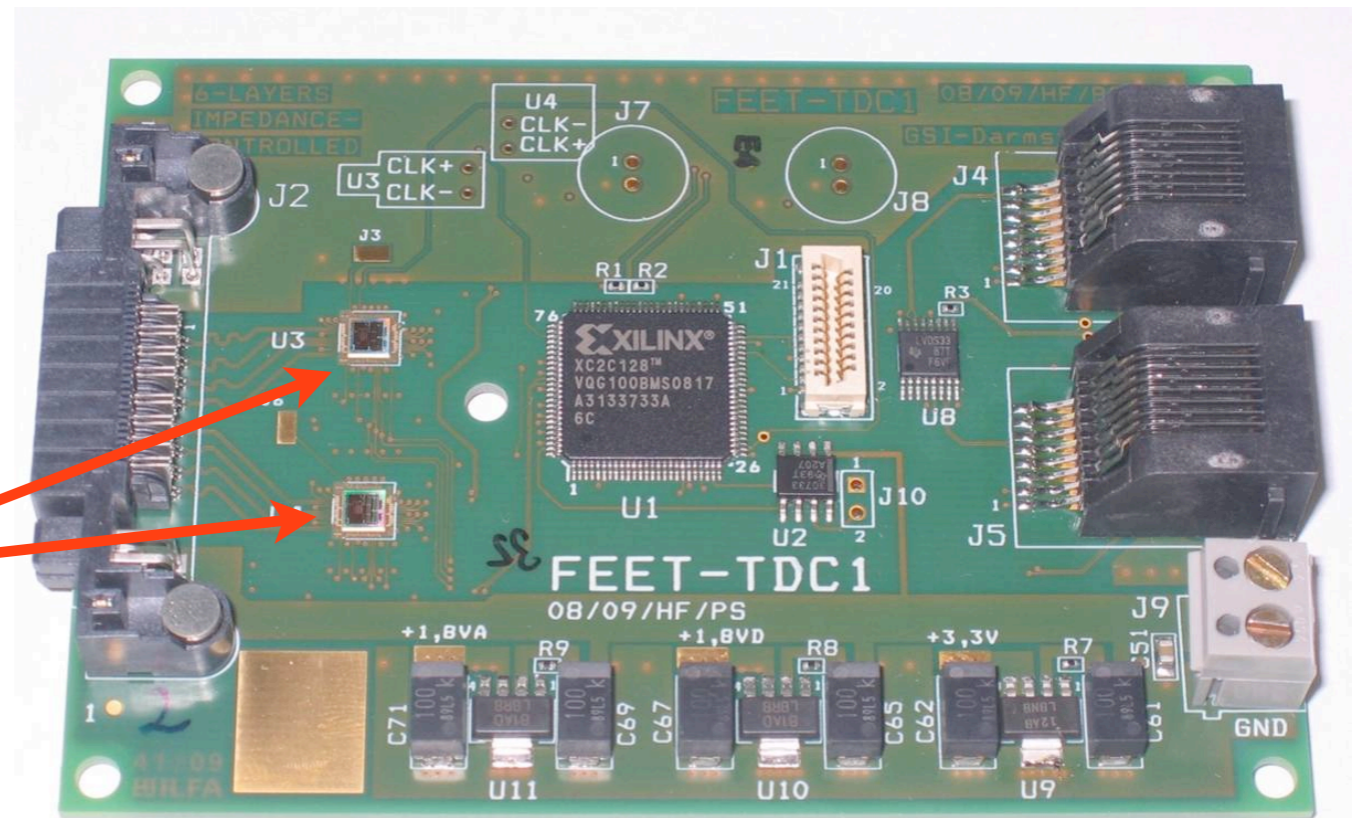

50 ps binning

counter for timestamps

FIFO as buffer for up to 12 events

Readout with a serial interface. Mean event rate the GET4 can cope with is given by data rate:
20 MBit/s for 100 kHz/ch

encoder can cope with 1 event / 3,2 ns
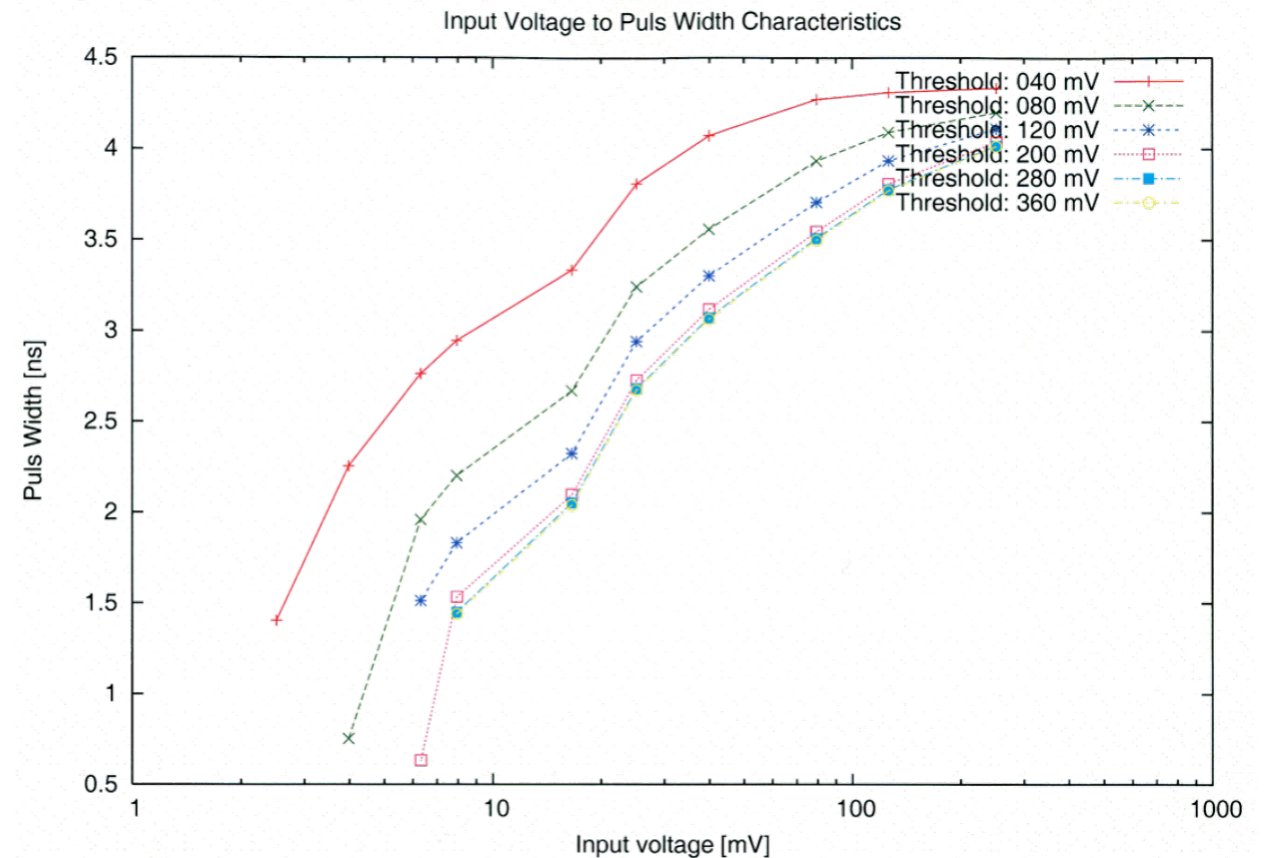⇒ burst rate: 320 MHz
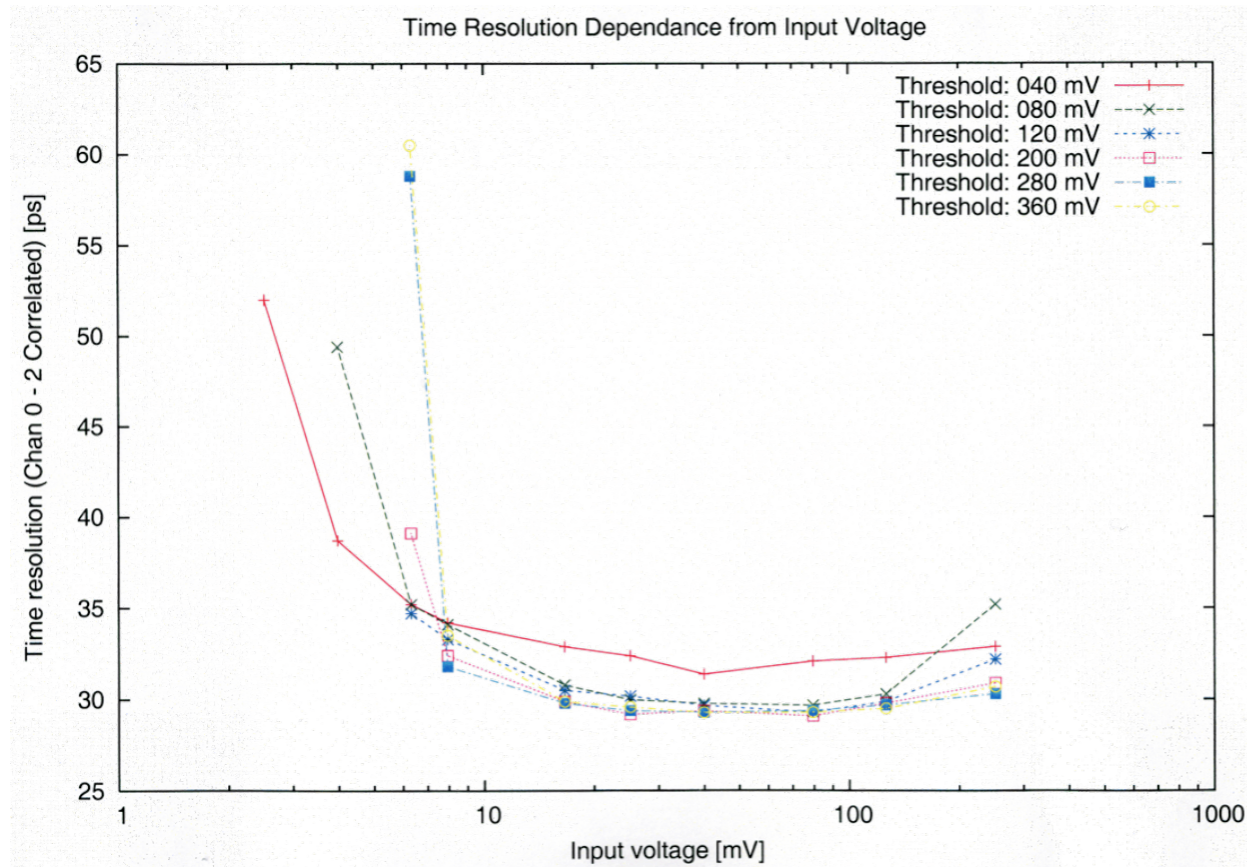
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The GET4 ASIC

- 180-nm-CMOS-technology by UMC
- 1 poly and 6 metal layer
- Supply voltages:
  - Core: 1,8 V
  - IO : 3,3 V
- Size: 3,24 × 3,24 mm^2
- Power consumption: 30 mW/ch

GET4-ASICs

Measurement Results of GET4 & PADI

- Preamplifier and Discriminator PADI developed by M. Ciobanu @ GSI
  - Preamplifier for low impedance differential detectors
  - RPC detectors @ CBM-ToF
- Time resolution PADI & GET4 ~ 21 ps (1 Channel uncorrelated)
- Pulse width < 1 ns resolvable

Current Developments

- Currently the next iteration of GET4 is under development (GET4-V1.0)
  - More efficient floor planning
  - Improved TDC core
  - Epoch counter
  - DLL lock state flag in data stream
  - Channel masking
  - Internal test pattern generator
  - I2C and / or SPI Master

  - Tape out foreseen for end of 2011 / early 2012

- CPU controlled readout controller
  - Aim: Reduction of serial links and readout hardware
  - Features: Buffering of event data, frame building, daisy chain readout
  - First test chip designed in 2010

The GPRC1