A Readout and DAQ Board for Precise Time Measurements

Outline

- Motivation
- HADES development: TRB
  – Synergy with other experiments
- The next step: TRBv3
  – TDC in FPGA and the results
- Summary

Motivation for a new FEE and DAQ system

Common Interests

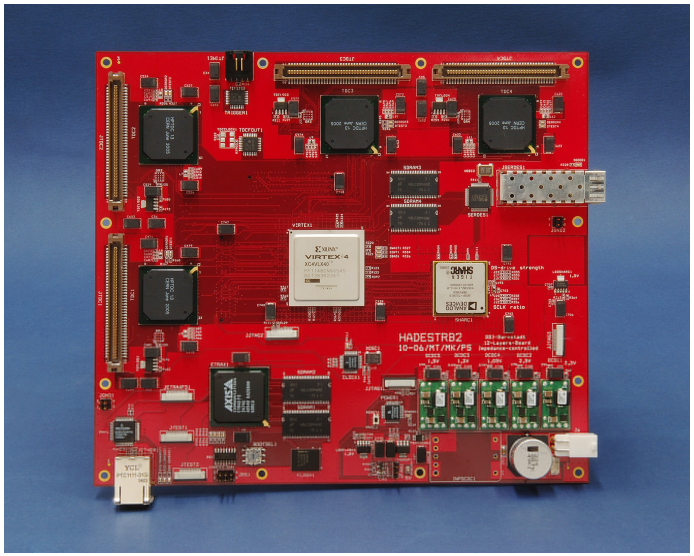
- high channel density, small, low power, „cheap“
- DAQ system should be as close as possible at the detector (reduce the cable-hell)
- Optical data transport
- DAQ software on board (no „VME-CPUs“ anymore)
- Simple power distribution (48V where possible)
- No ground loops, galvanically isolated

TRBv2

TRBv2 development for HADES

- 128 channel TDC measurements
- based on HPTDC → 30ps time resolution
- On board: CPU, Ethernet, 2GBit/s optical connection, 48V

- Synergy effect: TRB is used by other groups: KVI, Coimbra (for a PET-scanner) and by PANDA (DIRC and Straws, beam experiments September 2009 for DIRC detector), CBM-MVD and CBM-RPC-tests, DESY (beam diagnosis), etc...

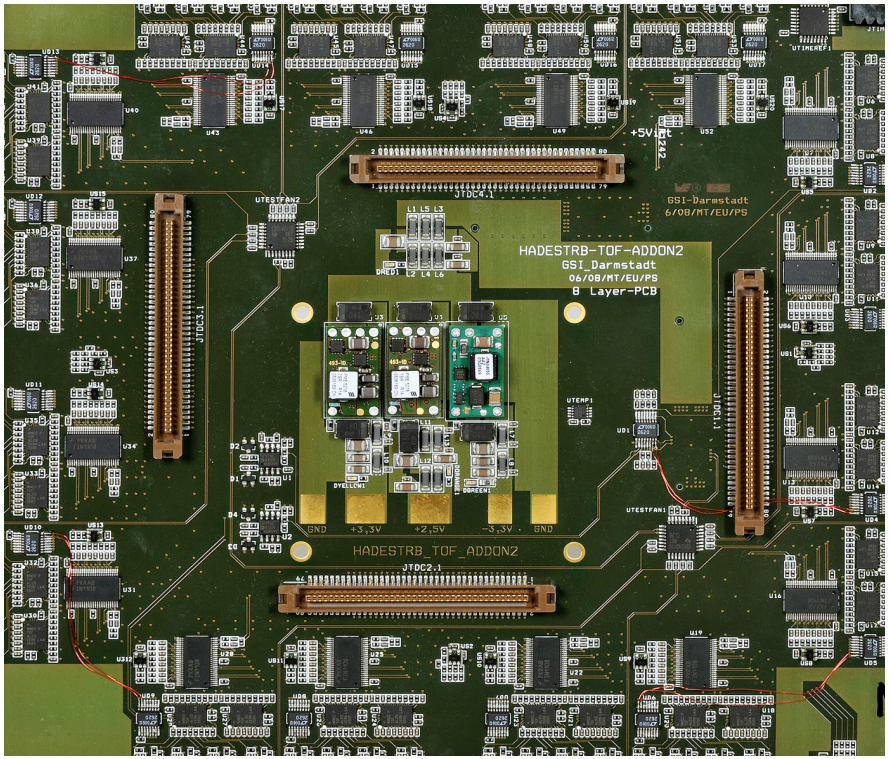


Publication:
„A General Purpose Trigger and Readout Board for HADES and FAIR-Experiments“
I. Fröhlich et al., Nuclear Science, IEEE Transactions on
Volume 55, Issue 1, Feb. 2008
Page(s):59 - 66

Discriminator + Q2W

PMT and similar applications

- Synergy with RPC-FEE development, the same concept (Q2W)
- Plugged to the back of the TRBv2
- Based on NINO-ASIC
- High integration reached (128 channels)
- Used by PANDA-DIRC in beam measurement and CBM-RPC-tests



We are done! Perfect World?

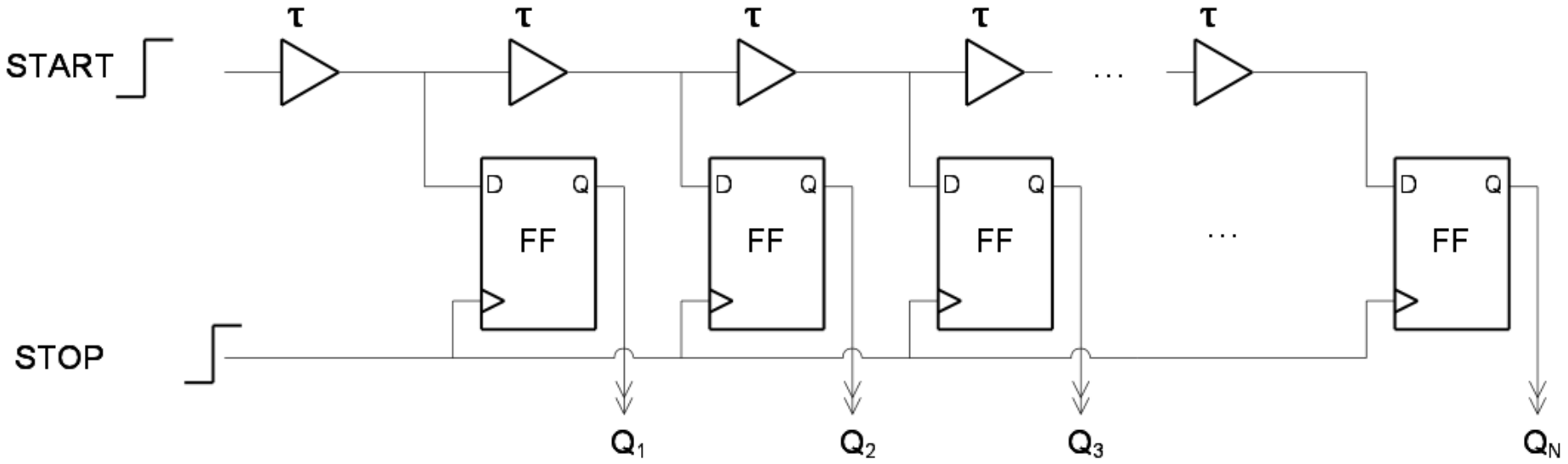
All problems solved?

- HPTDC:
  - Limited rate capability (1-2 MHz sustained)
  - Limited time resolution of around 30-40 ps (20 ps @ 8 ch.)
  - Is not produced anymore
  - 32 channels, instead of 33 needed
  - Not lead free solder compatible (240°C), hard to assemble new boards!
  - Minor bugs
- TRBv2:
  - 100 Mbit/s Ethernet, only **one** 2GB/s optical link
  - Processor on board (always obsolete)
  - FEE: No perfect adaptation to different experiments

→ **A new solution is needed**

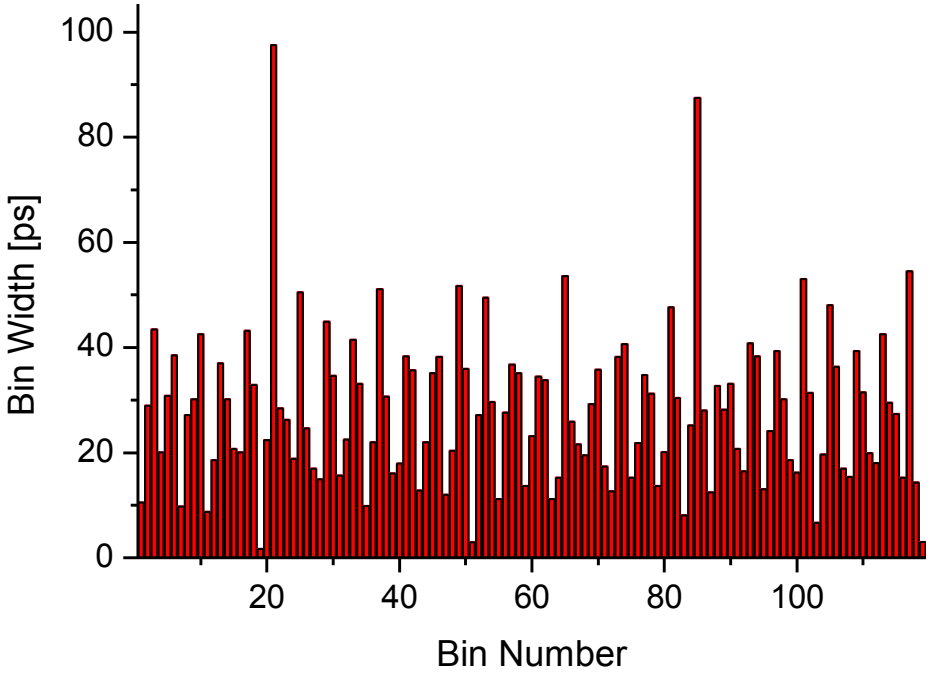
TDC in FPGA (I): Theory

- Developed, implemented and tested in hardware by Eugen Bayer
- The used method is very simple! **Tapped Delay Line**
  - The asynchronous input signal (e.g. one rising edge) runs through a chain of delay elements
  - The position of the 0/1 transition is stored in the FF array at the next rising edge of the system clock

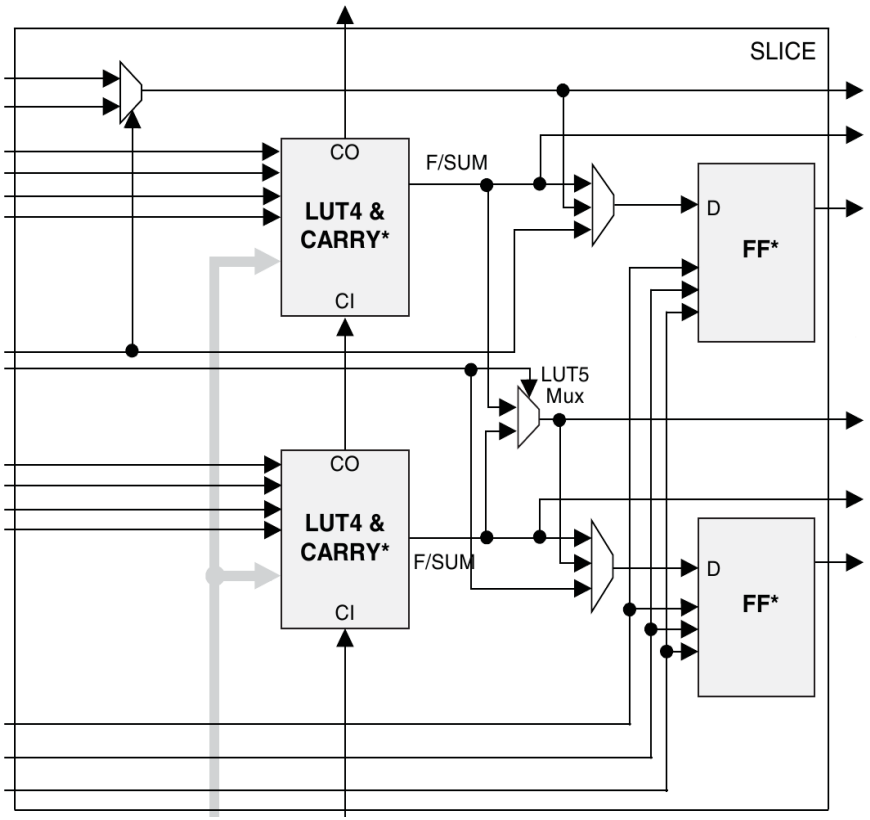


TDC in FPGA (II): Reality

- The "Carry-Chain" serves as a delay chain
- Carry-Chain multiplexers are the delay elements
- Delay (max.) = 45 ps (Virtex-4: CIN to COUT = 90 ps)
- Real delays vary: cell-by-cell calibration necessary

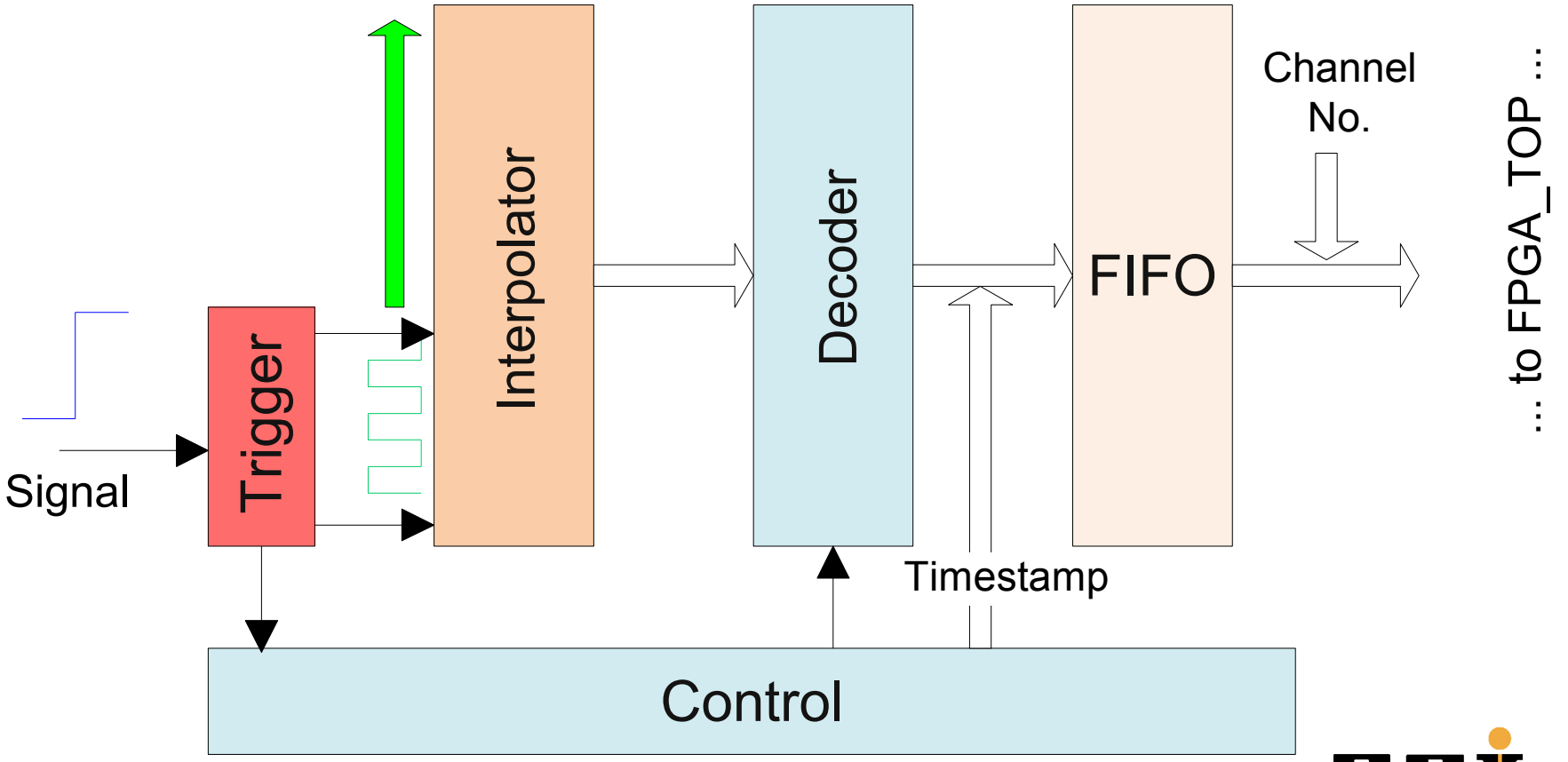


Lattice ECP3M Slice

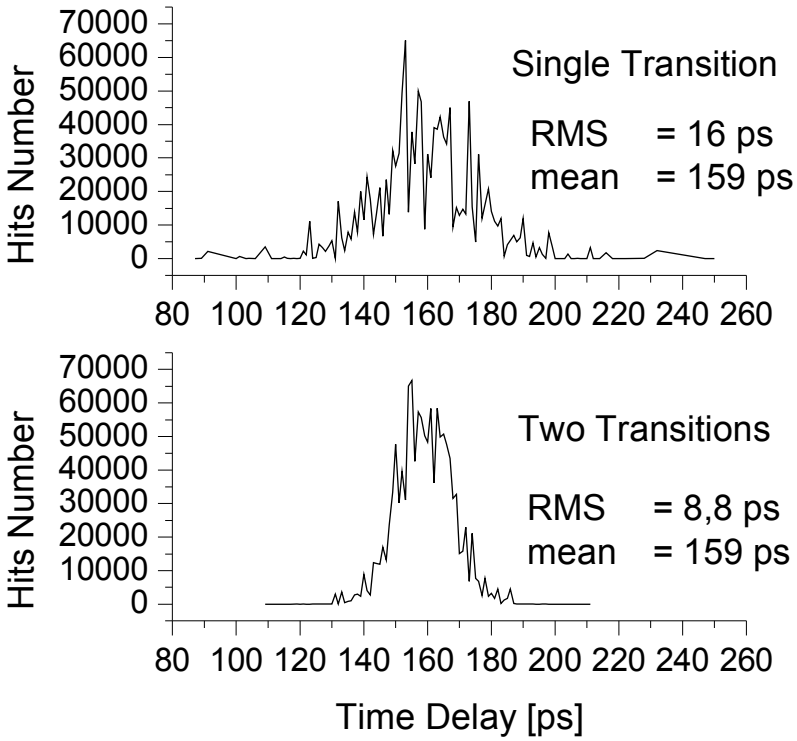


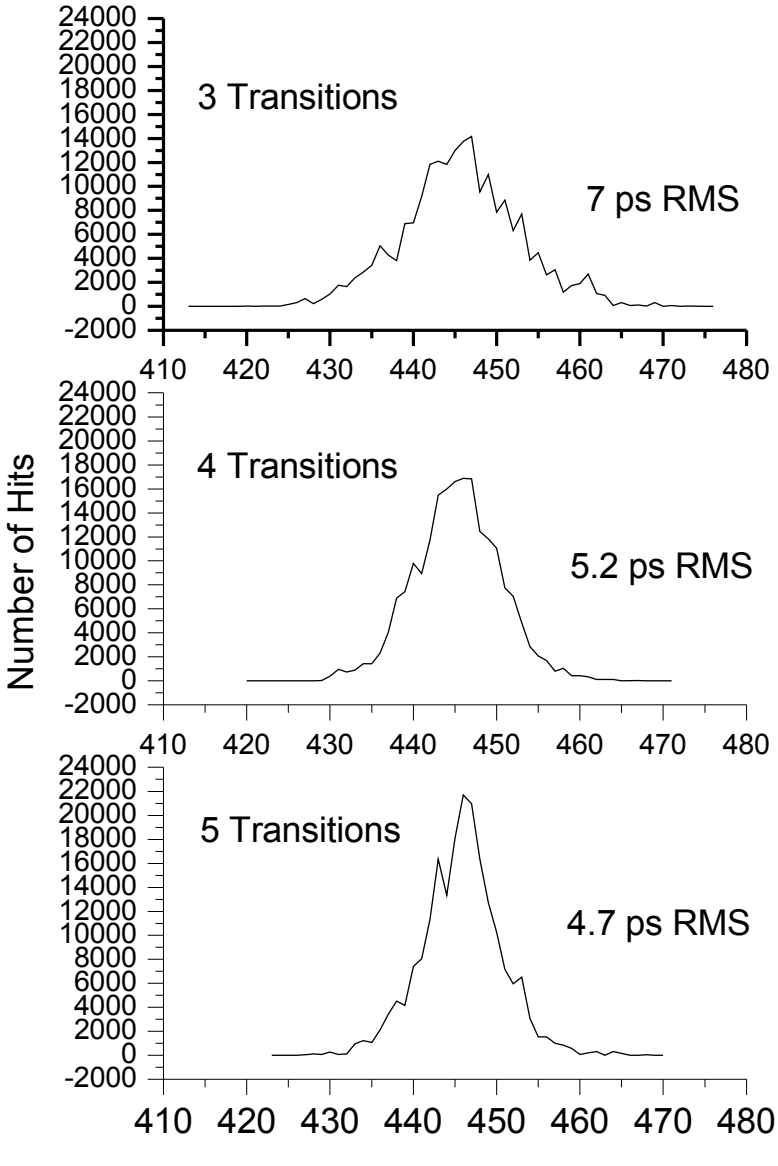
TDC in FPGA (III): Architecture

- TDL method extended with “Wave Union” method [Wu]
- Pipelined design
- Dead time = 15 ns (3 sys_clk cycles)
- Buffer for 512 hits per channel



TDC in FPGA (IV): Results





- TDC time resolution down to 5 ps RMS (two channels)
- World record!

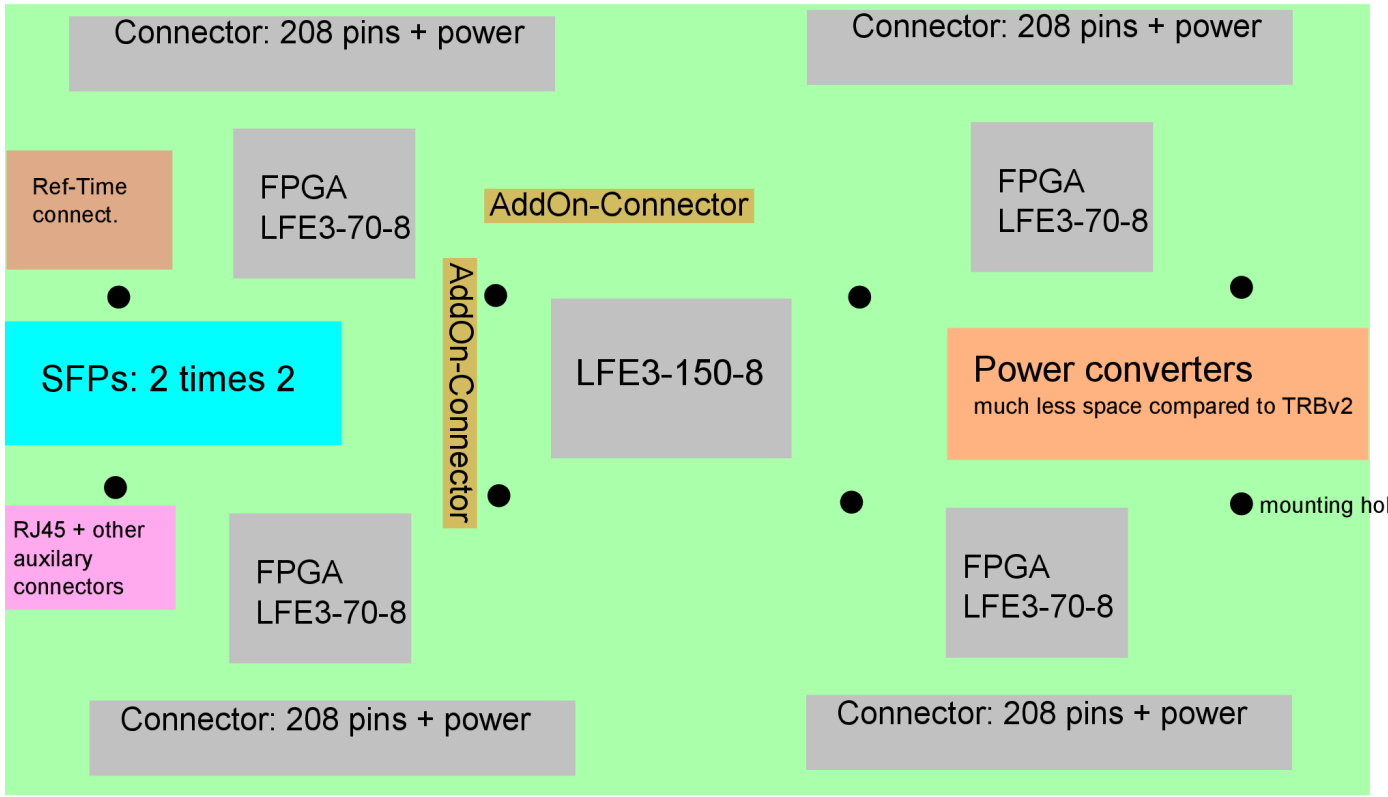
TDC in FPGA (V): Results

Answers to common questions:

- Temperature dependence
  - Below 5°C no new calibration table needed
- Voltage dependence
  - Mean moves around 6 ps for 10 mV supply voltage change → no problem for a good system design
- Crosstalk
  - No crosstalk measured for a correct PCB design
- Number of channels
  - Up to 56 channels on XC4VLX40 with 40k logic cell

→ **FPGA in TDC works extremely well! Let us use it!**

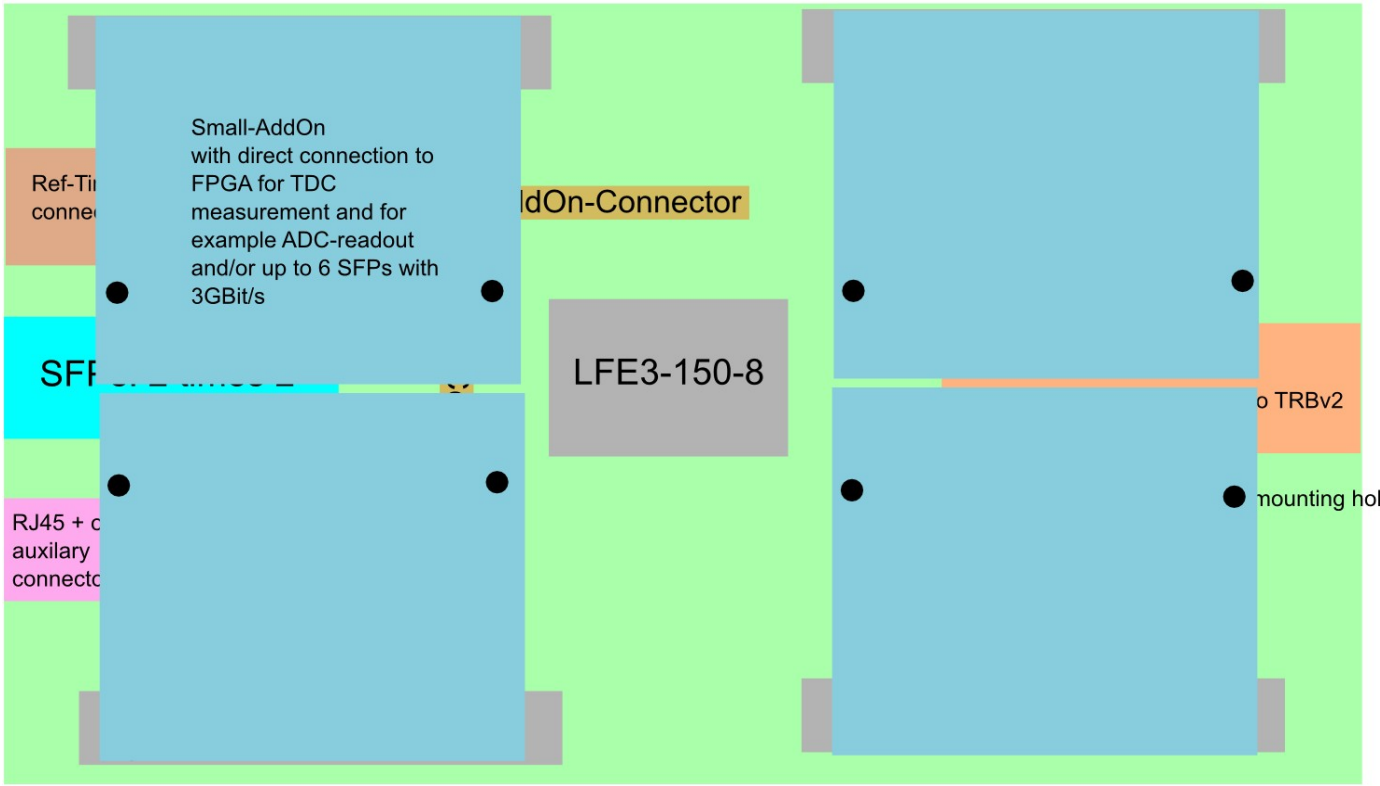
TRBv3, Layout + Features I



Result of experience with TRBv2:

- 4 modern FPGA-TDCs with high pin count (208) connectors
- More efficient and less noise power supply (48V)
- More SFPs (4 times up to 3GBit/s and/or 1GBit/s Ethernet)
- **No** DAQ-Processor, **no** DSP, **no** big memory

TRBv3, Layout + Features II



Result of experience:

- Small AddOns with 208 pin-connector and 6 SERDES-connections
- Applications: FEE-connector + Discriminator + Q2W + SFP + fast ADCs (with SERDES)

TRBv3: Status

- Designed to be flexible for many common needs
  - Included all wishes of PANDA Straw, PANDA-DIRC, HADES (fast diamonds), CBM-MVD
- Design + Schematics finished
- PCB in June
- 3 persons dedicated for commissioning
  - All code components are existing (TRBv2 + FPGA-TDC)
  - Missing: FPGA-TDC tailoring for PANDA needs, Slow control via UDP (no CPU), etc.

Summary

- TRBv2 proved to be very useful for many applications
  - HADES RPC, TOF, Diamond start detector, etc., Human PET Scanner, PANDA-Straw, PANDA-DIRC-Tests, CBM-RPC-tests, CBM-MVD and many other small applications
- New TDC in FPGA technology allows for a more flexible device (and time resolutions below 10ps RMS)
- Learned from experiences and errors made
- TRBv3 seems to be very useful for smaller table top setups **and** for large systems (as the TRBv2)

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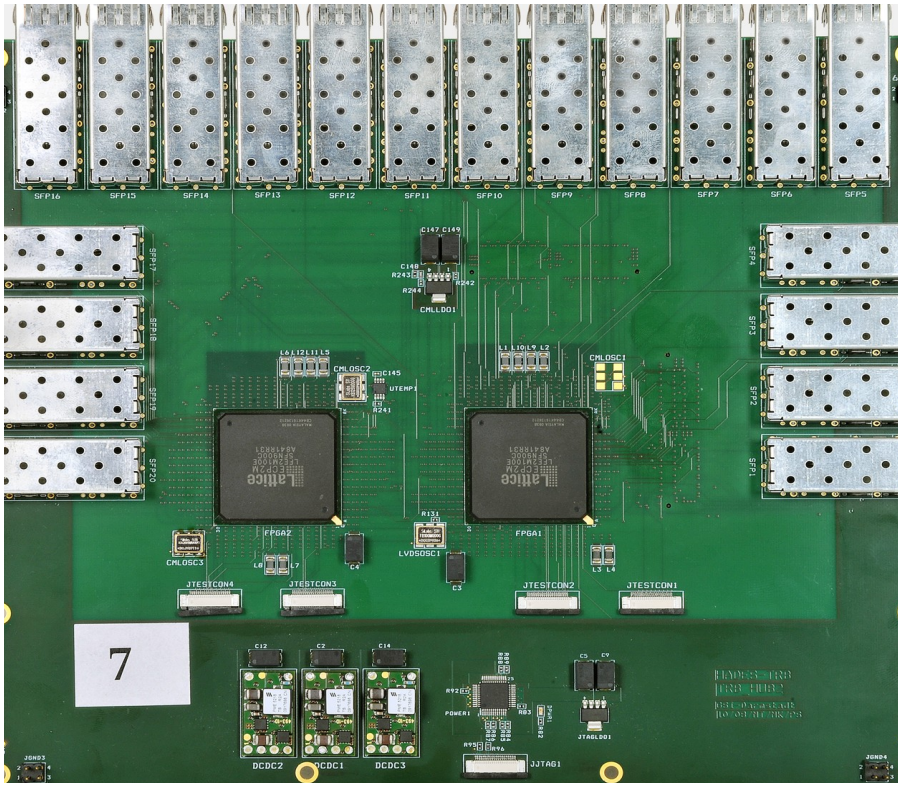
Thank you for your attention!

- Backup slides start here

Trigger Network

TRB Network

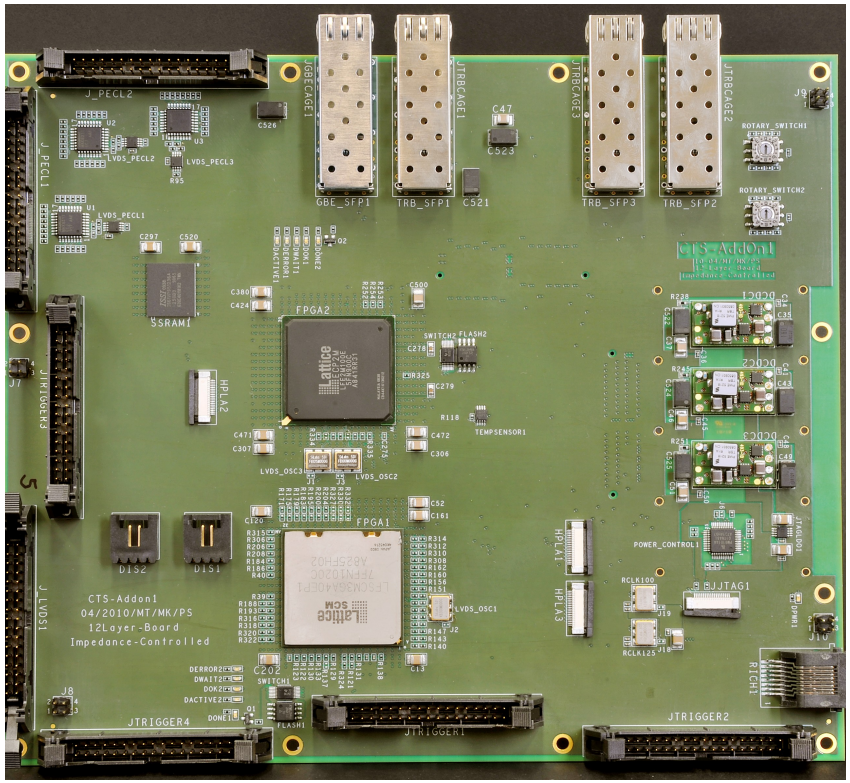
- Network protocol is stable and has the needed performance (low latency)
- Optical HUB hardware version 2 for direct GBit/s Ethernet connection has been produced and successfully deployed



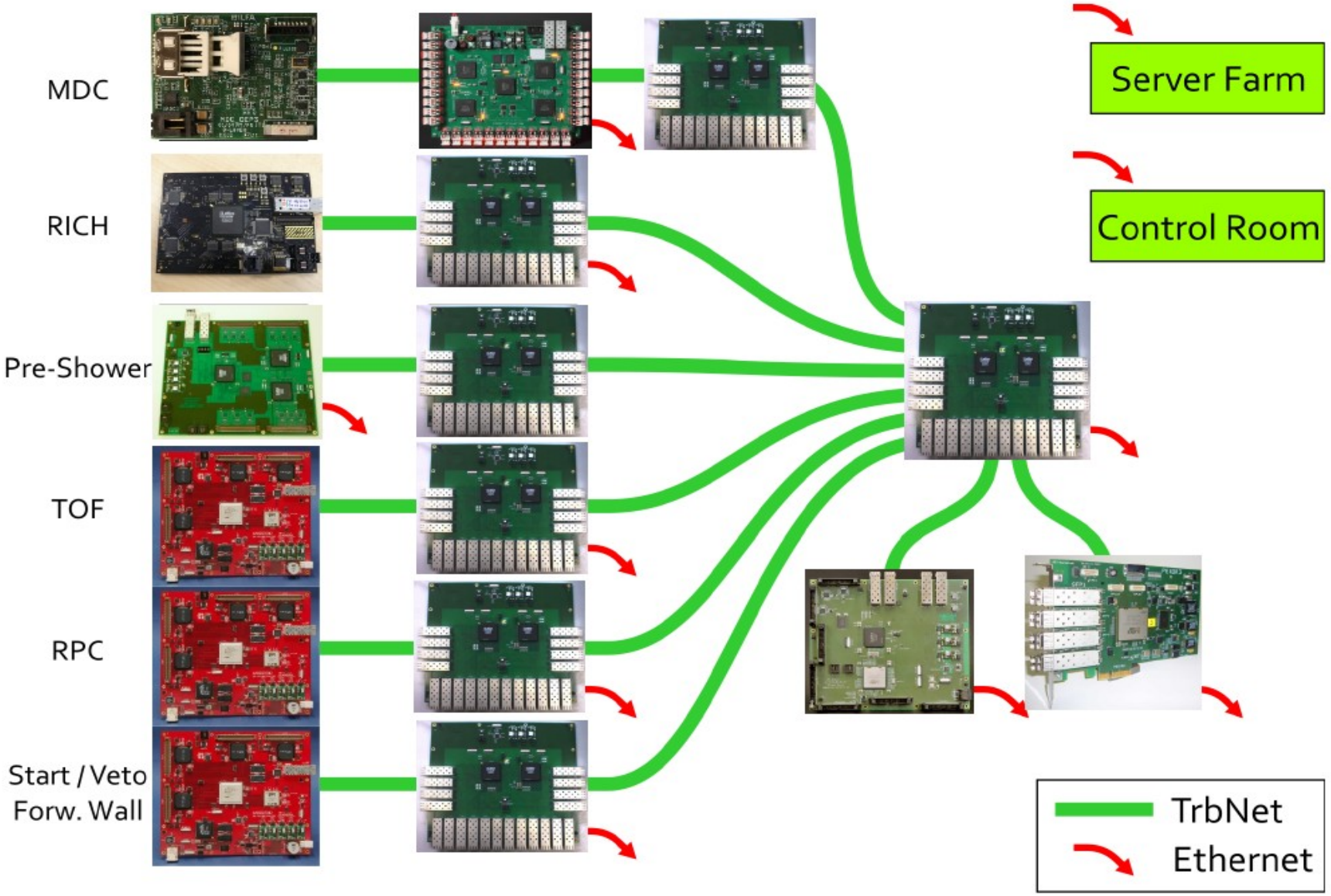
Description of Work, Trigger System

Central Trigger System (CTS)

- TRBv2 + Connectivity for Physics-Triggers
- Complex trigger decisions
- Synchronizes all sub-systems
- Has been verified during HADES beam times
- 800 MHz sample rate of input signals
- Large number of input and fanout channels (LVDS, LVpECL)



System Overview



Summary, HADES DAQ-FEE-System Upgrade in Numbers

- **Electronics**
  - 520 digital PCB with FPGAs
  - 4,500 PCBs in total
  - 1,500 ADC channels (multiplexed from 80,000 signals)
  - 30,000 TDC channels
  - 100 kHz trigger rate
  - 250 MByte/s (avg.), 400 MByte/s (peak) written to disk
- **DAQ Power Supply**
  - 4,000 voltage regulators
  - 9 power supplies
  - 5.5 kW total power (FEE only)
- **Data transport**
  - 550 FPGAs
  - 1050 optical transceivers (SFP & FOT)
  - 7,000 m optical fibre (glass-fibre & POF)
  - 800 m 1-wire & CAN bus
  - 32 Ethernet switches
  - 15 Gbit/s uplink to Eventbuilders
  - 10 Gbit/s uplink to storage (Lustre / Tape)
- **Server farm**
  - 160 TB hard disks
  - 44 CPU cores
  - 100 TB storage / week